

GTLP Output Control Circuitry: Reduces Noise and Enhances System Performance

Introduction

GTLP device technology was invented by Fairchild Semiconductor as a high speed backplane interface solution. It has reduced output swing (Note 1) and patented output circuitry to address one of the most prevalent problems with high speed devices, output switching noise (i.e., overshoot, undershoot, and ground bounce). The output design incorporates wave-shaping techniques which optimize GTLP devices for driving backplanes. Its focus is to control the output level transition, thereby minimizing switching noise, electromagnetic interference (EMI), and reducing signal settling time.

Note 1: Reduced output swing is a term used to classify the output signal swing of a digital device. Devices in this category have an output swing less than standard TTL or low voltage TTL levels. In general, the output swing is usually 1V or less.

Background

Stringent system timing budgets and increased data throughput requirements are changing the way backplanes are designed. As such, the choice of device technology for driving the system backplane is critical. For a backplane driving device to be considered, it must be able to meet the drive and settling time requirements of the application and have propagation delays well within the timing budget. Just as important in this selection process are the output switching characteristics of the device. The switching outputs of digital devices create electronic noise that may result in electromagnetic interference (EMI). As backplane speeds increase, the adverse effects of this electronic noise on signal integrity are exacerbated.

Electronic noise comes in the form of power distribution and de-coupling noise, (EMI), cross-talk noise, and transmission line reflections due to improperly terminated lines. It is directly influenced by the output switching characteristics of digital devices. Consequences of output switching

noise are; increased bus settling times which reduce system data throughput, false triggering that results in erroneous data or bus contention, and radiated electronic emissions that are above the government limits for EMI. To minimize these effects in a system, it is imperative to implement good PCB layout of the signal line distribution and power/ground planes. It is equally important to select a digital device technology, such as GTLP, which is specifically designed to address output switching noise.

GTLP is a digital device technology with reduced output signal swing. As a rule of thumb, digital devices with reduced output swing offer the system designer a variety of advantages over the standard rail-to-rail (CMOS) or TTL devices. In general, these advantages include: improved switching speeds, lower power consumption, and less device generated noise. GTLP not only has a reduced output swing, but specially designed output circuitry that "controls" the output transition. This control enables a GTLP device to have clean, moderate, output transitions with minimal settling times when driving terminated transmission lines.

How Does the GTLP Output Control Circuitry Work?

As previously stated the output transition, or edge rate, of a digital device is an important factor in the output noise performance of the device. This can ultimately effect the signal integrity on the backplane. The magnitude of the output switching noise generated is not only a function of the size of output swing, and any impedance mismatches on the backplane, but of the output transition time when changing the state of the bus. In general, faster transition times generate greater output noise. Figure 1 details the areas of the output transition (LOW-to-HIGH and HIGH-to-LOW) that are addressed by the GTLP output design.

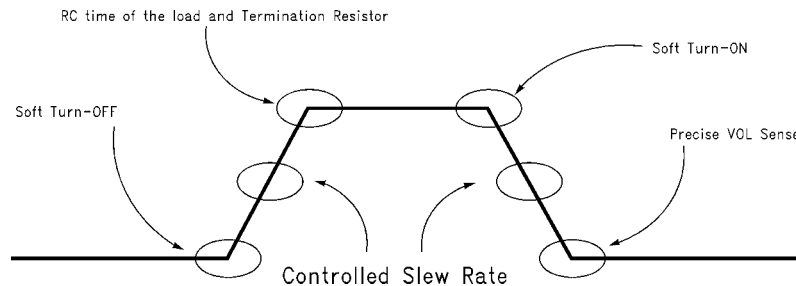


FIGURE 1.

How Does the GTLP Output Control Circuitry Work? (Continued)

The GTLP output structure is an open drain NMOS transistor that, when connected to a bus or backplane, is terminated by a pull-up resistor to a termination voltage source of 1.5V (Refer to Figure 2, transistor Q1). Switching the level of the bus is accomplished by turning the output NMOS transistor ON (if HIGH-to-LOW transition), or turning it OFF (if a LOW-to-HIGH transition). The output control circuitry is designed to regulate the turn-on and turn-off characteristics of the output transistor (refer to Figure 1). The result is a gradual output transition with controlled slew

rate (transition time). The output level is monitored by sense circuitry to maintain a specified V_{OL} (Note 2) level and to control undershoot. The RC time of the load and pull-up termination determine the magnitude of signal overshoot. Thus, by proper termination overshoot can be minimized.

Note 2: V_{OL} is the static Low level achieved by the output of a logic device. The typical V_{OL} for GTLP is 0.45V (25 Ω to +1.5V bus termination) and for FCT it is approximately 0.1V* (*This assumes no static DC current).

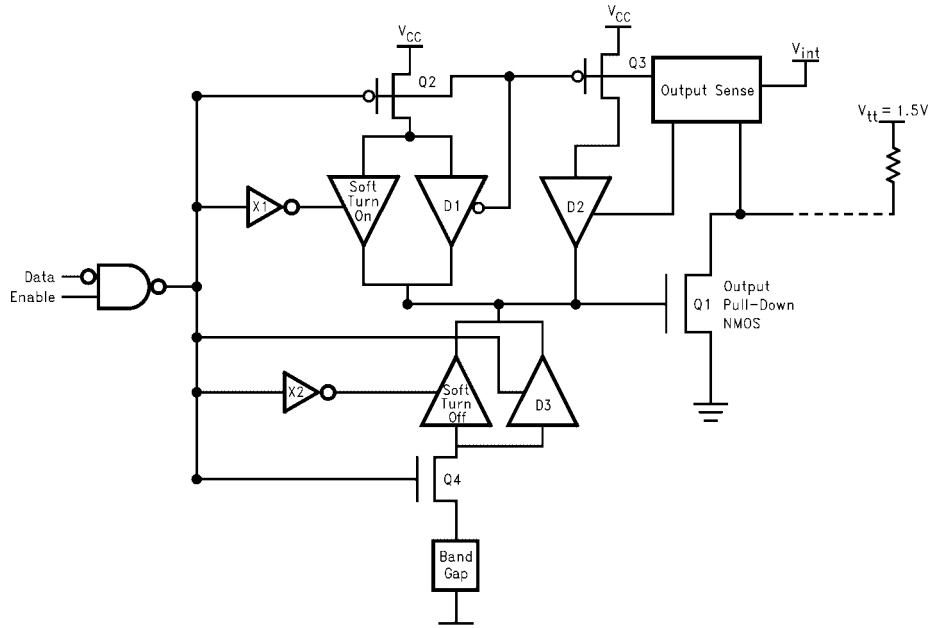


FIGURE 2.

The functional description of the output circuitry references the simplified schematic presented in Figure 2. The input pins to the output circuitry are DATA and ENABLE. They determine the state of the output (Q1) which is tied to a termination voltage supply of 1.5V through a pull-up resistor.

A HIGH-to-LOW output transition starts with the DATA pin low and ENABLE pin HIGH on the input of the NAND gate. The output of the NAND gate is LOW due to the inverted DATA input. The LOW level turns on PMOS transistors Q2 and Q3 which, in turn, enable the gate drive circuits, D1 and D2, to supply current from V_{CC} (+5.0V) to the gate of the output transistor Q1. The soft turn-on driver which is statically enabled assists the gate drivers in charging the gate of Q1. After a delay of approximately 250 ps the soft turn-on driver is disabled due to the LOW level that propagates through X1. This reduction in drive current ultimately decreases the charge rate of the gate of Q1, thus increasing the output transition time, or slew rate. The output sense circuit functions to maintain a stable V_{OL} level and minimize signal undershoot by comparing the output voltage level with an internally set reference (V_{int}). As the difference between the reference (V_{int}) and the output V_{OL} level goes to zero the output sense circuitry controls gate driver D2 to slowly turn off thereby completing a HIGH-to-LOW transition.

The LOW-to-HIGH transition is very similar to the HIGH-to-LOW. It begins with the DATA and ENABLE pins both HIGH. This results in a HIGH level output of the NAND gate which turns on transistor Q4 and allows the soft turn-off driver and the gate drive circuit D3 to sink the charge from the gate of transistor Q1. After a delay of 250 ps the soft turn-off drive circuit is disabled. The slew rate is then controlled by the discharge time of the gate of Q1 through drive circuit D3. When the V_{OH} level is approached and the output transistor is virtually off, the remainder of transition is controlled by the RC time of the load and termination pull-up resistor.

GTLP Output Performance?

The advantages of GTLP technology due to the output control circuit design become evident when evaluating electronic noise emissions (or EMI), ground bounce, and backplane driving performance. These parameters are discussed in this section with regards to GTLP technology. A performance comparison between GTLP and a typical high speed TTL technology (FCT-CT) is included.

EMI

The amount of high frequency content contained in a digital signal depends on the output transition. Sharper, or faster, output transitions contain more harmonic high frequency components. These high frequency components result in EMI emissions in a system. Relatively short PCB traces on a circuit board can act as antenna and transmit this unwanted noise. The higher the frequency, the shorter the

PCB trace needed for an antenna. Not only can the emissions from these antennae effect the environment around the system, but they can also have detrimental effects on other parts of the system. Since governmental agencies specify the allowable EMI levels that can be emitted from a system, it is important to understand and minimize any and all forms of electronic noise for compliance and reliable system design.

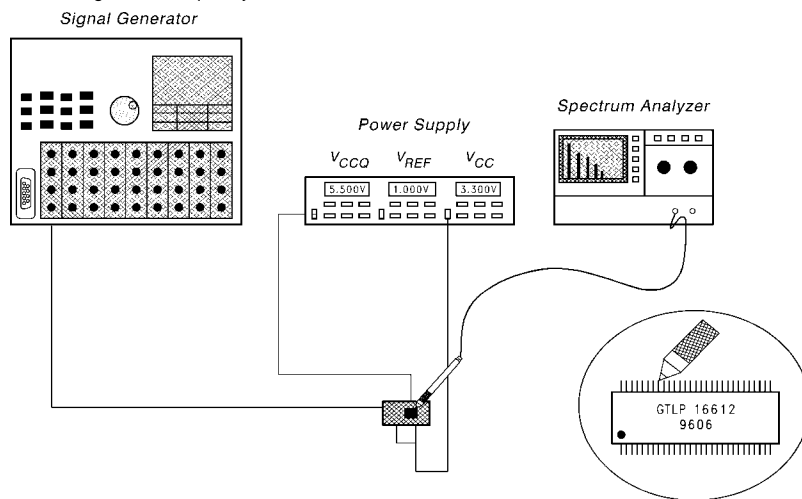


FIGURE 3.

EMI data, or the spectral energy content produced by a digital device, can be captured in two ways. The most common way, used primarily on electronic systems, is the open field radiated method. It involves using an antenna placed a specified distance (usually 3 meters) from an operating electronic system. The antenna is calibrated to receive any electronic noise emitted from the system. The test is done mainly for compliance of EMI regulations. The second, and

less common way, is through direct contact method (Figure 3). This test is usually performed on electronic devices. It is accomplished by monitoring the output of an unloaded device with a spectrum analyzer while the device output is toggling at a specific frequency ($f = 1$ MHz). The output signal is converted from a time domain waveform into its frequency domain components for analysis.

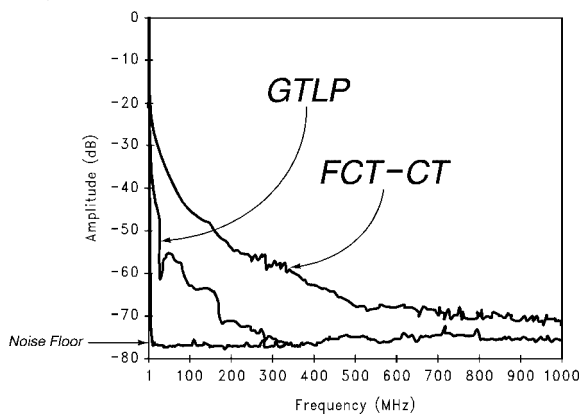


FIGURE 4.

The spectral content of a GTLP16612 output is plotted with comparison to an FCT16244-CT in Figure 4. The comparison clearly shows the difference in spectral energy content between these two technologies. The GTLP device with a reduced output swing and moderate controlled level transitions has a distinct noise performance advantage over this

standard TTL technology. Because of the nature of the GTLP output and its low spectral energy content, it can be an optimal solution in system backplane applications where EMI is of concern.

Ground Bounce

Another output switching noise phenomena is ground bounce. The ground bounce of a digital electronic device is a measure of how the "on-chip" ground level shifts under dynamic switching conditions. It is specified as V_{OLP} (the Peak level above the device static V_{OL}) and the V_{OLV} (the Valley or the lowest value of the shift below V_{OL}). The factors that exacerbate ground bounce are; the number of outputs switching in the same direction (HIGH-to-LOW) at the same time, the output edge rate, the inductance of the ground leads (Note 3) of the IC, and the load on the output. Ground bounce is, in effect, a limitation in the ability of the output of a device to bus current from its load into the system ground plane during the HIGH-to-LOW transition. The magnitude of this phenomena is exemplified when all outputs of a device are switching HIGH-to-LOW in unison. The ground leads of the IC that must "bridge" this, usually large, dynamic switching current from the output pins of the IC into the system ground, have a finite inductance. This inductance resists the instantaneous changes in current (di/dt) that are created by these outputs switching. The more outputs that switch in unison, or the faster the output transition time, the larger the di/dt . The inductive reactance of the ground leads of the IC creates a voltage differential ($V = L di/dt$) between the chip ground and the system ground. The result is a transient level shift in V_{OL} on the output. The di/dt , or dynamic change in current over time, and ground lead inductance determine the magnitude of the ground level shift.

The effects of ground bounce are seen not only as output noise, but as an internal shift of the input threshold region of the device (also called dynamic threshold). Both the output noise and the input threshold shift of a device can greatly reduce the effective usable noise margin on the

bus. In extreme cases, ground bounce can cause the false triggering of the switching device due to its moving internal threshold. It can also cause false triggering of a receiving device due to the output noise generated by the driver.

The two main approaches that are taken by IC vendors to minimize this form of electronic noise are to reduce the ground lead inductance, and/or control the output level transition of the device. Ground lead inductance can be reduced by adding more ground pins to the device. This creates more paths to bus the dynamic switching current from the chip to the system ground, thus the magnitude of the ground bounce is lowered. However, this is done at the expense of larger, costlier, IC packages. Secondly, controlling, or moderating, the output transition of a device can greatly reduce the di/dt into the ground leads which can greatly reduce the magnitude of the ground bounce without the package penalty. This approach was adopted in the design of the GTLP outputs.

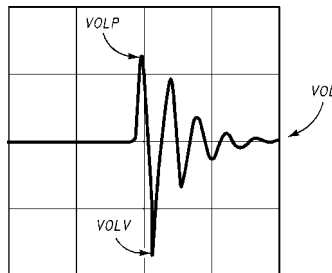
The diagram in Figure 5 is an example of the movement of the output V_{OL} level as would be seen on the "quiet" output (Note 4) of a device. The V_{OLP} and V_{OLV} points are marked for reference. Table 1 is a comparison of typical ground bounce data between the GTLP16612 and an FCT16244-CT. The effects of not only a low output swing, but the output edge rate, of GTLP reveal significant improvement in ground bounce performance over TTL technology.

Note 3: The ground lead structure of an IC, as defined in this document, includes the lead frame, bond wires (from the chip to the lead frame), and the "on-chip" ground traces. The "ground lead" inductance is the sum of the inductances of these three components.

Note 4: The "quiet" output refers to an output held statically in the LOW state while all other outputs of the device switch from High-to-Low in unison. The quiet output is monitored in ground bounce tests to determine the "worst-case" ground level shift due to dynamic switching.

TABLE 1

	Typical V_{OL}	Typical V_{OLP}	Typical V_{OLV}
FSC GTLP16612	0.45V	$V_{OL} + 0.25V = 0.70V$	$V_{OL} - 0.25V = 0.20V$
FCT16244-CT	0.01V	$V_{OL} + 0.81V = 0.82V$	$V_{OL} - 1.03V = -1.02V$



Quiet Output Switching Setup Conditions:

- Worst case (max) pin represented
- Load: 30 pF/500Ω (GTLP), 30 pF/500Ω (FCT)
- 17 outputs switching (GTLP), 15 outputs switching (FCT), 50% duty
- $V_{CC} = 5.0$; $V_{CCQ} = 3.3V$ (GTLP), $V_{CC} = 5.0V$ (FCT)
- All inputs deskewed to <10 ps
- Temp = Ambient
- $V_{th} = +1.5V$ (GTLP)

FIGURE 5.

Backplane Driving

System level performance is ultimately going to be the most important proving ground for a digital device technology. An example of the GTLP16612 driving an 18-slot backplane (18 inches long, $Z_o = 70\Omega$, $Z_{eff} = 40\Omega$, output of driver at the center of the backplane slot 9) is shown in Figure 6 and Figure 7. Once again, a technology comparison between the GTLP and FCT is made. The clean transitions exhibited during the LOW-to-HIGH and HIGH-to-LOW transitions are a trademark of the GTLP output design. The FCT16245-CT device included for comparison reveals the limitations of this TTL technology on a backplane, especially on the LOW-to-HIGH transition. The inability of the

FCT output to exceed the input high level threshold (2.0V) on the incident wave and the ringing associated with the transition results in increased settling time and induced electronic noise.

The system level advantages to the clean output transitions, resultant of output control circuitry, become evident in this comparison. First and foremost, they exhibit themselves in the form of reduced settling time when driving the bus. The ability to switch the backplane on the incident wave results in higher potential data rates. Therefore, the backplane design can be optimized for higher speed by selecting a low noise, low swing digital device technology such as GTLP.

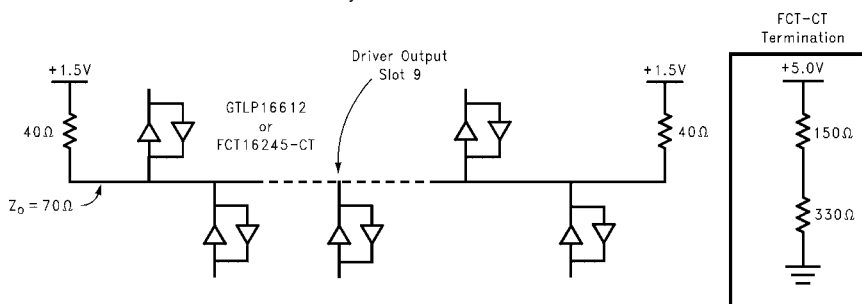
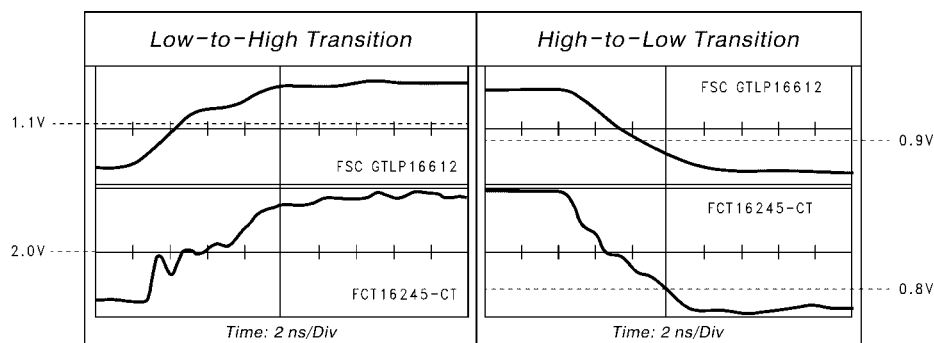


FIGURE 6.



Setup Conditions:

- 18 slot backplane (fully loaded); $Z_o = 70\Omega$, $Z_{EFF} = 40\Omega$
- Output of driver card shown (Center: slot 9)
- Terminations (GTLP: 40Ω to 1.5V, FCT: Thevenin termination 150/330 to +5V)
- Single output switching, 50% duty
- $V_{CC} = 5.0V$; $V_{CCQ} = 3.3V$ (GTLP), $V_{CC} = 5.0V$ (FCT)
- Temp = Ambient

FIGURE 7.

Summary

As backplane speeds continue to migrate toward higher and higher data rates, addressing the demand for increased data throughput can be a difficult task for a system designer. System and device level noise issues such as EMI, ground bounce, and cross-talk become paramount

in high-speed design. This makes the selection of a low noise digital device technology imperative. GTLP technology from Fairchild Semiconductor uses a proven approach for backplane driving and low noise performance, reduced output swing and controlled (moderate) output transitions.

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