

Application Note 4108

A Fairchild Power Switch based on Switched Mode Power Supply for CRT Monitor Use

1. Introduction

FS6S series is a Fairchild Power Switch (FPS) that is specially designed for off-line SMPS of CRT monitor with minimal external components. This device is a current mode PWM controller combined with a high voltage power SenseFET in a single package. The PWM controller features integrated oscillator to be synchronized with the external sync signal, under voltage lockout, optimized gate driver and temperature compensated precise current sources for the loop compensation. This device also includes various fault protection circuits such as over voltage protection, over load protection, abnormal over current protection and over temperature protection.

The **FS6S** series has a more rugged SenseFET than the previous Fairchild Power Switch series. The **FS6S** series features include burst mode operation for low power consumption in standby mode. This application note

describes the features and design considerations of the **FS6S** series for the monitor power supply, which improves upon the existing KA5S-series. The **FS6S** series has three package types: TO-3P-5L, TO-220-5L and TO-220F-5L as shown in figure 1-1.

The **FS6S** series has a synchronization pin, which accepts an external sync signal. In order to remove the screen noise generated by the switch action, the **FS6S** series synchronizes its switching with the external sync signal. When in power saving mode, the **FS6S** series pulls down the output voltages to a predetermined level and enters burst mode with a switching frequency of 50kHz.

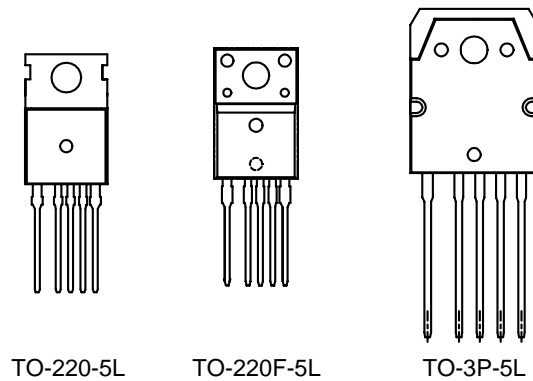


Figure 1-1. Package Line-Up

Table 1: Product Line-up (Monitor Application)

Product	Rating	Package
FS6S0765RCB	7A/650V	TO-220-5L
FS6S0965RT	9A/650V	TO-220F-5L
FS6S0965RCB	9A/650V	TO-220-5L
FS6S1265RE	12A/650V	TO-3P-5L
FS6S1565RB	15A/650V	TO-3P-5L

2. Internal Block and Important Features

2.1 Internal Block and Features

- Current mode control
- Burst mode operation for low power consumption in standby
- Higher rugged SenseFET (QFET)
- Optimized gate Driver for low EMI
- Low standby power consumption (low startup current and low operating current)
- Various internal protection circuits (Auto-restart)
 - Over Voltage Protection (OVP)
 - Over Load Protection (OLP)
 - Thermal Shutdown Protection (TSD)
 - Over Current Latch (OCL)
- Minimization of production defects by reinforcing V_{CC} surge immunity and internal diode.
- Reduction of secondary side diode voltage stress during startup and transient by introducing slope to the sync threshold voltage.

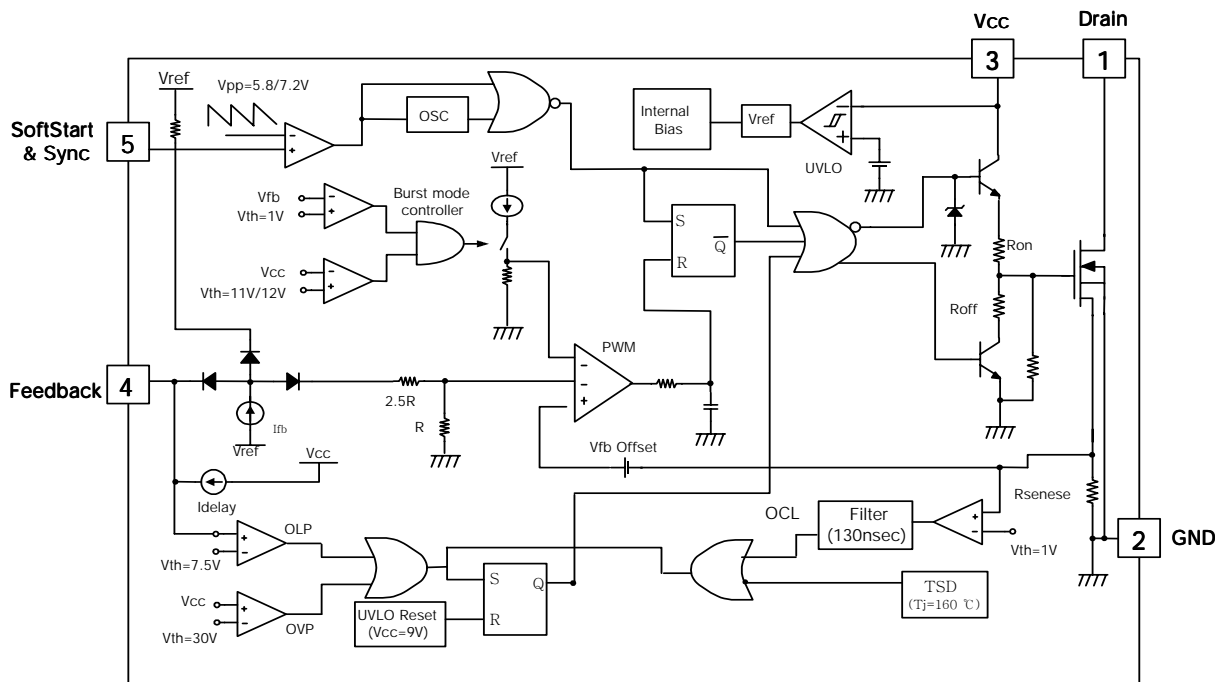


Figure 2-1. Internal Block Diagram

2.2 Starting resistor design and UVLO

By assuming an universal input voltage (85-265Vac), startup resistor is designed as follows:

The minimum average input voltage (V_a^{\min}) applied to the startup resistor, is obtained as

$$V_a^{\min} = \frac{1}{2\pi} \int_0^{\pi} (\sqrt{2} \cdot 85 \cdot \sin t - 15) dt$$

$$= \frac{2V_p - 15\pi}{2\pi} = \frac{2 \times 85\sqrt{2} - 15\pi}{2\pi} = 30.8V$$

The resistor for startup is calculated by assuming a startup current of 200uA as follows

$$R_{start} = 30.8 \div 200\mu A = 154K$$

The maximum RMS voltage applied to the startup resistor is approximately obtained as

$$V_{rms}^{\max} \cong \sqrt{\frac{1}{2\pi} \int_0^{\pi} (\sqrt{2} \cdot 265 \cdot \sin t - 15)^2 dt} \cong \frac{265}{\sqrt{2}}$$

$$= 187V$$

The maximum loss in the startup resistor is obtained as

$$P(\text{loss}) = \frac{(V_{rms}^{\max})^2}{R_{start}} = 0.23W$$

The FPS starts switching operation when the V_{CC} voltage reaches 15V (the start voltage). Once it starts switching, the current consumed by the control IC increases to 10mA (operating current). The starting resistor cannot provide the operating current and consequently, the transformer auxiliary winding supplies most of this current once FPS starts up. The start time will be delayed if the V_{CC} capacitor is too large, so a moderately sized capacitor should be used. Typically, 22 ~ 47μF capacitor is used. This operation is described in Figure 2-2. V_{CC} should be maintained above 9V after starting. However, it should be set so that OVP (OVP threshold is typically 30V) is not triggered during the normal operation.

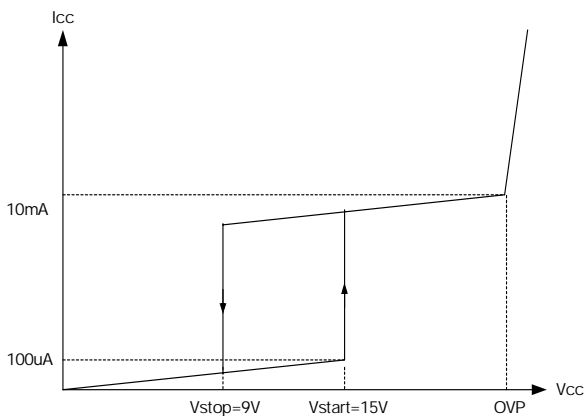


Figure 2-2. Start-up Waveform

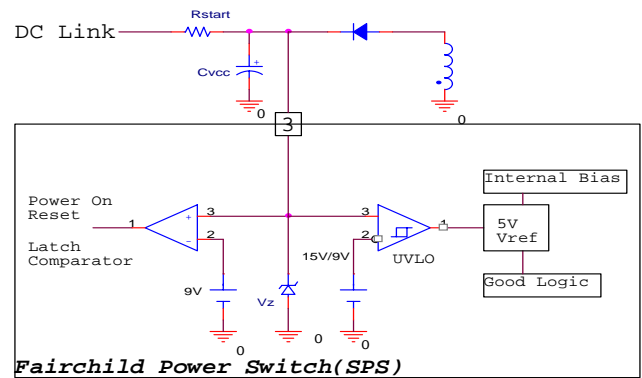


Figure 2-3. UVLO Block

2.3 Fairchild Power Switch Protection Circuits.

FPS has several self-protection circuits, which can be used without adding external components, thus providing system reliability without increasing cost. Under auto restart mode, protection circuits become disabled when V_{CC} falls below 9V (stop voltage), after which the FPS tries to restart. Under latch mode, protection circuits become deactivated only when V_{CC} falls to 6.5V (reset voltage), then the Fairchild Power Switch tries to restart. When V_{CC} drops to 9V due to latch protection, the operating current of the IC drops from 10mA to 100μA. Therefore the V_{CC} capacitor starts to charge towards 15V through the starting resistor. For V_{CC} to fall to 6.5V (reset voltage), the input voltage must be removed.

2.3.1 Over Load Protection (OLP)

Overload as described here is different from a load short circuit. It is a condition where a load becomes greater than the preset level, though it is operating normally.

Essentially, the overload protection circuit forces the Fairchild Power Switch to stop its operation if the load draws a higher current than the predetermined maximum value. A problem associated with this type of protection circuit is that it can trigger erroneously on load transients. As a security measure, the Fairchild Power Switch triggers the protection circuit after a specific time delay. This avoids false triggering on short load transients.

The above operations are executed as follows. Since the Fairchild Power Switch uses current mode control, maximum switch current is limited internally. For a fixed input voltage, this limits the power. Therefore, if the power at the output exceeds this maximum, V_O shown in figure 2-4 becomes less than the set voltage, and KA431(LM431) can draw only the allowed minimum current. As a result, the photo-transistor's current becomes zero. If all the current of the 0.9mA Fairchild Power Switch current source flows through the internal resistor ($2.5R+R=3.3K$), V_{fb} becomes approximately 3V. At this time the 2μA current source starts to charge C_{fb} . Because the photo transistor's current is zero, V_{fb} continues to increase. The Fairchild Power Switch shuts down when V_{fb} reaches 7.5V. The shutdown delay time can be easily determined as the time required to increase the C_{fb}

by 4.5V (from 3V to 7.5V) using $2\mu\text{A}$. When C_{fb} is 47nF, delay time is approximately 100ms. The FPS will not shut down within this time. Increasing C_{fb} to get a longer delay time can become a problem, because C_{fb} is an important parameter in determining the SMPS dynamic response time. One method to delay the shutdown time is to add a resistor between the feedback pin and GND and to subtract the amount of the delay current. When the $4.7\text{M}\Omega$ resistor was used experimentally with a C_{fb} of 47nF, shutdown time was almost doubled to 180~200ms. When V_{fb} voltage is 7.5V, the current flowing to the $4.7\text{M}\Omega$ resistor is approximately $1.6\mu\text{A}$.

To obtain the same results, a zener diode (approx. 3.9V) can be series-connected to a capacitor (47nF) which can then be parallel connected to C_{fb} as shown in Figure 2.4.

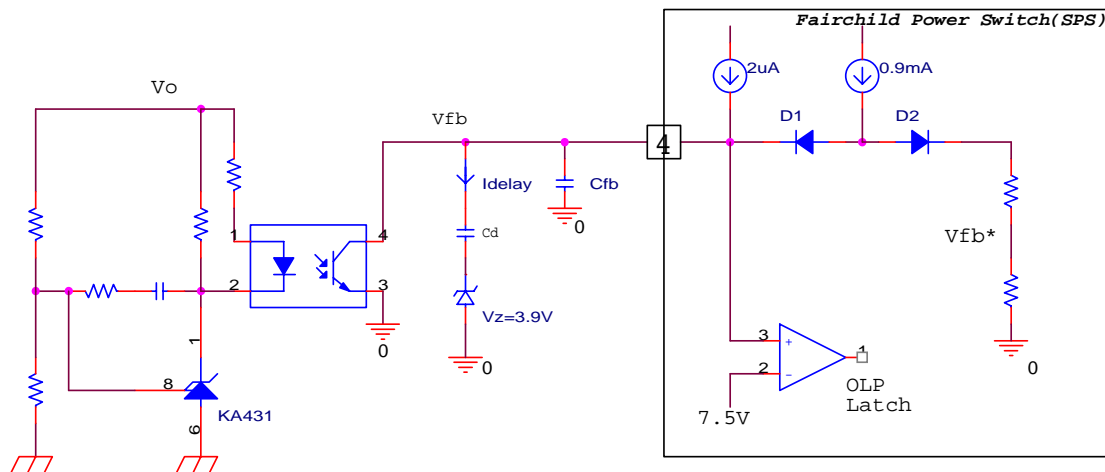


Figure 2-4. Fairchild Power Switch Long Delayed Shutdown

2.3.2 Over Voltage Protection

The Fairchild Power Switch has self protection features that function even when abnormal states occur such as an open or short circuits in the feedback loop.

When the feedback terminal shorts as viewed from the primary side, the feedback terminal voltage becomes zero and prevents switching from starting. If it opens, the protection circuit acts as an over voltage protection circuit. When there is an abnormal state or a possibility of opening due to improper soldering etc. in the secondary side feedback circuit, the primary side continues to switch using the maximum set current until the protection circuit starts to operate. In such instances, it is common for the secondary side voltage to become greater than the rated voltage, which can lead to a fuse blowing or, more seriously, a fire if a protection circuit is not in place. Even if this was not the case, ICs immediately connected to the secondary output without a regulator can be destroyed.

Therefore, Fairchild Power Switch employs the over voltage protection circuit to protect against feedback anomalies.

The Fairchild Power Switch V_{CC} is proportional to the output voltage. When the Fairchild Power Switch V_{CC} exceeds 30V, the over voltage protection feature is triggered. Therefore, V_{CC} must be maintained at less than 30V during normal operation.

2.3.3 Over Current Protection (OCP).

The existing concept of I_{peak} control does not go beyond limiting the amount of current during normal operation.

The OCP block prevents damage to Fairchild Power Switch from abnormal states, such as a diode or a load short. A diode or a load short causes a large current to flow through the SenseFET for a short time. This can be tens of amperes. The leading edge blanking circuit sets the minimum turn on time at 600nS. Tens of amperes for 600nS could destroy the Fairchild Power Switch and so the OCL block senses this instantaneous current and latches like the existing protection circuits.

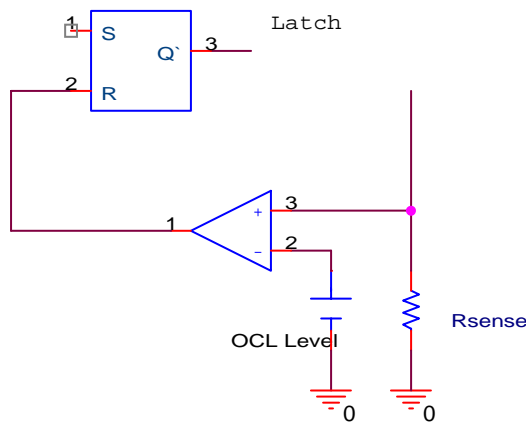
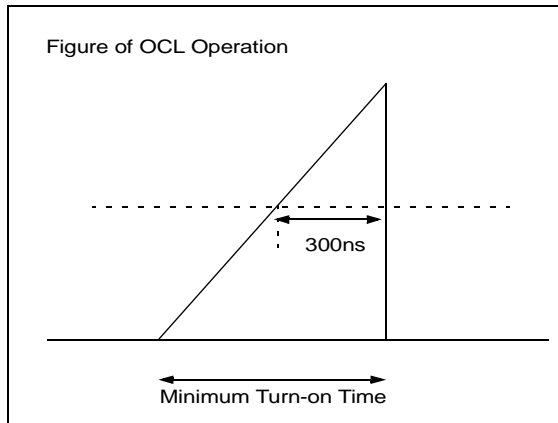


Figure 2-5. Over Current Latch (OCL)

3. External Frequency Synchronization Method

As mentioned, the Fairchild Power Switch operates within a wide frequency range synchronized to the horizontal deflection frequency of a monitor. This section describes the

frequency synchronization method which uses the horizontal deflection frequency delivered to the number 5 pin of the Fairchild Power Switch. Figure 3-1 shows the circuit around the pins. At start up, a ramp is generated on pin 5 by charging C_s with I_{fb} and the current through the $50k\Omega$ resistor. This ramp increases the maximum duty cycle slowly, which results in soft start. After the soft start, V_{cs} remains at 5V and thus the voltage at pin 5 becomes 5V DC plus the external sync input. The sync comparator generates the comparator output waveform (V_{comp}) by comparing the voltage of pin 5 with a sawtooth waveform of 5.8~7.2V as shown in Figure 3-1. The internal timing capacitor, C_t , charges and discharges between 5.8 and 7.2V thresholds. The oscillator output waveform V_{CK} becomes low while C_t charges and high while it discharges. This output signal is sent to the set terminal of the S/R latch.

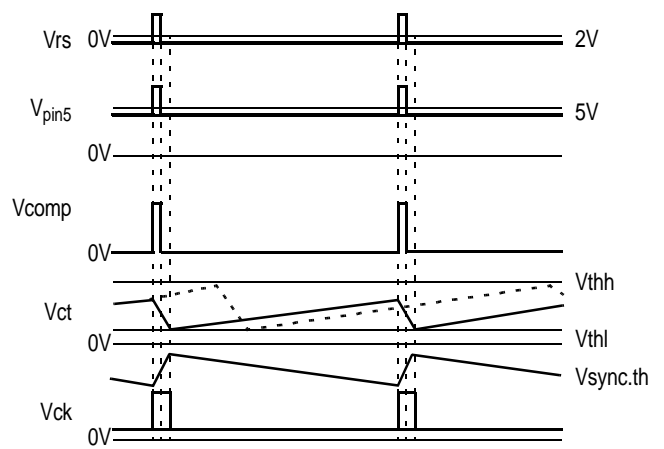


Figure 3-1 Synchronous Operation

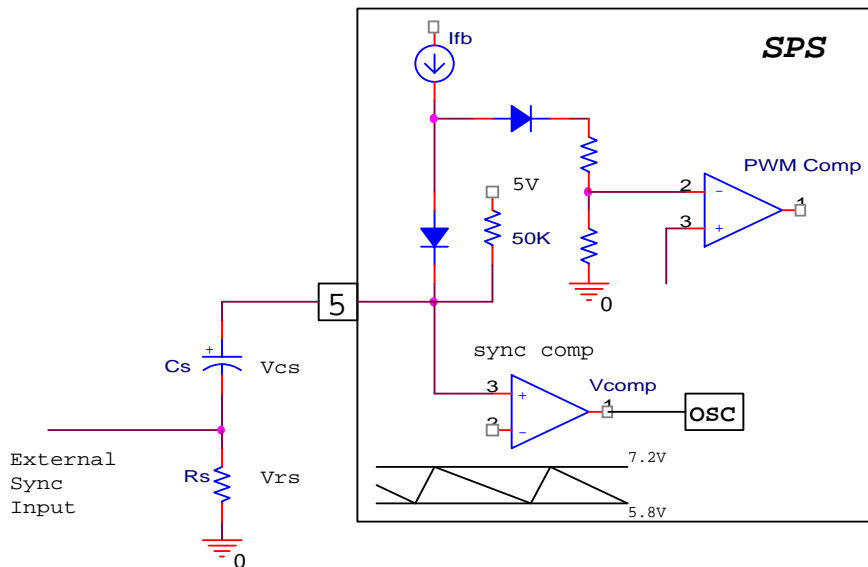


Figure 3-2. Synchronization Circuit

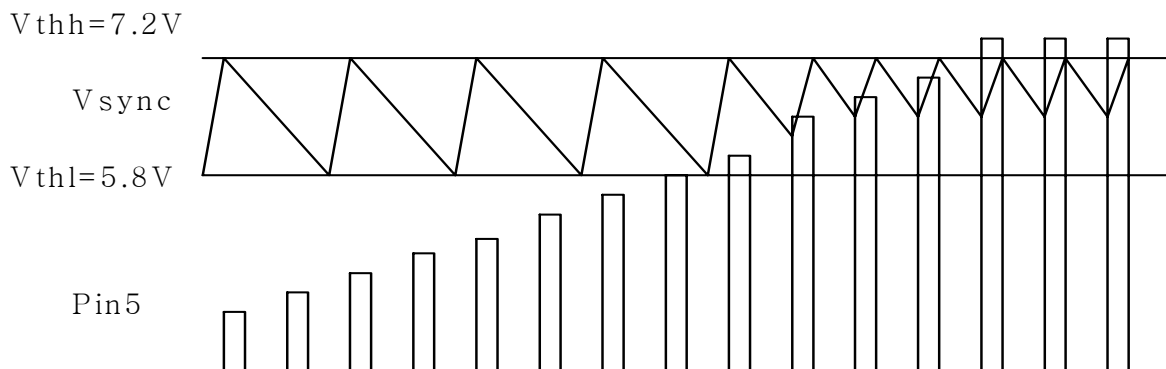


Figure 3-3 Negative Slope Synchronized to Sync Pulses

The inverse slope of the oscillator output becomes the sync comparator reference, V_{sync} , which oscillates between 7.2V and 5.8V with the basic frequency of 25kHz.

Figure 3-2 shows that when the sync signal is applied or V_{sync} reaches the V_{thh} of 7.2V, V_{ct} starts to decrease toward the low threshold voltage V_{thl} . The oscillator output, V_{ck} , outputs a high signal while V_{ct} decreases. As soon as V_{ct} comes down to V_{thl} , V_{ct} starts to increase, V_{ck} drops down, and the SenseFET gate turn on signal is generated. The high duration of V_{ck} is restricted to 5% of one switching period to keep switching noise off screen. If a constant sync comparator reference is used, the SenseFET can be turned on just after being turned off by the first sync signal. In this case the secondary rectifying diode is turned off while it is still conducting.

This causes a high reverse voltage spike between the anode and cathode of the diode due to the long reverse recovery time. In order to solve this problem, FS6S series uses the negative slope as the sync comparator reference. Generally the levels of sync pulses increase gradually to a certain value. If these gradual increasing sync pulses are compared with the negative slope, the first sync pulse that touches the negative slope will be placed in the back area of the basic period of the oscillator as shown in Figure 3-3.

This makes the MOSFET turned off at low or no current levels of the secondary windings of the switching transformer, which can reduce the reverse voltage spike of the rectifying diode significantly. The level of the applied sync signal should be large enough to cross the sync threshold. The level should not exceed 9V for safe frequency synchronization since it is clamped by the 9V voltage source at the sync comparator terminal in the Fairchild Power Switch. Furthermore, the sync signal is added to DC 5V across the soft start capacitor on pin 5.

Therefore, the voltage level should be between 8V and 9V (pure sync signal voltage level is 3 ~ 4V) for safe frequency synchronization.

3.1 Sync Transformer Method

This is the most commonly used method for frequency synchronization in monitor designs and is shown in Figure 3.4. The horizontal sync signal is applied to pin 5 of the Fairchild Power Switch through a transformer.

Delay time is short and thus the switching noise is pushed to the left of the monitor screen, and does not appear in the visible area. One turn from the FBT can also be used instead of the sync.

3.2 Photo-coupler Method

Unlike the sync transformer method, this method shown in Figure 3-5 produces a slight delay time but almost no noise on the screen. The zener diode can compensate the Current Transfer Ratio (CTR) of photo-coupler. Though this method is not frequently used, it has a few advantages for auto-assembly during manufacture.

3.3 Quasi Resonance Method

The resolution on the screen is slightly poor when using the quasi-resonance method shown in Figure 3-6. Switching noise is present on the screen but is not visible since it is not correlated with the picture scan. The Fairchild Power Switch does not depend on the external sync signal but uses the self oscillation frequency which varies with load. However, additional devices, such as the sync transformer or photo-coupler etc., are not required because the Fairchild Power Switch is not synchronized to the sync frequency.

The method is not only highly cost competitive but also advantageous in terms of power loss because it uses zero voltage switching.

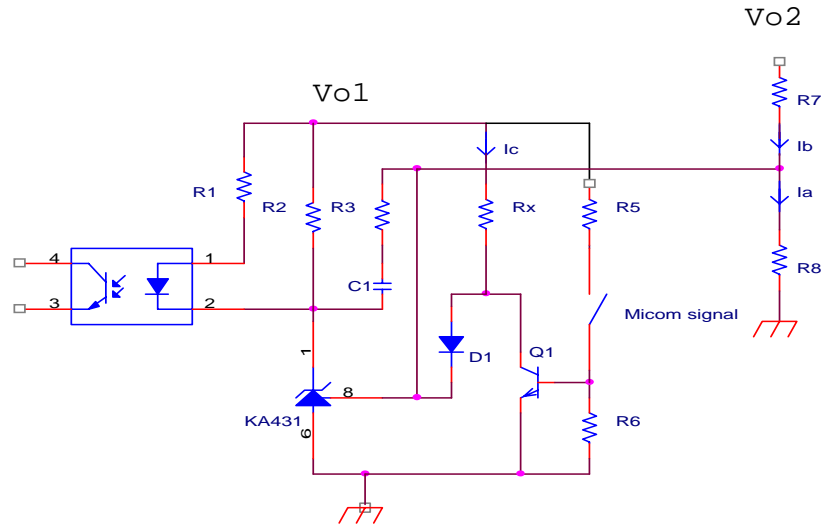


Figure 4-1. Rx Setting Circuit for Burst Mode Operation

4.3. Experimental Results of Burst Mode Operation

4.3.1. V_{CC}/V_{ds} and V_{regin}/V_{regout} waveforms in burst mode.

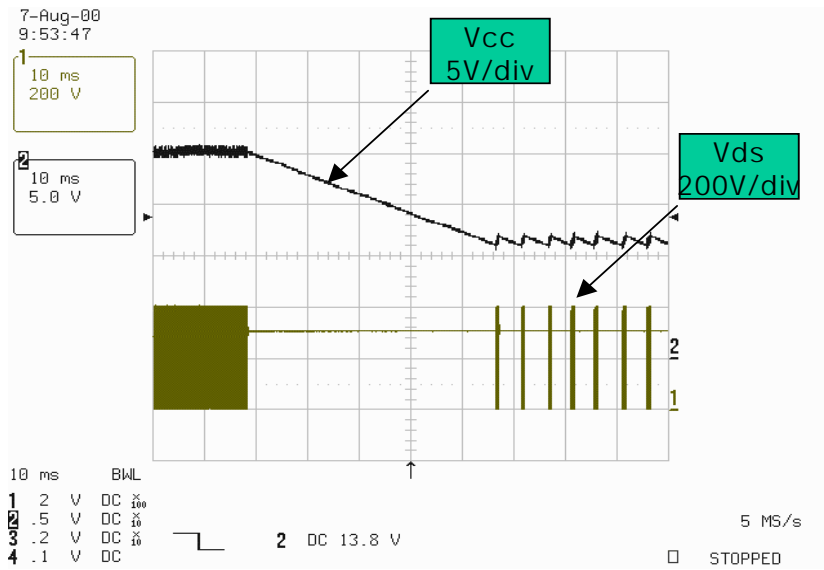


Figure 4-2. V_{CC}/V_{ds} in Burst Mode Operation

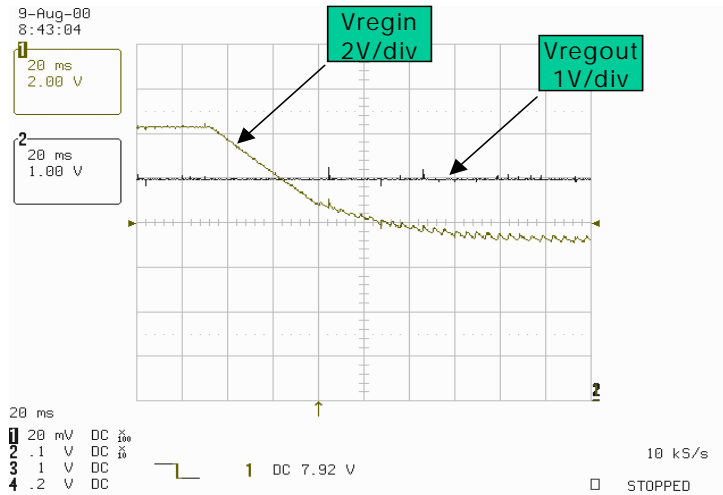


Figure 4-3. Vregin/Vregout Operation in Burst Mode.

Experimental results are shown in, Figure 4-2 and Figure 4-3. With minimum load and normal operation: $V_{ac} = 240V$, $P_{in} = 4.82W$, $V_{CC} = 20V$, $V_o = 190V$ and $V_{regin} = 12.24V$.

When the Fairchild Power Switch operates Burst Mode: $P_{in} = 2.72W$, $V_{CC} = 11\sim 12V$, $V_o = 132V$ and $V_{regin} = 7.07V$

4.5 Circuits for DPMS mode

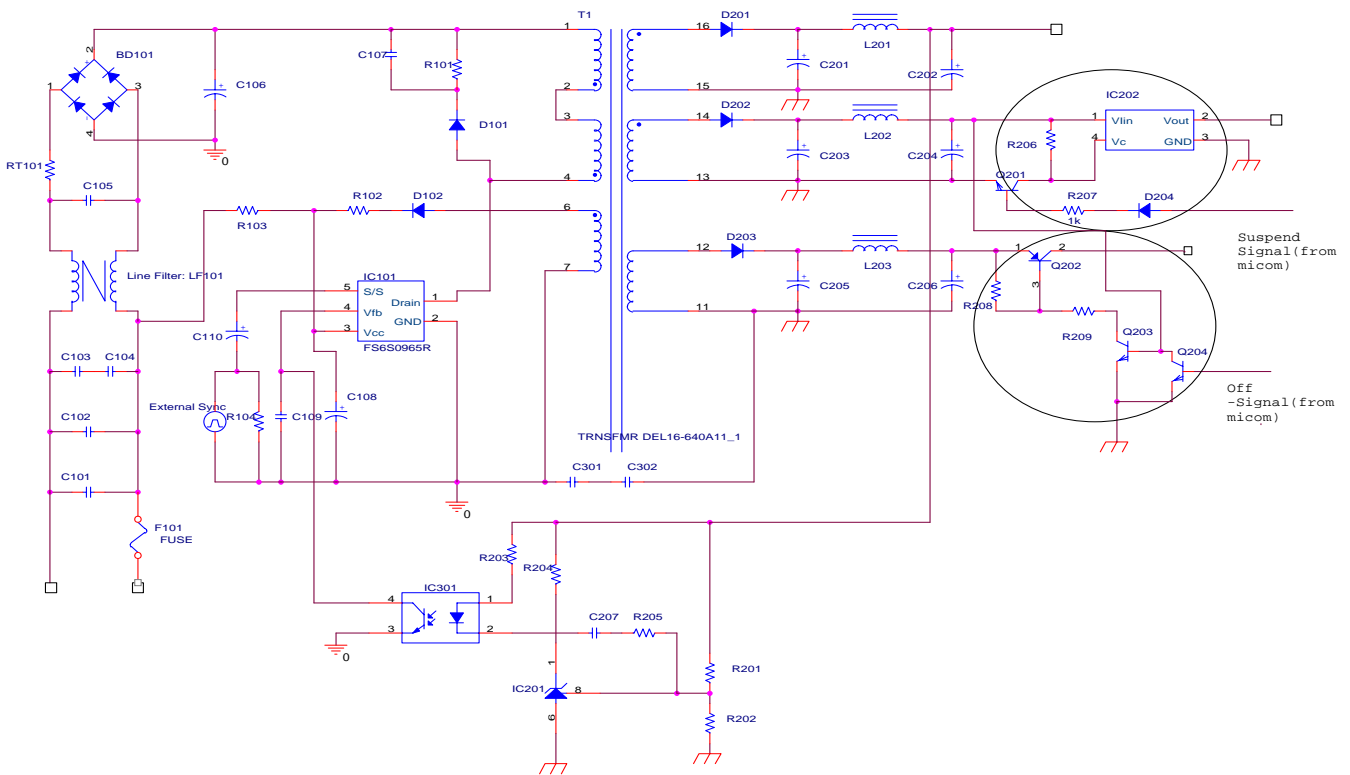


Figure 4-4. Micro Controller Method for Controlling DPMS Mode

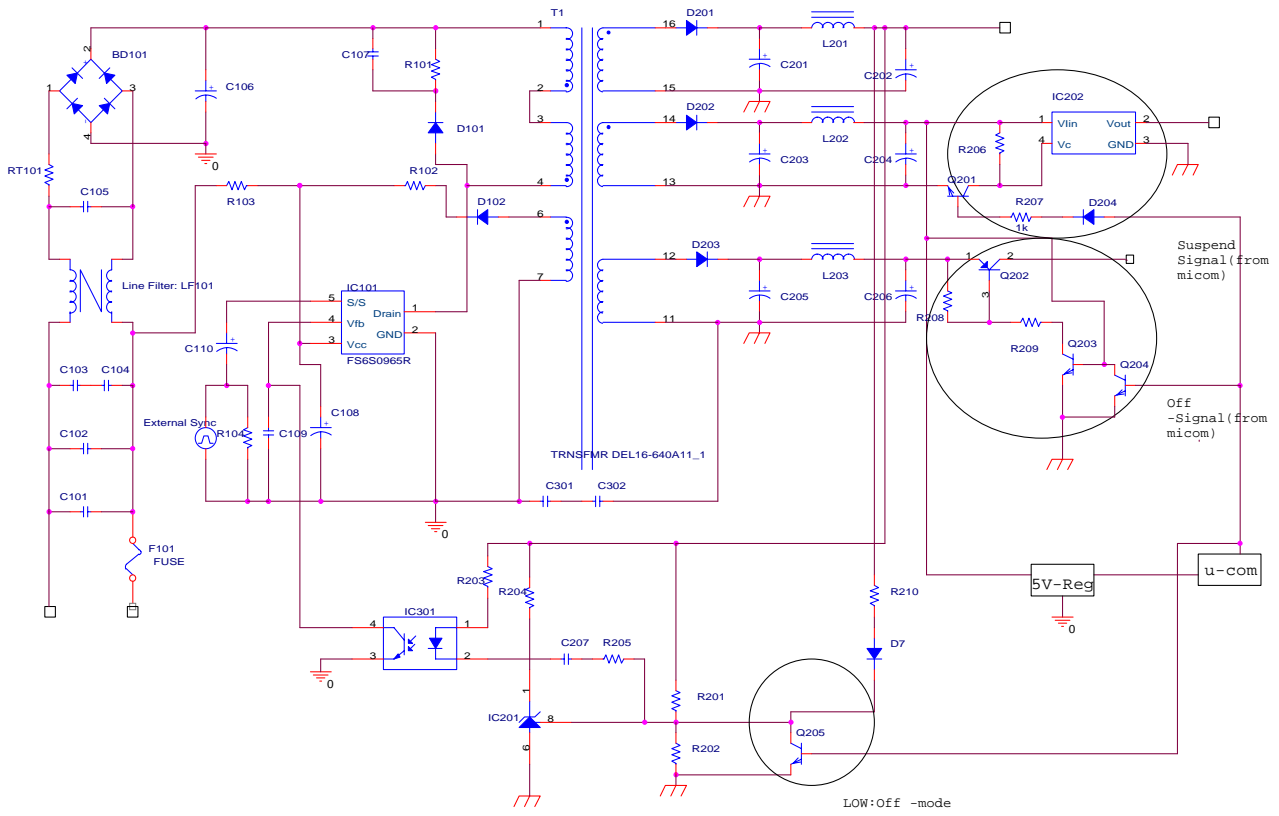


Figure 4-5. Using Burst Mode Operation for DPMS.

5. Monitor Application

5.1 Flyback converter demo circuit

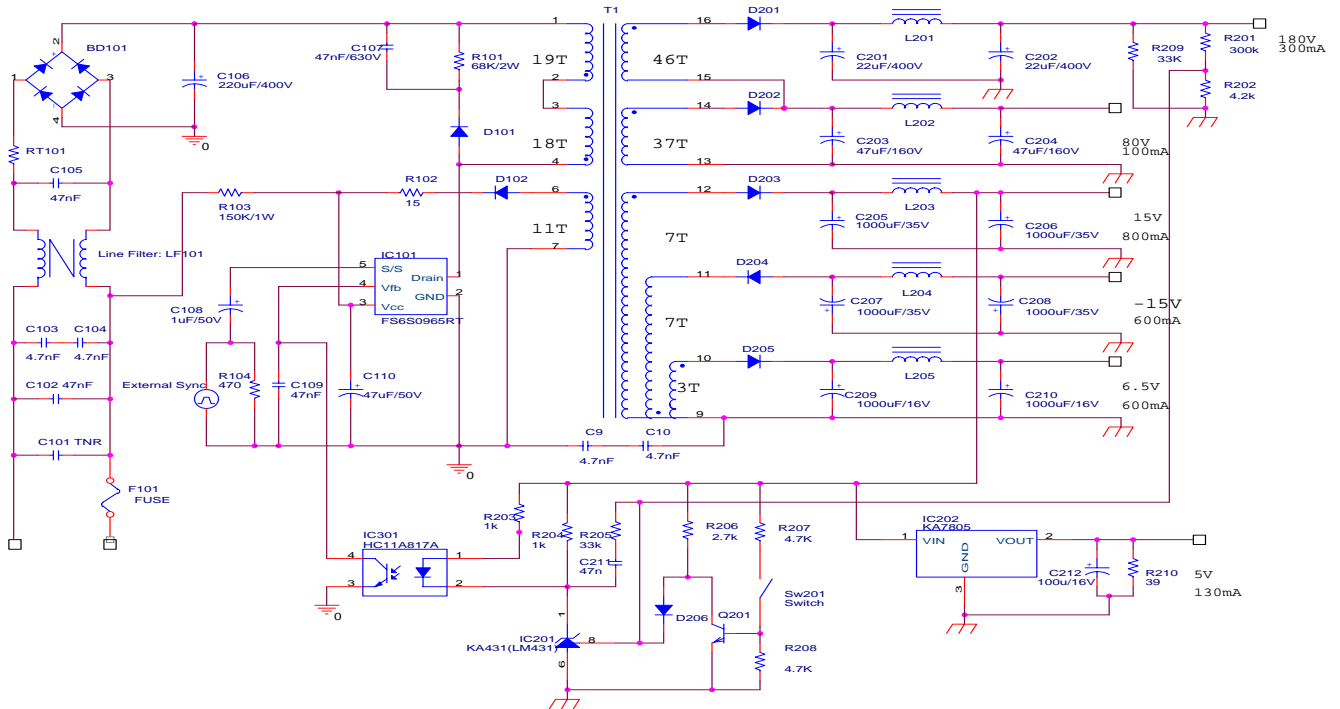


Figure 5.1 Fairchild Power Switch Flyback Converter DEMO BOARD for a Monitor Application

5.2 Part List for Fairchild Power Switch Flyback Converter DEMO BOARD for a Monitor Application

Part Name	Value	Part Name	Value
LF101	BSF-1925	R206	33K, 1/4W
IC101	FS6S0965RCB	R207	2.7K, 1/4W
BD101	KBL407	R208	4.7K, 1/4W
RT101	NTC	R209	4.7K, 1/4W
R101	68K,3W	R210	39, 1/4W
R102	15, 1/4W	C201	22 μ F/400V
R103	150K, 1W	C202	22 μ F/400V
R104	470, 1/4W	C203	47 μ F/160V
C101	TNR	C204	47 μ F/160V
C102	BOX CAP, 47nF	C205	1000 μ F/35V
C103, C104	EMI FILTER CAP, 47nF	C206	1000 μ F/35V
C105	BOX CAP, 47nF	C207	1000 μ F/50V
C106	220 μ F/400V	C208	1000 μ F/50V
C107	47nF/630V	C209	1000 μ F/16V
C108	47 μ F/50V	C210	1000 μ F/16V
C109	47nF/50V	C211	47nF / 50V
C110	1 μ F/50V	C212	100 μ F/16V
D101	UF4007	D201	RG4C
D102	TVR10G	D202	SUF15J
-	-	D203	UG4D
IC201	KA431(LM431)	D204	UF1G
IC202	KA7805/LM7805/MC7805	D205	UG4D
R201	120K, 1/4W	D206	TVR10G
R202	1.8K, 1/4W	-	-
R203	33K, 1/4W	IC301	QT817A
R204	1K, 1/4W	C301	4.7nF/2KV
R205	1K, 1/4W	C302	4.7nF/2KV

Parts in Boldface are available from Fairchild Semiconductor.

5.3 Transformer Specification

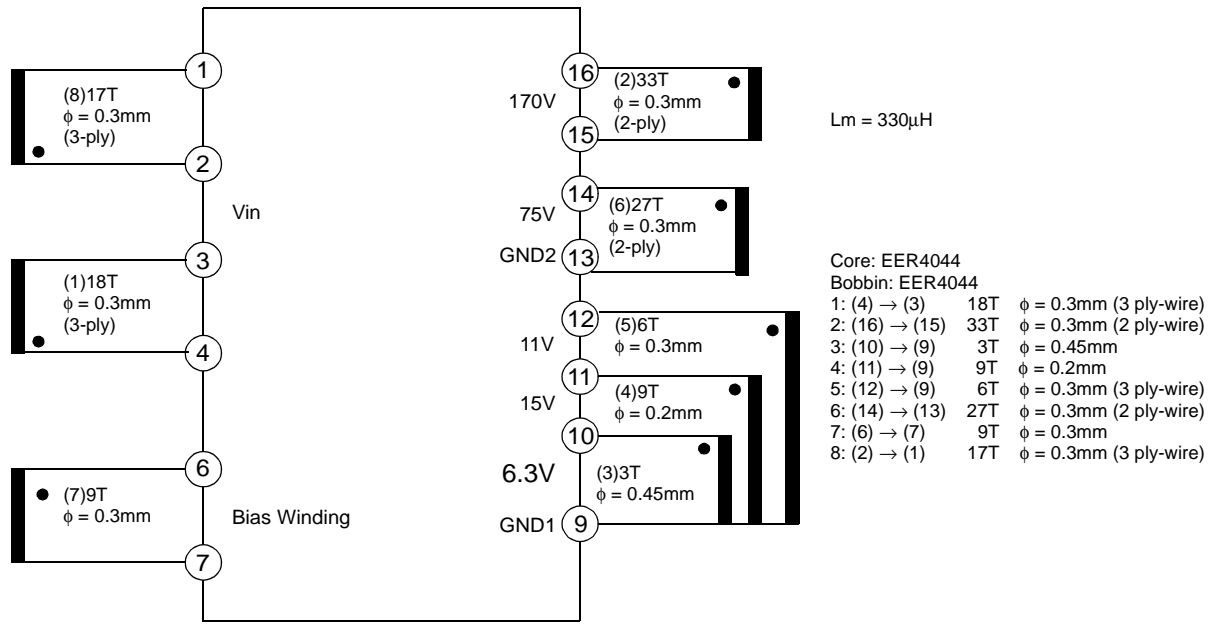


Figure 5-2 FS6S0965RCB Transformer Specification for a 95W Monitor Application.

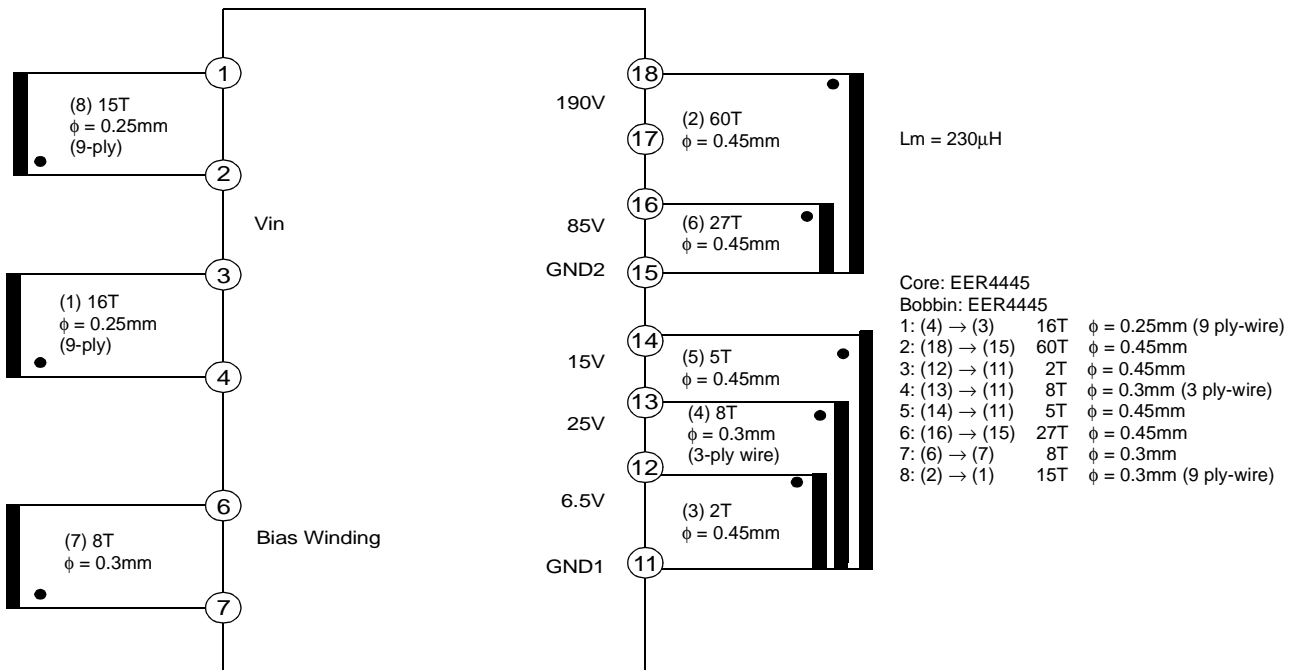


Figure 5-3. FS6S0965RCB Transformer Specification for a 120W Monitor Application.

- FS6SXX65R Comparison Table of Electrical Characteristics -

Content	FS6S-series			KA5S-series			KA2S-series			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Start-up Current	-	100	170	-	100	170	100	300	550	μA
Operating Current	-	10	15	-	7	12	6	12	18	mA
Initial Frequency	22	25	28	18	20	22	18	20	22	kHz
Burst Mode Frequency	40	50	60	-	-	-	-	-	-	kHz
Over Current Protection	0.9	1.0	1.1	-	1.1	-	-	-	-	V
Burst Mode Ipeak	0.6	0.85	1.1	-	-	-	-	-	-	A
Burst Mode Range	11.0	-	12.0	-	-	-	-	-	-	V
Over Voltage Protection	27	30	33	23	25	28	23	25	28	V
Shutdown Delay Current	1.6	2.4	2.4	3.0	4.0	5.0	1.4	1.8	2.2	μA

Table 3. FS6S-Series Comparison with Previous KA5S and KA2S - Series

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.