

Application Note 42032

FAN4822 Power Factor Correction With Zero Voltage Resonant Switching

Introduction

The boost converter is a popular topology for improved power factor and reduced line harmonics, as specified in IEC 555-2 and other more recent standards. With this solution limitations inherent in the continuous conduction mode (CCM) boost converter topology have been recognized. As with all power converters, limitations on operating frequency are always of interest. Higher operating frequencies allow for smaller filter components both at the output and input filter. This reduces cost and increases packaging density. The fundamental limitations on the operating frequency of the CCM boost converter are the reverse recovery current associated with the boost diode and the switching losses associated with the FET output capacitance. At frequencies above 100kHz these losses become excessive.

A typical method for reducing reverse recovery currents is the addition of L2 in series with the main switching transistor (see Figure 1). Inductor L2 requires an equivalent volt-seconds during the off time for proper reset. This method requires a tapped boost inductor to provide the extra voltage

required for reset. Also, L2 must carry the same current seen by the main FET. Although this method does provide significantly reduced reverse recovery currents it does not eliminate the switching losses associated with the capacitance at the drain node being discharged by the FET.

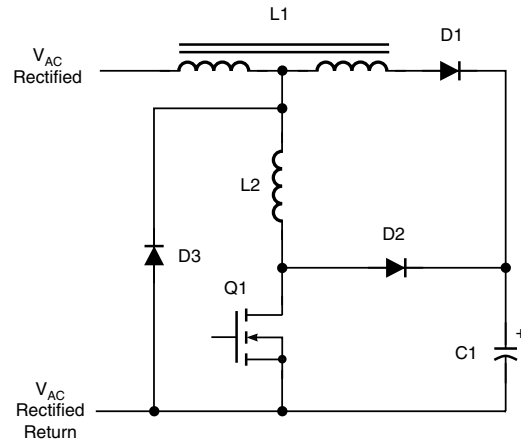


Figure 1. Tapped Boost

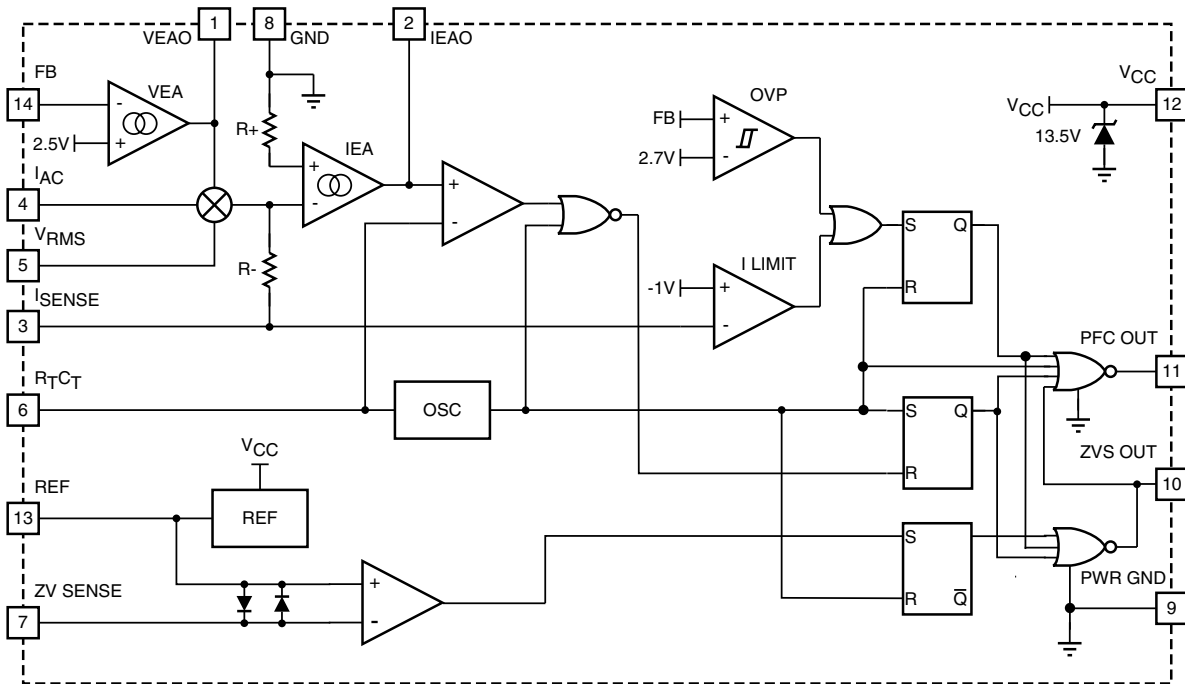


Figure 2. Block Diagram

This paper presents a zero voltage switching technique that eliminates the diode recovery problem and significantly reduces FET switching losses using Fairchild Semiconductor's FAN4822 ZVS power factor control IC. The method allows operation at higher frequencies with greater efficiency and reduced EMI.

FAN4822 Boost ZVS Integrated Circuit

The FAN4822 is a standard power factor controller IC that provides an additional gate drive output necessary to implement ZVS. The PFC section of the IC is identical to the PFC section of the ML4824. A ZVS gate drive output with sensing circuitry provides the ZVS capability.

The ZVS circuitry consists of an additional switching FET, resonant inductor and capacitor, and a clamping diode necessary for resetting the resonant inductor (see Figure 4).

The RMS current seen by the ZVS Q is small. An ultra low Rds on FET is not necessary, but the capacitance of the ZVS Q is important. A device with reduced capacitance (higher Rds on) will reduce switching losses.

FAN4822 ZVS Switching Theory and Operation

The ZVS gate drive precedes the PFC switch Q gate drive output. The duration of the ZVS output is the time necessary for a controlled turn off of the boost diode plus the time required for the main FET drain voltage to resonate to zero. The ZVS sense input determines the duration of the ZVS pulse. Once the main FET resonates to zero the ZVS pulse is terminated. The PFC output follows the ZVS pulse. Figure 3 shows the operation of the ZVS circuitry throughout a switching cycle.

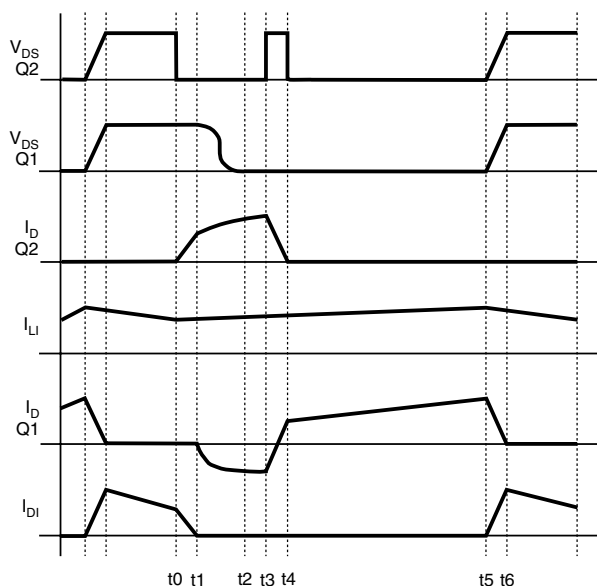


Figure 3. ZVS Timing Diagram

t0–t1

At the beginning of each switching cycle the ZVS transistor (Q1) turns on and the current in the inductor L2 builds up until it is equal to the main inductor (L1) current. At this point the D1 diode current has decayed to zero.

t1–t2

The effective circuit during this interval consists of a parallel resonant LC circuit where the C is the C_{OSS} of Q1 and whatever parallel capacitance is present. L is the resonant inductor, L2. Energy is transferred from the capacitor to L2 until the voltage has collapsed to zero (complete transfer of energy from the capacitance to L2). Q1 is gated on once the voltage has collapsed to zero at its drain. When turning on in this manner, the main Q no longer must discharge the drain node capacitance. This further reduces its turn-on switching losses. At 250 kHz with a capacitance of 500pF this would amount to a loss of 10W. This does not include the additional turn-on losses caused by the reverse recovery current of the main rectifier.

$$t_{12} = \frac{\pi}{2} \sqrt{L_{ZVS} C_{ZVS}}$$

t2–t3

Using the method shown in Figure 10 Q2 will remain on until the ZVS sensing circuitry senses roughly zero VDC on the drain of Q1.

Another method is to leave Q2 on for a predetermined amount of time. This time is the worst case time expected for this whole process to happen. The total time necessary should include the time necessary for L2 to build up to the L1 current, turn off CR1 and transfer C_{OSS} energy to inductor L2. The penalty for not sensing Q1 voltage and turning off Q2 instantly is increased losses in Q2.

What happens if Q2 remains on after this process has completed? The natural tendency is for the inductor to try to transfer this energy back into the capacitor (resonate) to a potential of opposite polarity. The inductor will attempt this unsuccessfully due the body diode of Q1. The resonant inductor is clamped at both ends and stays charged until Q2 turns off. Since the total voltage across the inductor is very small there will be very little change in current. Hence L1 stays charged during this part of the cycle. In summary, Q1 and Q2 are on during this time, clamping L2 at the energy level reached at time t2.

t3–t4

Once Q2 turns off, L1 will reset itself by transferring its stored energy to the output through D2. Since the Voltage across L2 is the output voltage, the time necessary to reset L2 should be approximately equal to the on time of Q2 (see Figure 13).

Once L2 has reset through D2 its current will have decayed to zero. As this current decays through zero it will continue to flow from the cathode to the anode of D2. This will turn off D2 in a benign fashion, but unfortunately will store energy in L2. Once D2 turns off the stored energy will resonate against the parasitic capacitance at the anode of D2. D4 and R1 serve to dampen that resonance. Also, a saturable reactor in series with L2 (L3) helps to limit the amount of energy stored in L2 as D2 recovers. Since the saturable reactor has a large swing in flux density, keeping the core cool will be a concern.

t5–t6

This interval is identical to the conventional boost. At this point Q1 turns off and the drain voltage rises with the wave-shape of a constant current source feeding a capacitor. The current source is the boost inductor and the capacitance is the total capacitance seen at the drain node of Q1. The ZVS capacitor will help to limit the dv/dt of Q1 if necessary.

Design Specifications

Output Power	500 W
Line Voltage	85 VAC to 265 VAC
Frequency	250 kHz
Efficiency	>95%

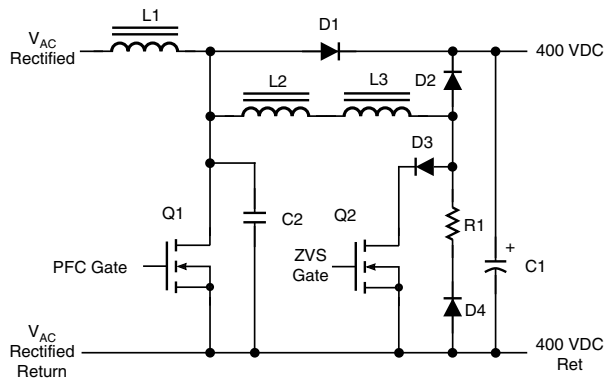


Figure 4. ZVS Power Stage

Power Stage Design

Inductor

The boost inductor value should give a ripple current that is 10% to 20% of the peak current. This not only provides continuous conduction, but also provides sufficient ramp slope to trip the over current comparator at the trailing edge of the on pulse.

$$I_{pk} = \frac{P_{out} \sqrt{2}}{V_{MINac}} = \frac{500 \cdot \sqrt{2}}{85} = 8.3A$$

$$D = \frac{V_{out} - V_{in}}{V_{out}} = \frac{400 - 85 \cdot \sqrt{2}}{400} = 0.7$$

$$L = \frac{V_{in}}{\Delta I_{pp}} \cdot D \cdot T_s = \frac{85 \cdot \sqrt{2}}{2} \cdot 0.7 \cdot 4 \mu \text{ sec} = 168 \mu H$$

Capacitor

In the selection of the output capacitor the main concerns are hold up time, and 120 Hz ripple voltage. The 120 Hz ripple on the output capacitor is a source of 3rd harmonic distortion. It is fed back through the voltage error amplifier and attenuated there so as to limit the 120 Hz ripple component, limiting the 3rd harmonic distortion it can generate.

$$V_{holdup} = V_{out} - \sqrt{\frac{2 \cdot P \cdot t_{holdup}}{C}} = 400 - \sqrt{\frac{2 \cdot 500 \cdot 20 \text{ msec}}{330 \mu F}} = 289 \text{ V}$$

Output capacitor ripple summary:

$$I_{in}(t) = I_{pk} \cdot \sin(2\pi ft)$$

$$V_{in}(t) = V_{pk} \cdot \sin(2\pi ft)$$

$$P_{in}(t) = V_{in}(t) \cdot I_{in}(t)$$

$$I_{out}(t) = \frac{P_{in}(t)}{V_{out}} = I_{pk} \frac{V_{pk}}{V_{out}} \cdot (1 - \cos(2\pi \cdot 2ft)) = 8.3 \frac{120}{400} (1 - \cos(2\pi \cdot 2ft))$$

$$I_{outavg}(t) = \frac{P_{out}}{V_{out}} = 1.25A$$

$$I_{cap}(t) = I_{out}(t) - I_{outavg} = 2.49(1 - \cos(2\pi \cdot 2ft)) - 1.25$$

$$V_{capripple}(t) = \frac{I_{cap}(t)}{2\pi \cdot 2f \cdot C}$$

$$V_{pp} = 2 \cdot |V_{capripple}(0)| = 10.6V$$

Boost Transistor

Solving for the duty and peak current as a function of input voltage phase angle, one can estimate the on losses. Averaging this over the complete cycle results in 5.8W for an R_{dson} of 150mΩ. The calculation uses 1.5 times the 25 C R_{dson} in order to account for the temperature coefficient.

$$D(\theta) = \frac{V_o - V_{in} \sin(\theta)}{V_o}$$

$$I_{pk}(\theta) = \frac{2P_{out}}{V_{in}} \sin(\theta)$$

$$I_{pkRMS}(\theta) = I_{pk}(\theta) \sqrt{D(\theta)}$$

$$P_{on}(\theta) = I_{pkRMS}^2(\theta) \cdot R_{dson}$$

$$P_{avg} = \frac{1}{\pi} \int_0^{\pi} P_{on}(\theta) d\theta$$

Boost Diode

Estimate the boost diode current by averaging the peak over 1/2 of a line cycle. The peak diode current is 8.3A.

$$I_d(\theta) = I_{pk}(\theta) \cdot (1 - D(\theta))$$

$$I_{davg} = \frac{1}{\pi} \int_0^{\pi} I_d(\theta) d\theta = 1.3A$$

For simplicity the boost and diode calculations above assume CCM throughout the line cycle. In reality the converter will go into discontinuous conduction mode (DCM) at the valleys of the line. The equation for duty cycle does not apply for DCM.

ZVS Component Selection

Resonant Inductor

By minimizing the ZVS on time, the ZVS inductor reset time is minimized. This minimizes the output voltage required for proper reset of the ZVS inductor. Likewise the ZVS cycle should be long enough such that the peak currents stay within acceptable levels.

The first portion of the ZVS cycle is the time required for L2 to build up to the current in L1. Excluding ripple current, Equation 1 describes the peak current. Since the ZVS inductor is on during the downslope of the boost inductor current, the actual peak current seen by L2 during this portion of the ZVS cycle is less. Equation 2 shows the time required for L2 to build up to this current.

The value chosen for L2 is flexible and limited by the acceptable limit in the dv/dt of the main switch Q. The smaller the inductor the lower the losses experienced in Q2.

The value chosen for L2 in this design was 8.5 μ H. This gives a time of 160ns for t1 at maximum input power and minimum line voltage.

$$I_{pk} = \frac{P_{out} \sqrt{2}}{V_{RMS}} = \frac{500 \cdot \sqrt{2}}{85} = 8.32A \quad (1)$$

$$t_1 = \frac{L_2 I_{pk}}{V_{out}}$$

Substituting for Ipk –

$$L_2 = \frac{t_1 \cdot V_{out} \cdot V_{RMS}}{P_{out} \cdot \sqrt{2}} \quad (2)$$

$$t_1 = \frac{L_2 P_{out} \sqrt{2}}{V_{out} V_{RMS}} = \frac{8.5 \times 10^{-6} \cdot 500 \cdot \sqrt{2}}{400 \cdot 85} = 177ns$$

Resonant Capacitor

The ZVS resonant capacitor should sufficiently limit the dv/dt at turn off yet not significantly affect the minimum duty cycle.

Setting t12 roughly equal to t1 requires a value of 1000 pF for C_{ZVS}. This means setting the time required for L2 to ramp up to L1 current equal to 1/4 of the resonant frequency period. C_{ZVS} includes C_{OSS} of the main FET.

$$f_{res} = \frac{1}{2\pi \sqrt{L_{zvs} C_{zvs}}}$$

$$t_{12} = \frac{t_{res}}{4}$$

$$C_{zvs} = \frac{\left(t_{12} \cdot \frac{2}{\pi}\right)^2}{L_2}$$

$$t_{12} = \frac{\pi}{2} \sqrt{L_{zvs} C_{zvs}} = \frac{3.14}{2} \cdot \sqrt{8.5 \times 10^{-6} \cdot 1000 \times 10^{-12}}$$

$$= 144ns$$

If the dv/dt of the drain voltage at turn off is not of concern, C_{OSS} of the main switch should suffice as the resonant capacitor. This helps to reduce the time required to resonate to zero VDC on the drain. It will also reduce the peak current seen by Q2 and L2. It is interesting to note that the capacitance at this node can be increased with little penalty in efficiency. This is not the case in a standard boost configuration especially at 250kHz. This gives some freedom to limit the dv/dt on the main switching without significantly increasing losses. The penalty one does pay in increasing C2 is an increase in the time required to reset L2. This puts a limit on the minimum on time allowed for Q1. The greater the capacitance, the larger the minimum on time. This is a concern at the high line condition where the on time can approach zero. Putting a limit on the on time requires the output voltage to be set higher than would be required in a standard boost.

ZVS Switch

The losses in the ZVS switch (Q2) consist of both switching and Rdson losses. Figure 13 displays the magnitude of the current throughout the ZVS cycle at 500W and 120VDC input with no external capacitance added.

Initially the current ramps up to roughly 4A and then resonates to close to 8A.

Since the resonant inductor limits the turn on current through the ZVS switch, the turn on losses are dominated by the discharge of the C_{OSS} through its own Rdson.

Calculate the on losses by estimating the RMS of the current during the first two portions of the resonant cycle.

Neglecting the ripple current, the peak current during the first portion of the cycle can be used to derive an RMS value.

$$I_{pk} = \frac{P_{out} \sqrt{2}}{V_{RMS}} = \frac{500 \cdot \sqrt{2}}{85} = 8.32A$$

The RMS of this portion of the waveform can be calculated if a triangle waveform for this portion of the waveform is assumed.

$$I_{rms1} = I_{pk} \sqrt{\frac{t_1}{3T_s}} = 8.32 \cdot \sqrt{\frac{177ns}{3 \cdot 4\mu s}} = 1.01A$$

Since we have not included the ripple current this is a conservative estimate.

Using Equation 3 we can solve for I2 and then calculate the RMS of the second portion of the waveform. This equation represents the transfer of energy from the resonant capacitor to the inductor.

$$\begin{aligned} \frac{1}{2} L_{zvs} (I_2^2 - I_{pk}^2) &= \frac{1}{2} C_{zvs} V_{out}^2 \\ I_2 &= \sqrt{I_{pk}^2 + \frac{C_{zvs} \cdot V_{out}^2}{L_{zvs}}} \\ &= \sqrt{8.3^2 + \frac{1000 \times 10^{-12} \cdot 400^2}{8.5 \times 10^{-6}}} = 9.37A \end{aligned} \quad (3)$$

Equation 4 describes the current during the second portion of the ZVS cycle. Taking the RMS over one quarter of a cycle for this waveform we get 1.7A.

$$\begin{aligned} I_{12}(t) &= I_{pk} + (I_2 - I_{pk}) \cdot \sin\left(\frac{t}{\sqrt{L_{zvs} \cdot C_{zvs}}}\right) \\ I_{RMS12} &= 1.7A \end{aligned} \quad (4)$$

Combining the two RMS values we can estimate the total RMS current during the on time.

$$I_{rms_{total}} = \sqrt{I_{rms12}^2 + I_{rms1}^2} = 1.99A$$

Using a FET with an R_{dson} of 1.5Ω the worst case R_{dson} will be less than 2.25Ω resulting in 9W on losses. This loss assumes a peak power at the peak of the low line (85VAC) condition. In reality the input is a rectified sinusoid, thus the envelope of the peak inductor current will be a rectified sinusoid also. Therefore the actual I_{RMS} of the ZVS Q will be less.

Assuming a C_{OSS} of 160 pF results in an additional 1.6W loss giving roughly 10.6W in a 1.5Ω TO-220 package at 250kHz. Turn off switching losses will also be a significant factor at this switching frequency.

Care must be taken in the selection of the ZVS transistor. A low R_{dson} FET results in excessive switching losses. A high R_{dson} FET will have significantly less switching losses with excessive on losses. An IRF830 provides the best balance between R_{dson} losses and switching losses at 500W and 250kHz.

ZVS Clamp Diode Conduction

The current seen by the ZVS clamp diode (D2) is the peak current in the inductor as it ramps to zero, resetting itself.

Equation 5 shows the average current seen by the diode.

$$\begin{aligned} t_{reset} &= \frac{L_{zvs}}{V_{out}} I_2 = 200ns \\ I_{avg} &= \frac{I_2}{2} \cdot \frac{t_{reset}}{T_s} = 0.5A \end{aligned} \quad (5)$$

For a forward voltage of 1 Volt this amounts to 0.5W dissipation. The diode switching losses must also be considered.

Saturable Reactor and Series Blocking Diode

After the ZVS inductor is reset energy will be transferred to the ZVS inductor as diode D2 turns off. Saturable reactor L3 limits this energy by introducing a high impedance. This high impedance limits the amount of current drawn from D2 as it turns off. Without limiting this current, excess energy will be stored in the ZVS inductor (L2). This energy will have to be dissipated so as to limit the high frequency ringing and protect D2 from excessive voltage.

Given the large flux density swing and frequency of operation, L3 will require some form of heatsinking to maintain its permeability.

Diode D3 also helps to limit the amount of energy transferred to the ZVS inductor. It prevents energy stored in the output capacitance of Q2 from being transferred to the ZVS inductor after it has reset.

ZVS Damping Network

The values required for the damping network can be determined by first examining the undamped waveform seen at the drain of the ZVS transistor. By examining the frequency of this waveform the parasitic capacitance can be calculated.

$$C_p = \frac{1}{(2\pi f_{osc})^2 L_{zvs}}$$

Then the characteristic impedance of this network can be determined.

$$R_o = \sqrt{\frac{L_{zvs}}{C_p}}$$

Setting the damping resistor equal to the characteristic impedance results in a Q of 1.

ZVS Gate Drive

The ZVS gate drive output has a 0.5A peak current capable of directly driving the ZVS Q gate at frequencies up to 500kHz.

The Main Q peak drive current is also 0.5A and requires an additional driver for high frequency operation. The gate charge required for turn on of the main Q can be as much as three times that of the ZVS Q, therefore a 0.5A peak current capability will typically not be sufficient for the main Q drive. In this particular application two 1.5A peak drivers were paralleled.

Minimum Duty Cycle

In order to ensure proper reset of the ZVS inductor there is a minimum output voltage requirement.

The volt-second balance of the main inductor shows that during the t₁ portion of the cycle, the main inductor is still clamped to the output, just as it is during the off time. Therefore the minimum on time can be estimated as the time required for the ZVS inductor current to ramp to zero. Performing a volt-second balance with these assumptions gives the minimum voltage requirement (neglecting drain rise and fall times and assuming continuous conduction mode).

As a quick estimate of what the minimum output voltage will be, assume t_{reset} is 200ns.

$$V_{\text{outmin}} = \frac{V_{\text{RMSmax}} \sqrt{2}}{1 - D_{\text{min}}} = \frac{V_{\text{RMSmax}} \sqrt{2}}{1 - \frac{t_{\text{reset}}}{T_s}} = \frac{265 \cdot \sqrt{2}}{1 - \frac{200 \times 10^{-9}}{4 \times 10^{-6}}} = 394\text{V}$$

Control Circuit Design

Multiplier Setup

Since the maximum current demand is at low line the multiplier is set up to provide the maximum output current at the low line condition. V_{RMS} (pin 5) programs the multiplier gain. A voltage of 1.2VDC will program the multiplier for maximum gain (Figure 5). The network feeding this voltage from the rectified AC input should be set up to provide 1.2 VDC at the low line point.

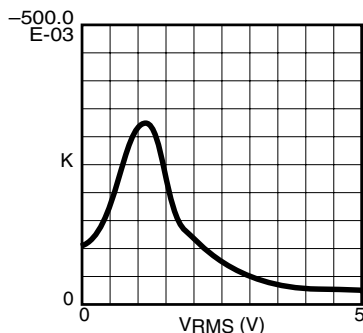


Figure 5. Multiplier Gain vs. V_{RMS}

Given 1.2V at pin 5 and the maximum voltage error amplifier output voltage, I_{AC} (pin 4) is set up to demand the maximum multiplier current at the peak of the line.

$$\frac{R_{15}}{R_{15} + R_{14} + R_{12}} \sqrt{2} V_{\text{ac}} \frac{2}{\pi} = 1.22\text{V}$$

$$\text{max} I_{\text{mult}} = 200\mu\text{A}$$

$$k_m = 0.328\text{V}^{-1}$$

$$I_{\text{AC}} = \frac{200\mu\text{A}}{k_m (V_{\text{EAO}} - 1.5\text{V})} = \frac{200 \times 10^{-6}}{0.326 \cdot (6.7 - 1.5)} = 118\mu\text{A}$$

$$R_{13} \frac{\sqrt{2} V_{\text{AC}}}{I_{\text{AC}}} = \frac{\sqrt{2} \cdot 85}{118 \times 10^{-6}} = 1\text{M}\Omega$$

Current Sense Resistor

With a maximum multiplier current of 200 μA and termination resistors of 3500Ω the maximum sense voltage is 0.7VDC. Maximum output power and maximum R_{sense} can be calculated using the maximum sense voltage.

$$R_{\text{sense}} \leq \frac{\text{max} V_{\text{sense}}}{\sqrt{2} \frac{P_{\text{out}}}{V_{\text{AC}}}} = \frac{0.7}{\sqrt{2} \frac{500}{85}} = 0.084\Omega$$

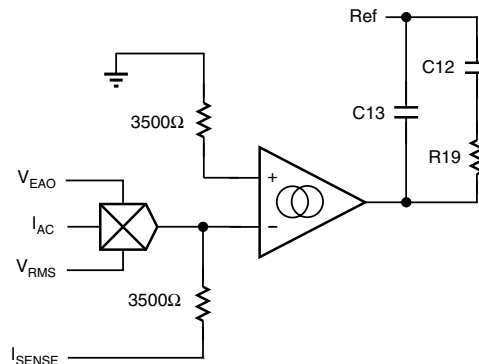


Figure 6. Current Error Amplifier with Multiplier

Current Loop

There are a number of issues when considering the crossover frequency of the current loop. Typically a crossover frequency of 1/6 of the switching frequency is achievable. Since the 60 Hz rectified waveform contains no significant harmonics above 10 kHz, anything above 10 kHz would provide the performance required. At the same time a crossover too high will result in too much switching frequency signal at the output of the current error amplifier. The peak-to-peak input signal to the current error amplifier at the switching frequency is equal to the downslope current of the main inductor times the sense resistance. Limiting this to one-tenth of the sawtooth amplitude will limit the crossover frequency to 18.5 kHz, well above the 10 kHz goal. In Equation 6 k_{error} is the gain required to limit the switching frequency signal to one-tenth of the sawtooth amplitude.

$$k_{\text{error}} = \frac{V_{\text{ramp}}}{10} \frac{1}{I_{\text{Lpp}} R_{\text{sense}}} = \frac{25}{10} \frac{1}{2 \cdot 0.073} = 1.712 \frac{\text{V}}{\text{V}} \quad (6)$$

$$G_{\text{pwr}}(f) = \frac{V_{\text{out}} R_{\text{sense}}}{2\pi f L V_{\text{ramp}}}$$

The crossover frequency can be calculated from Equation 7, assuming the error amplifier gain is flat in this region.

$$f_{\text{ci}} = \frac{V_{\text{out}} R_{\text{sense}} k_{\text{error}}}{2\pi L V_{\text{ramp}}} \quad (7)$$

$$f_{\text{ci}} = 18.5 \text{ kHz}$$

Multiplying the error amp transconductance times the impedance seen at the output near crossover frequency gives the error amp gain. Solving for R_g is the first step in the procedure. Figure 7 details the current amplifier gain vs. V_{in} .

$$g_m = 181 \times 10^{-6} \cdot \frac{\text{Amp}}{\text{Volt}}$$

$$R_{19} = \frac{k_{\text{error}}}{g_m} = \frac{1.712}{181 \times 10^{-6}} = 9.46 \text{ k}\Omega$$

Use 10 k Ω .

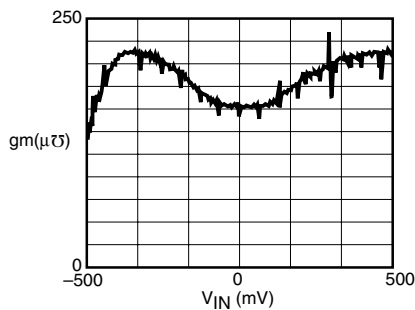


Figure 7. Current Error Amplifier Gain vs. V_{in}

Setting the lead zero at 1/3 of the crossover frequency gives more than 60 degrees of phase margin at the crossover frequency.

$$C_{12} = \frac{1}{R_g 2\pi \frac{f_{\text{ci}}}{3}} = \frac{1}{10 \times 10^3 \cdot 2\pi \frac{18.5 \times 10^3}{3}} = 27 \text{ nF}$$

A pole is also placed at 10 times the crossover frequency to reject high frequency noise.

$$C_{13} = \frac{1}{R_g 2\pi f_{\text{ci}} 10} = \frac{1}{10 \times 10^3 \cdot 2\pi \cdot 18.5 \times 10^3 \cdot 10} = 86 \text{ pF}$$

Use 100 pF.

Voltage Loop

The voltage error amplifier must primarily limit the amount of 120Hz ripple seen at its output. The dynamic range of the error amplifier is 6.05VDC.

$$\Delta V_{\text{ea}} = (6.7 - 0.65) = 6.05 \text{ V}$$

In order to limit the 120Hz component of the voltage error amplifier output to 1.5% its magnitude must be limited to 91mV. This amounts to 0.75 % distortion at the multiplier output, leaving room for an additional 0.75% contribution due to miscellaneous sources. The IAC input will contribute the additional 1.5% at the multiplier output.

$$V_{\text{dist}} = V_{\% \text{dist}} \cdot \Delta V = 1.5\% \cdot 6.05 = 0.091 \text{ V}$$

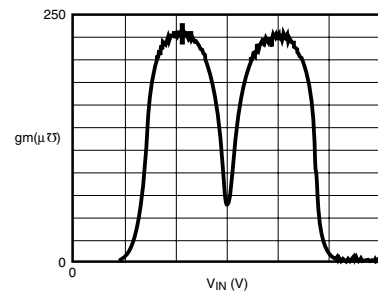


Figure 8. Voltage Error Amplifier Transconductance vs. V_{in}

Voltage amplifier 120Hz gain can be determined by examining the 120Hz component of the output cap ripple.

$$\text{Gain}_{120\text{Hz}} = \frac{V_{\text{dist}}}{V_{\text{pp}}} = \frac{0.091}{10.5} = 0.009 = -41 \text{ dB}$$

The error amplifier gain at 120Hz is assumed to be dominated by C11. The crossover frequency is assumed to be much less than 120Hz. See Figure 8 for a graph of the voltage error amplifier transconductance vs. V_{in} .

$$\text{Gain}_{120\text{Hz}} = \frac{R_{11}}{R_{11} + R_{10}} \cdot g_{\text{op}} \cdot \left(\frac{1}{2\pi \cdot 120\text{Hz} \cdot C_{11}} \right)$$

Resistor values R11 and R10 determine the DC operating point for the output voltage. The reference voltage for the error amplifier is 2.5VDC.

$$V_{\text{out}} = V_{\text{ref}} \cdot \frac{R_{10} + R_{11}}{R_{11}} = 2.5 \cdot \frac{364 \text{ k}\Omega + 237 \text{ k}\Omega}{237 \text{ k}\Omega} = 387 \text{ V}$$

$$C_{11} = \frac{R_{11}}{R_{11} + R_{10}} \cdot \frac{g_{\text{op}}}{2\pi \cdot 120\text{Hz} \cdot \text{Gain}_{120\text{Hz}}}$$

$$= \frac{237 \text{ k}\Omega}{237 \text{ k}\Omega + 364 \text{ k}\Omega} \cdot \frac{70 \mu\text{mho}}{2\pi \cdot 120\text{Hz} \cdot 0.009} = 66 \text{ nF}$$

Use 68nF.

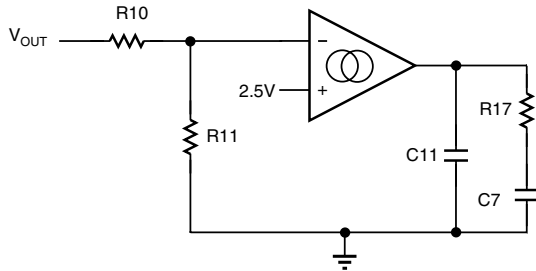


Figure 9. Voltage Error Amplifier

From here we step backwards and determine the crossover frequency and place a pole there. Multiplying the power stage gain times the error amp gain gives the loop gain. By setting this equal to unity and solving for the frequency we obtain the crossover point.

$$G_{pwr}(f) = \frac{P}{\Delta V_{ea} \cdot V_{out} \cdot j \cdot 2\pi f C} = \frac{-j \cdot 105}{f}$$

$$\text{Gain}_{amp}(f) = \frac{R_{11}}{R_{11} + R_{10}} \cdot g_{op} \cdot \frac{1}{2\pi f j C_{11}} = \frac{-j}{f}$$

$$G_{loop}(f) = G_{pwr}(f) \cdot G_{amp}(f)$$

$$G_{loop}(f) = \frac{105}{f} \cdot \frac{1}{f} = \frac{105}{f^2} = 1$$

$$f_c = \sqrt{105} = 10.5\text{Hz}$$

Set a pole at the crossover frequency

$$R_{17} = \frac{1}{2\pi f_c C_{11}} = 225\text{k}\Omega$$

Use 220k Ω .

Compensate with a zero one decade before the crossover frequency.

$$C_7 = \frac{1}{2\pi \cdot \frac{f_c}{10} \cdot R_{17}} = \frac{1}{2\pi \cdot \frac{10.5}{10} \cdot 220 \times 10^3} = 0.68\mu\text{F}$$

ZVS Sensing Network

The ZVS sensing network trips the ZVS comparator once the main Q voltage falls to zero. Reset of the ZVS comparator must occur prior to the following clock cycle. The FAN4822 uses leading edge modulation, and the trailing edge of the gate drive occurs at the end of the clock cycle, regardless of duty. This means simply sensing the main Q drain voltage rising may not trip the ZVS comparator prior to the subsequent clock cycle. For this reason the method used for resetting the ZVS Comparator does not depend upon the main Q drain voltage. Estimating the minimum on time at 200ns

requires resetting the ZVS comparator within 200ns. Figure 10 displays the ZVS sensing circuitry.

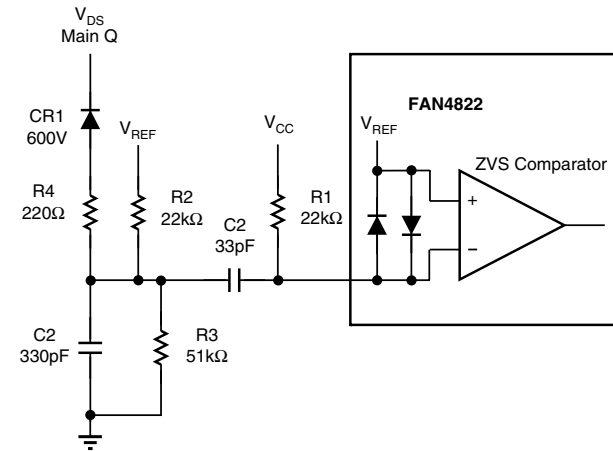


Figure 10. ZVS sensing Network

Oscillator Ramp

The oscillator frequency is determined by the values of R_T (R16) and C_T (C21). The period is the sum of the ramp time and the dead time.

$$t_{ramp} = C_T R_T \ln \left[\frac{V_{ref} - 1.25}{V_{ref} - 3.75} \right] = 0.51 \cdot R_T C_T$$

$$V_{ref} = 7.5\text{V}$$

$$T_{deadtime} = C_T \cdot \frac{25\text{V}}{7.5\text{mA}}$$

Typically the dead time will be so small that the oscillator period can be approximated by the ramp time.

$$f_{osc} = \frac{1}{t_{ramp}}$$

If there is a problem with the ZVS flip-flop not resetting prior to the end of the clock cycle, increasing the deadtime may help.

Over-Voltage Comparator:

For a large step in load from full load to no load the energy stored in the boost inductor must be absorbed by the output cap. With a very low bandwidth voltage loop, these large excursions can go unnoticed for a relatively long time before being compensated for. In fact, by the time the error amplifier recognizes the change the damage most likely would have already occurred. In order to keep these transitions minimized, an overvoltage comparator senses the output and shuts down the PFC during overvoltage conditions. The overvoltage comparator is fed by the same signal that feeds the voltage error amplifier. The PFC output is shut down when the feedback pin reaches 2.7V. The comparator hysteresis will reset at 2.575V.

Overvoltage

$$V_{ovp} = \left(\frac{R_{10} + R_{11}}{R_{11}} \right) \cdot 27V = \frac{364 \times 10^3 + 2.37 \times 10^3}{2.37 \times 10^3} \cdot 2.7 = 415V$$

Reset voltage

$$V_{ovp} = \left(\frac{R_{10} + R_{11}}{R_{11}} \right) \cdot 2.575V = \frac{364 \times 10^3 + 2.37 \times 10^3}{2.37 \times 10^3} \cdot 2.575 = 398V$$

V_{CC}

V_{CC} consists of an internal shunt zener regulator. The tolerance of the voltage is from 12.8 to 14.2VDC. The load regulation for V_{CC} is ±150 mV given an I_{CC} from 25 mA to 55 mA. Since the internal zener is clamped under normal operating conditions it must be fed by a high impedance in order to limit the current. In the design example we first ensure that the maximum zener current is not exceeded and that sufficient voltage is present to prevent undervoltage lockout.

The V_{CC} voltage is fed by the auxiliary winding of the boost inductor. The effective voltage is the turns ratio times the output voltage times the coupling coefficient.

$$V_{aux} = V_{out} \frac{N_{aux}}{N_{pri}} \cdot k = 400 \cdot \frac{1.5}{36} \cdot 0.8 = 13.3V$$

$$V_{cc} = V_{aux} - I_{cc} \cdot R_{series} = 13.3 - 0.06 \cdot 22 = 12V$$

For 60mA of I_{CC} and a 22Ω series resistor sufficient voltage is available. Next check that the internal zener current is limited to a safe value and that the series resistor power dissipation is safe.

$$I_{series} = \frac{V_{aux} - V_{ccmin}}{R_s} = \frac{13.3 - 12.8}{22} = 23mA$$

$$P_{series} = I_{cc}^2 \cdot R_{series} = 0.06^2 \cdot 22 = 0.08W$$

Measured Results

Efficiency improved from 87% (without ZVS) to 92% (with ZVS) at 120VDC input. At 370VDC input the efficiency, with or without ZVS operation, is roughly 95%.

Figure 11 shows the main switch current and voltage at turn on. The reverse current is due to the resonant circuit and eventually flows through the body diode. The drain current does not build up until the drain voltage has dropped to zero. The reverse recovery spike due to the free-wheeling diode has been eliminated.

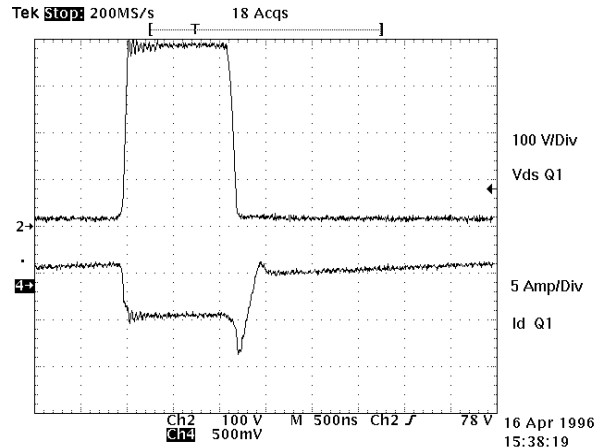


Figure 11. Main Switch Q Turn On Waveform

Figure 12 shows the gate drive waveforms of the main and ZVS transistors. The ZVS drive is high until the main transistor voltage fall to zero. The ZVS pulse is then terminated and the main gate drive initiated.

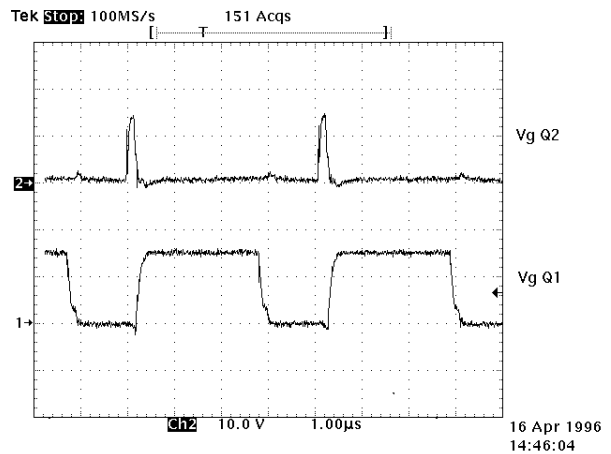


Figure 12. Gate Drive Waveforms

Figures 13 and 14 display the ZVS inductor current and transistor voltage. Note the quick reset of the ZVS inductor subsequent to the termination of the ZVS pulse.

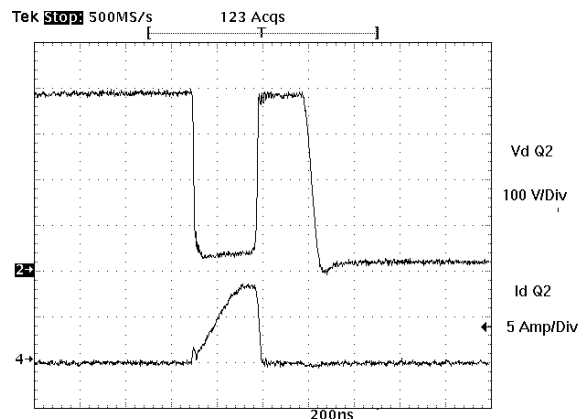


Figure 13. ZVS Waveforms

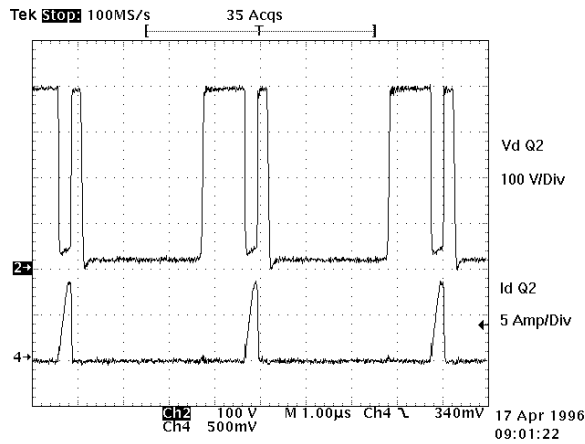


Figure 14. ZVS Waveforms

Figure 15 shows the main transistor current and voltage, while Figure 16 shows the timing of the ZVS and main transistor voltages.

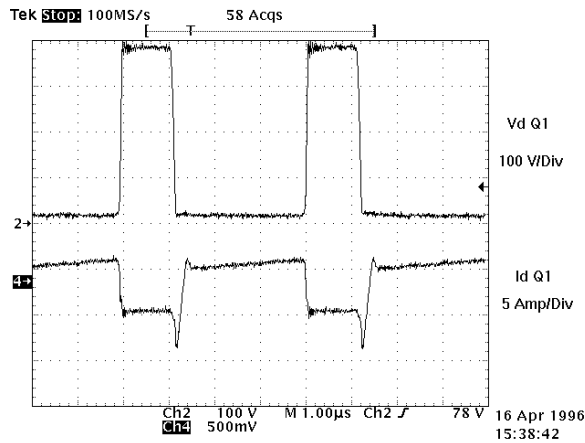


Figure 15. Main Q Waveforms

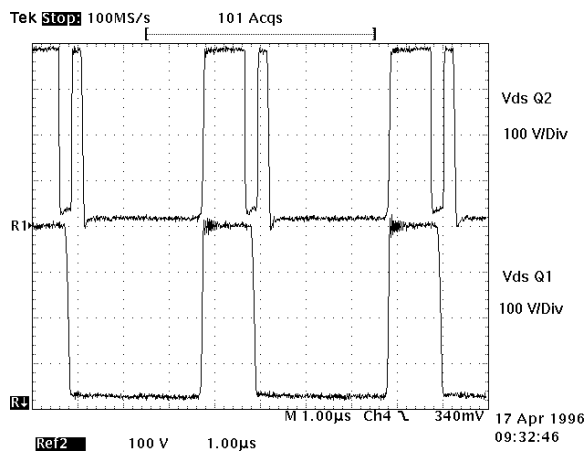


Figure 16. Drain Waveforms

Figure 17 is a graph of efficiency versus DC input voltage. The graph compares efficiency with and without the ZVS circuitry. Figure 18 is a graph of efficiency versus AC voltage.

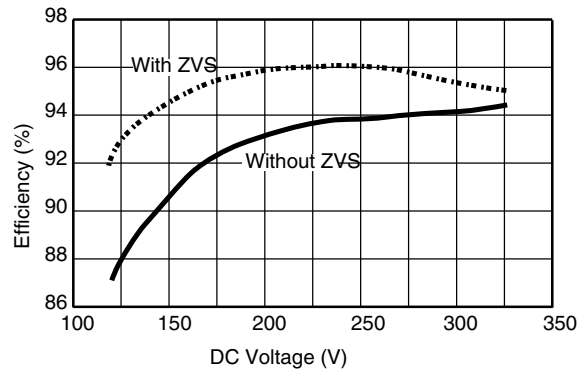


Figure 17. DC Efficiency, with and without ZVS

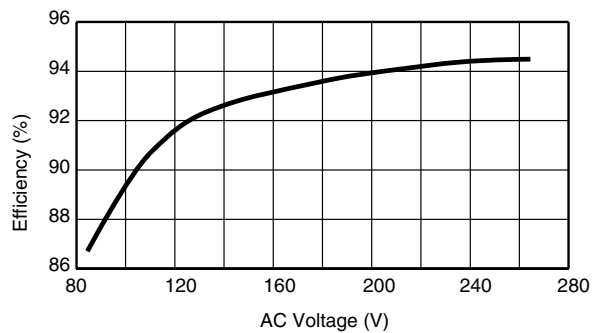


Figure 18. AC Efficiency

Conclusion

In a standard boost the selection of the freewheeling diode is critical. If the diode is too slow, thermal runaway is a likely problem. With ZVS switching of a Boost converter the freewheeling diode, even at 250 kHz, is not nearly as critical as with a standard boost. In fact, a standard ultra-fast recovery diode may be sufficient. This can be important when some of the more specialized diodes are difficult to obtain.

Increase in capacitance across the main switch is possible with little penalty in efficiency. This is true even at 250kHz. This allows for reduction in EMI due to the dv/dt of the main Q at turn off.

The limitations on frequency of operation for the ZVS Boost are the switching losses in the ZVS Q and the core losses in the saturable reactor. Higher power levels may require reduced switching frequencies or other methods which do not require a saturable reactor.

In summary, the FAN4822 solution significantly reduces stress on the boost diode and transistor, allows for a higher frequency of operation at an improved efficiency, and reduces electromagnetic interference.

Bill of Materials

Part	Value
Resistors	
R1	220Ω, 1W, 5%
R2, R3	10Ω 1/4 W, 5%, carbon comp.
R4,R6	10kΩ, 1/4 W, 5%, carbon film
R7	22Ω, 1/4 W, 5%, carbon film
R10	364kΩ, 1 W, 1%, carbon film
R11	2.37kΩ, 1/4 W, 1%, carbon film
R12	906kΩ, 1/4 W, 1%, carbon film
R13	1MΩ, 1/4 W, 1%, carbon film
R14	100kΩ, 1/4 W, 1%, carbon film
R15	10.2kΩ, 1/4 W, 1% carbon film
R16	22.6kΩ, 1/4 W, 1%, SMD 1206
R17	220kΩ, 1/4 W, 5%, SMD 1206
R18	0.0732Ω, 5 W, 1%
R19	10kΩ, 1/4 W, 5%, SMD 1206
R21	2x39kΩ, 2 W, 5%, metal film
R25, R27	22kΩ, 1/4 W, 5%
R26	51kΩ, 1/4 W, 5%
R28	220Ω, 1/4 W, 5%
Capacitors	
C1	330μF, 450 V, Electrolytic
C2	470pF, 1600 V, Wima FKP1
C4, C5	0.1μF, 35 V, Ceramic
C6	0.47μF, 50 V, Ceramic
C7	0.68μF, 10%, 50 V, Ceramic
C8, C9, C10, C17, C18	1μF, 35 V, Ceramic
C11	0.068μF, 10%, 50 V, Ceramic
C12	2.2nF, 10 %, 50 V, Ceramic
C13	100pF, 10 %, 50 V, Ceramic
C15	0.47μF, 250 VAC, Wima MKS4-R
C16	1500μF, 35 V, 20%, Electrolytic
C19	33pF, 5%, 50 V, NPO Ceramic
C20, C21	330pF, 5%, NPO Ceramic

Part	Value
Diodes	
B1	Fairchild / GBPC2506
D1	Fairchild / ISL9R1560P2
D2	Fairchild / ISL9R860P2
D3	Fairchild / EGP30J
D4, D10, D11, D12	Fairchild / EGP10J
D5, D6	Fairchild / IN4747A
D8, D9	Fairchild / IN5818
Transistors	
Q1	Fairchild / FGH30N6S2D
Q2	Fairchild / IRF830B
IC's	
U1	Fairchild / FAN4822IM ZVS PFC
U2	TelCom / TC4427 Gate Drive
Magnetics	
L1	165 μH 10 A
L2	8.5 μH 14 A
L3	Saturable Reactor
Fuse	
F1	7A, 250 VAC Fast Blow

Magnetics Construction

L1: Boost Inductor, 165 μH @ 10A
Magnetics Inc., E21 Core, P/N P-44317-EC
Magnetics Inc., Bobbin, P/N PC-B4317-L1
36 Turns, 17 AWG, 45 mil Butt gap.
Start pins 11, 12, Finish pins 7, 8
1° Turns 29 AWG pins 5, 6

L2: Resonant Inductor, 8.5 μH @ 14A
Magnetics Inc., E2425 Core, P/N P-42510-EC
Magnetics Inc., Bobbin, P/N PC-B2510-T1
20 Turns, 19 AWG, 30 mil Butt gap.
Start pins 2, 3 Finish pins 8, 9

L3: Saturable Reactor
Toshiba, MS18 ´ 12 ´ 4.5
9 Turns, 19 AWG

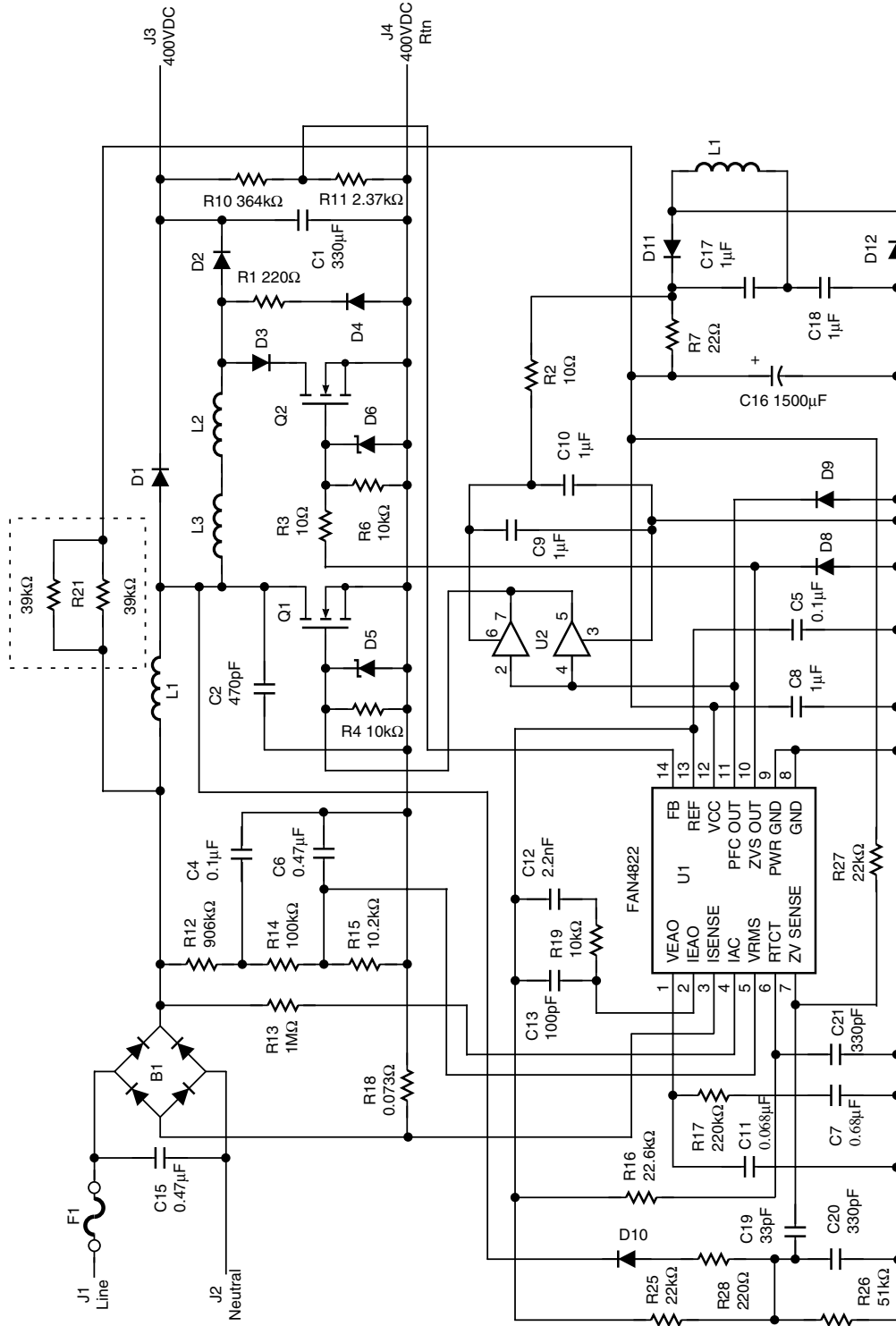


Figure 19. Schematic

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