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# Low Voltage Device Output Load Specifications, 30pF versus 50pF

### Introduction

With the development of 2.5 volt $V_{CC}$ low voltage CMOS families, JEDEC (Joint Electron Device Engineering Council) has specified a 30 pF output test load for devices that are designed to operate primarily in this 2.5 volt range. The load differs from the 50 pF output load that has been used in CMOS devices designed to operate primarily with 3.3 volt and higher supply voltages. However, many device families, such as Fairchild Semiconductor's LCX and LVT product lines are specified to run with $V_{CC}$'s from 3.6 volts down to 2.0 volts. These devices use a 50 pF output load for specification. Other families specified to run in this voltage range, and lower, such as Fairchild Semiconductor's VCX™ family, which are designed to run with $V_{CC}$'s from 3.6 volts to 1.8 volts, use a 30 pF output load for specification. As can be seen, there is a considerable range of voltage overlap. This gives the low voltage system designer many family device options to select from, but also poses a dilemma. How does one derive an equitable performance comparison when the products are not tested and specified to the same output load? Fairchild Semiconductor has recognized the need to answer this question.

### What do the load specifications mean?

JEDEC standard JESD64 defines a 30 pF output test load for devices designed to run primarily in the 2.5 volt range. The output load differs from the JESD36 standard of a 50 pF test load for devices designed to run primarily in the 3.3 volt range and higher.

The output load specified by JEDEC includes the test jig stray capacitance, load capacitance (lumped) and test probe parasitics. Essentially, the load consists of test jig output line and stub capacitance, plus a lumped load capacitance to add up to the specified value. As line and stub capacitance in test fixtures are intentionally designed to have minimum capacitance, the lumped load makes up most of the specified output capacitive load. This means that the only quantifiable difference between the 30 pF and 50 pF test fixtures will be the size of the lumped load Figure 1.

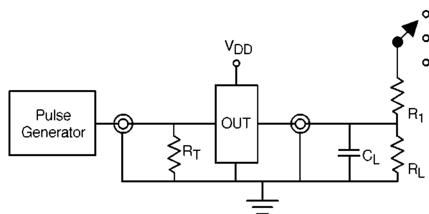


**FIGURE 1. The JEDEC specified test circuit. (This circuit is identical for both JESD36 and JESD64 with the exception of the specified output capacitive load ($C_L$))**

### How is an accurate comparison made?

Output load differences can lead to confusion when attempting to compare specifications such as the propagation delay of two technologies, when one is tested and specified with 50 pF and the other is tested and specified with 30 pF.

Since device output behavior will be directly affected by the driven load, it is important to understand which parameters will be affected, and how the device behavior will change.

**Affected Parameters:**

**Edge Rate** - When driving a capacitive load, the 'on' resistance, as well as the saturation point of an output, limit the transition time due to the finite rate at which the output load can be charged or discharged. This behavior is essentially the same for a bipolar device. When a CMOS transistor enters saturation, it acts as a constant current source.

$$\Delta V = \frac{I \ \Delta t}{C}$$

When $\Delta V$ is the change in voltage across the capacitive load, I is the saturation current, $\Delta t$ is the change in time, and C is the capacitance value of the output load.

As it charges or discharges the load to the point where it falls out of saturation mode, the device acts resistive, and the RC time constant takes over the discharge rate.

$$\Delta V = \frac{I(t) \ \Delta t}{C}$$

Where $\Delta V$ is the change in voltage across the capacitive load, I(t) is the instantaneous current, $\Delta t$ is the change in time, and C is the capacitance value of the output load.

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**Propagation Delay** - The internal propagation delay of a device is not effected by the output load. However, the effective propagation delay will change with output load size. Propagation delay variability is due to the change in output edge rates, which are directly effected by the load Figure 2.

CMOS propagation delays are typically measured at the 50% point of the waveform, input edge to output edge. The longer the output edge takes to cross the measure point due to load size, the longer the measured propagation delay time will be.

**Input LH versus 30 pF and 50 pF Output Load**

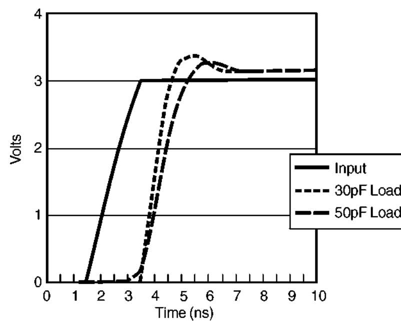


**FIGURE 2. A comparison of typical Low to High propagation delay from Input signal to a 30 pF load, and a 50 pF load.**

$\mathbf{f_{MAX}}$ - If a load becomes heavy enough, and if frequency is high enough, the same RC effects limit or reduce both the Voltage Output High level ($V_{OH}$) and the Voltage Output Low level ($V_{OL}$) of the output. The point at which $V_{OH}$ is reduced to the Voltage Input High level ($V_{IH}$) switch point or the $V_{OL}$ is limited to the Voltage Input Low level ($V_{IL}$) switch point is referred to as $f_{MAX}$, or the maximum frequency of operation.

**Noise** - The output voltage fluctuations, during and after edge transitions, are often referred to as ground bounce. These voltage fluctuations are greatly affected by the size of the capacitive load.

$$I = C_L \frac{dV}{dt}$$

Where I equals current generated charging the load, $C_L$ is the load capacitance, dV instantaneous voltage, and dt instantaneous time.

Additionally, load type plays a critical part in output signal behavior, i.e. lumped versus distributed. A lumped load, close to the device output such as that in a test circuit, has a much higher instantaneous current demand, than for example, a distributed load.

$$I(t) = C_L \frac{dV}{dt}$$

Where I(t) is instantaneous current demand, t is time, and $C_L$ is load capacitance, dV instantaneous voltage, and dt instantaneous time.

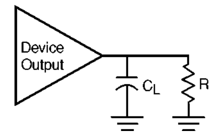


**FIGURE 3. A lumped capacitive load ($C_L$) in a test circuit is placed as close to the device output as possible. For practical purposes, propagation delay from device output to the load is zero.**

The high instantaneous current demand from the lumped capacitive load causes more rapid current changes in the $V_{CC}$ and ground planes, package bond wires and lead frames. The inductive resistance to a current change is seen as a voltage shift or 'bounce' on the output signal.

BiCMOS design devices, such as Fairchild's LVT family, behave somewhat differently than pure CMOS devices. LVT has high drive outputs, which enable this family to drive various loads with less edge rate variation. Additionally, a bipolar transistor tends to limit current at the ends of its voltage transition; this design somewhat limits ground bounce. This behavior is reflected in the included noise and edge rate derating graphs.

**The Solution: Comparison Options**

To accurately compare multiple device types that may be specified to different output loads, several methods can be used.

**Bench Testing** - Test and measurement of multiple device families in a common, repeatable test setup is a good way to evaluate characteristic differences. Suitability of various product types for a system design can be accurately evaluated provided the test setup is representative of the end application, and is exactly repeated for all families. However, process variability needs to be taken into account. And, for some end users, bench testing is not a practical option, due to time, or various other bandwidth constraints.

**Fairchild Semiconductor Supplied Data** - Fairchild Semiconductor supplies additional, non-datasheet information for our low voltage families. This data is of two types; electronic device models (i.e. HSPICE and IBIS), and additional published family and device data.

**Models** - Fairchild Semiconductor has parametric models available for our low voltage devices. Because the use of simulation in the system design cycle is more common, Fairchild Semiconductor supplies models of most low voltage offerings. Models can be requested from a Fairchild Semiconductor representative. To compare the output behavior of various product families to one another, IBIS (I/O Buffer Information Specification) or HSPICE I/O models are recommended.

Running the family I/O models from multiple families while using the same output load structure will give an accurate comparison of output behavior. The data that can be compared using these types of models include; output edge rate, active edge noise, and $V_{OH}$ and $V_{OL}$ behavior. If no model is available for the particular device being evaluated, a function type equivalent usually can be substituted, i.e. a gate for a gate, a 3-STATE buffer for a 3-STATE buffer.

**Additional Data** - This data is in the form of extended specifications and device family specifications. Fairchild Semiconductor also includes non-specified device characteristics data. This data is published in the Extended Specifications and Characteristics section included in Fairchild Semiconductor's Advanced Logic Products data book. The data is quite extensive and includes output load derating plots for Multiple Output Switching (MOS) and Output Edge rates.

Data specific to this application note discussion is included in Appendix A for the LVT, LCX and VCX *CROSSVOLT*™ Low Voltage families. This data is in the form of output load derating graphs.

Data is included for all of the following:.

- Output edge rate, single output switching at 2.5 $V_{CC}$ and 3.3 $V_{CC}$
- Propagation delay, single output switching, eight data pins switching, and sixteen data pins switching, at 3.3 $V_{CC}$
- Noise data has been included for $V_{OLPHL}$ (Voltage Out Low Peak, High to Low) and $V_{OLVHL}$ (Voltage Out Low Valley, High to Low) at 2.5 $V_{CC}$ and 3.3 $V_{CC}$.

The data can be used to help compare various families to one another.

**Note:** All of the data is taken on the 16244 device type.

**Summary**

As low voltage logic migrates to 2.5 $V_{CC}$ and below, a new 30 pF output specification has been introduced by JEDEC. For accurate comparisons of devices that are specified with different output loads, an understanding of what parameters are effected, and also why it is important. Several options are available to facilitate the end user in making accurate comparisons; including bench testing, Parametric Device modeling, and Vendor supplied supplementary data.

These various output data sources give a system designer multiple options for deriving a performance correlation between families that are specified at different output loads.

**Appendix A Output Load Derating Graphs**

**Edge Rate Derating Plots** - Figures 4 - 7 compare 16244 devices in LVT, LCX and VCX technology. Loading is from 10 pF to 100 pF, tested $V_{CC}$'s are 2.5 V and 3.3 V. Setup is Single Output Switching (SOS), all others held low.

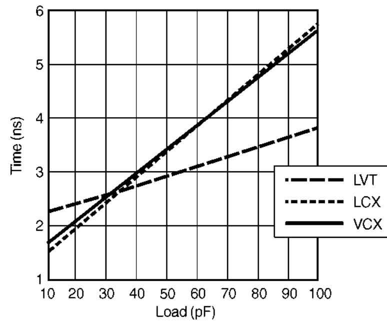


**FIGURE 4. Edge Rate versus Load @ 2.5V, Rise Time**

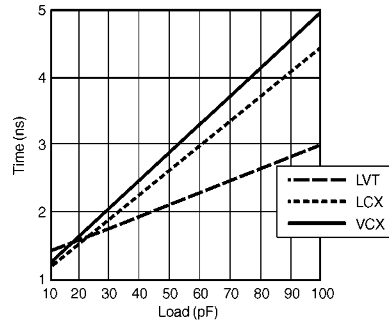


**FIGURE 6. Edge Rate versus Load @3.3V, Rise Time**

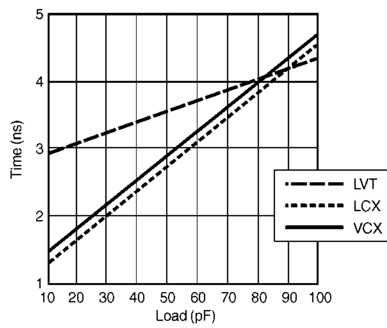


**FIGURE 5. Edge Rate versus Load @ 2.5V, Fall Time**

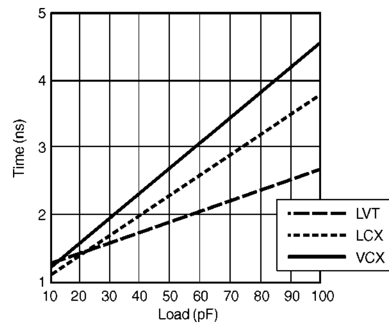


**FIGURE 7. Edge Rate versus Load @ 3.3V, Fall Time**

**Propagation Delay Derating Plots** - Figures 8 - 13 compare 16244 function devices in LVT, LCX and VCX technology. Loading is from 30 pF to 100 pF, tested $V_{CC}$ is 3.3V. Setups are: Single Output Switching, all others held low (SOS); Multiple Outputs Switching, 8 data pins switching, others held low (MOS8); and Multiple Outputs Switching, all 16 data pins switching (MOS16).

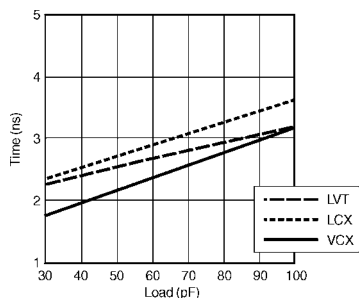


**FIGURE 8. $t_{PLH}$ versus Load @ 3.3 V, SOS**

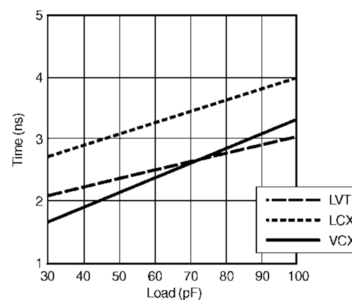


**FIGURE 9. $t_{PHL}$ versus Load @ 3.3 V, SOS**

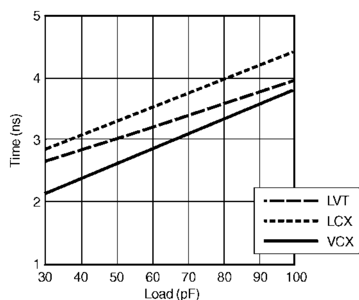


**FIGURE 10. $t_{PLH}$ versus Load @ 3.3 V, MOS8**

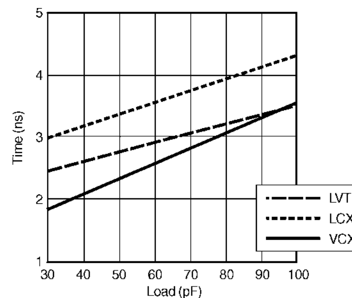


**FIGURE 11. $t_{PHL}$ versus Load @ 3.3 V, MOS8**

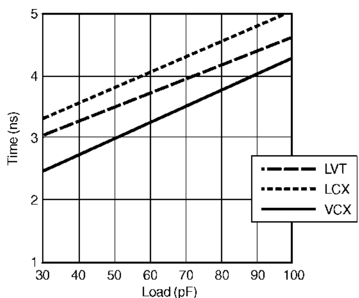


**FIGURE 12. $t_{PLH}$ versus Load @ 3.3 V, MOS16**

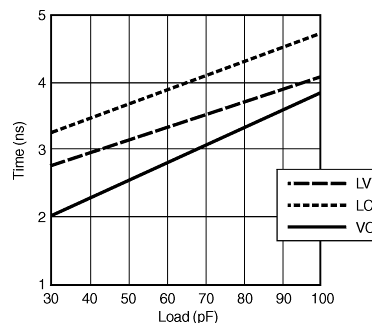


**FIGURE 13. $t_{PHL}$ versus Load @ 3.3 V, MOS16**

**Noise Derating Plots** - Figures 14 - 17 compare 16244 function devices in LVT, LCX and VCX technology. Loading is from 10 pF to 100 pF, tested $V_{CC}$'s are 2.5 V and 3.3 V. Setup is Multiple Outputs Switching (MOS), all 16 outputs switching. Data is for $V_{OLVHL}$ and $V_{OLPHL}$.

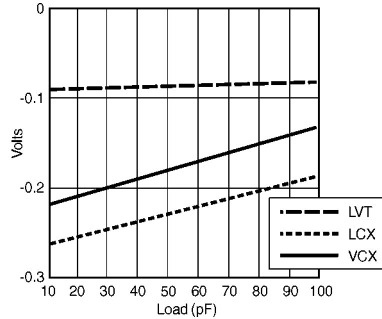


**FIGURE 14. $V_{OLVHL}$ @ 2.5$V_{CC}$**
**Load versus Noise (voltage valley)**

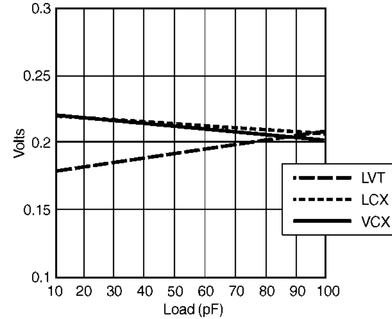


**FIGURE 15. $V_{OLPHL}$ @ 2.5$V_{CC}$**
**Load versus Noise (voltage peak)**

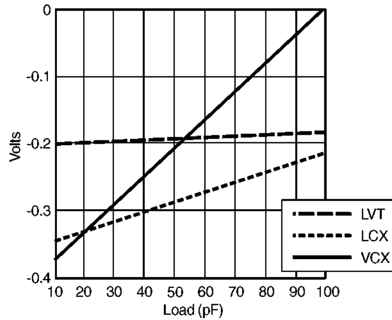


**FIGURE 16. $V_{OLVHL}$ @ 3.3$V_{CC}$**
**Load versus Noise (voltage valley)**

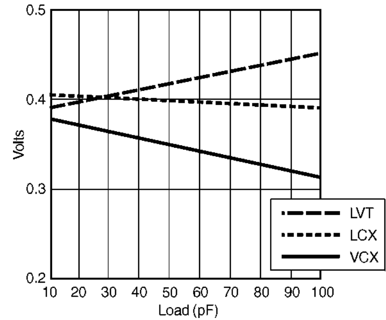


**FIGURE 17. $V_{OLPHL}$ @ 3.3$V_{CC}$**
**Load versus Noise (voltage peak)**


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