

Fairchild Solutions for 133MHz Buffered Memory Modules

Fairchild Semiconductor provides several products that are compatible with the PC133 SDRAM Registered DIMM Specification. Many of today's 133MHz SDRAM memory modules require buffering due to the inability of the system memory controller to drive the large amount of memory devices, while maintaining signal integrity or timing; but typically use a registered device to maintain the synchronous timing of the system. The 168-pin registered SDRAM DIMM is a JEDEC-defined device (Rev. 1.1). This standard defines which signal paths need to be buffered, the polarity of the latch enable, et al.

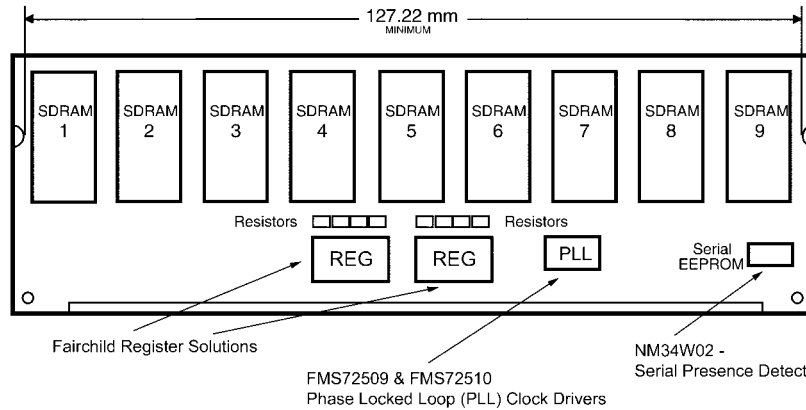


FIGURE 1. Fairchild PC133 Support Products for Registered DIMMs

FMS72509 & FMS72510

Phase Locked Loop (PLL) Clock Drivers

- PC133 spread spectrum compliant
- Frequency range of 75 MHz to 150MHz
- V_{DD} range of 3.0V to 3.6V
- Less than 150ps output-to-output skew
- Less than 150ps cycle-to-cycle jitter
- 24-pin TSSOP package

NM34W02

Serial Presence Detect

- 2K-bit EEPROM with standard 2-wire bus interface
- Permanent Write Protection for first 128 bytes provides Serial Presence Detect function
- Supports 133MHz
- 1.8V to 5.5V operating range
- Available in 8-pin TSSOP

Fairchild Register Solutions

Device #	Function
74VCXF162835	18 Bit Universal Buffer
74VCX16838	16 Bit Selectable Register Buffer
74VCX162838	16 Bit Selectable Register Buffer w/ 25 Ohm Resistor
74VCX16839	20 Bit Selectable Register Buffer
74VCX162839	20 Bit Selectable Register Buffer w/ 25 Ohm Resistor

PC133 SDRAM Register and PLL Recommendations

Raw Card Version	Module Size	Registers			PLL
		Option 1	Option 2	Option 3	
A, AA	64MB - 256MB	2 - 74VCXF162835	2 - 74VCX1839	2 - 74VCX16838	1 - FMS72509
B (Planar)	128MB - 512MB	3 - 74VCXF162835	3 - 74VCX16839	2 - 74VCX16839 1 - 74VCX16838	1 - FMS72510
B, C, D (Stacked)	256MB - 1024MB	3 - 74VCXF162835	3 - 74VCX16839	2 - 74VCX16839 1 - 74VCX16838	1 - FMS72510

Recommended EEPROM Device

The NM34W02L is designed with Permanent Write Protection for the first 128 Bytes for Serial Presence Detect (SPD) function on memory modules. The NM34W02 (2k Bit EEPROM with Standard 2 wire bus interface) is PC100 compliant and is recommended for PC133 modules. The operating voltage for this device is 2.7V 0-5.5VG V_{DD} and is available in the 8 pin JEDEC standard TSSOP Package.

JEDEC PC133 Specification

The JEDEC PC133 specification (Rev.1.1) calls out the following recommendations for each raw card type.

JEDEC PC133 Standard Solutions by PC133 Raw Card Type

Raw Card	Register Type	SDRAMs Per Output	Registers Per Module	PLL Type	SDRAMs Per Output	PLLs Per Module
A	VCXF162835	9	2	FMS72509	3	1
AA	VCXF162835	9	2	FMS72510	3	1
B	VCXF162835	9	3	FMS72510	3	1
		18	3	FMS72510	3	1
C	VCXF162835	18	3	FMS72510	3	1
D	VCXF162835	18	3	FMS72510	3	1
E	VCXF162835	9	3	FMS72510	3	1

Register Specifications

Parameter	Symbol	PC133 (REV 1.1)		74VCXF162835		74VCX16838		74VCX16839		Units
		$C_L = 50 \text{ pF}$		$C_L = 50 \text{ pF}$		$C_L = 50 \text{ pF}$		$C_L = 50 \text{ pF}$		
		Min	Max	Min	Max	Min	Max	Min	Max	
Max Clock Frequency	f_{MAX}				250		250		250	MHz
Propagation Delay CLK to Y	$t_{PHL/LH}$	1.4	3.5	1.4	3.5	1.4	3.3	1.4	3.5	ns
Setup Time	t_{SET}	1.0		1.0		1.0		1.0		ns
Hold Time	t_{HOLD}	0.6		0.6		0.7		0.7		ns
Input Current	I_{IN}		10.0			5.0	5.0		5.0	μA
CLK Input Capacitance	C_{IN}	3.30	6.00	3.6 (Typ)		3.6 (Typ)		3.6 (Typ)		pF

Note: AC Specifications for the FSC products above are for $V_{CC} = 3.3V \pm 0.3V$, and $T_A = 0^\circ\text{C}$ to 85°C unless specified otherwise.
JEDEC Specifications are for $T_A = 0^\circ\text{C}$ to 70°C .

PLL Specifications

Parameter	Symbol	PC133 (REV 1.1)			FMS72509/72510			Units
		Min	Typ	Max	Min	Typ	Max	
Operating Frequency	f_{MAX}	50		140	50		140	MHz
Jitter (Output in CLK_n to CLK_{n+1})	t_{JIT}	-75		+75	-75		+75	ps
SSC Induced Skew	t_{SSC}			+150			+150	ps
Skew	t_{SK}			+150			+150	ns
Clock Input Capacitance	C_{IN}		4			4		pF

Note: AC Specifications for the FSC products above are for $V_{CC} = 3.3V \pm 0.3V$, and $T_A = 0^\circ\text{C}$ to 70°C unless specified otherwise.

Alternative Register Routing Solutions

The JEDEC PC133 Specification (Rev. 1.1) defines required performance and functionality for registers. While the specification suggests specific IC part numbers, the specification allows for other alternatives. The tables below show alternatives that meet the performance and functional requirements of the JEDEC specification.

For Raw Card Version "A" or "AA" DIMMs: (9 SDRAMs Per DIMM)

Register Options:	Possible Module Sizes
Opt 1. 2 - VCX16839's	a) 64 Mbyte - Using 64 Mbit SDRAM Devices
Opt 2. 1 - VCX16839's and 1 - VCX16838	b) 128 Mbyte - Using 128 Mbit SDRAM Devices
Opt 3. 2 - VCX16838's	c) 256 Mbyte - Using 256 Mbit SDRAM Devices

For Raw Card Version "B" (Planar) DIMM's: (18 SDRAMs Per DIMM)

Register Options:	Possible Module Sizes
Opt 1. 3 - VCX16839's	a) 128 Mbyte - Using 64 Mbit SDRAM Devices
Opt 2. 2 - VCX16839's and 1 - VCX16838	b) 256 Mbyte - Using 128 Mbit SDRAM Devices
	c) 512 Mbyte - Using 256 Mbit SDRAM Devices

For Raw Card Version "B", "C", "D" (Stacked) DIMM's: (36 SDRAMs Per DIMM)

Register Options:	Possible Module Sizes
Opt 1. 3 - VCX16839's	a) 256 Mbyte - Using 64 Mbit SDRAM Devices
Opt 2. 2 - VCX16839's and 1 - VCX16838	b) 512 Mbyte - Using 128 Mbit SDRAM Devices
	c) 1,024 Mbyte - Using 256 Mbit SDRAM Devices

For Raw Card Version "E" DIMM's: (9 SDRAMs Per DIMM)

Register Options:	Possible Module Sizes
Opt 3. 3 - VCX16839's	d) 128 Mbyte - Using 64 Mbit SDRAM Devices
Opt 4. 2 - VCX16839's and 1 - VCX16838	e) 256 Mbyte - Using 128 Mbit SDRAM Devices
	f) 512 Mbyte - Using 256 Mbit SDRAM Devices

Register Wiring

Register Wiring on Raw Card Version "A" or "AA" or "E" DIMMS

Option 1: - 2 - VCXF162835 - (JEDEC PC133 Specification (Rev.1.1) Solution)

Option 2: - 2 - VCX16839's

Option 3: - 1 - VCX16839 & 1 - VCX16838

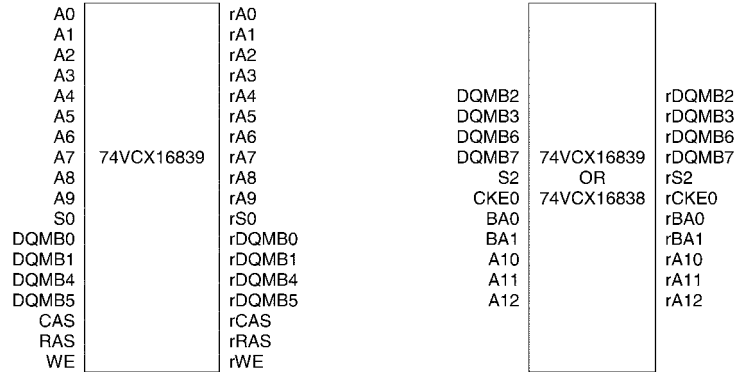
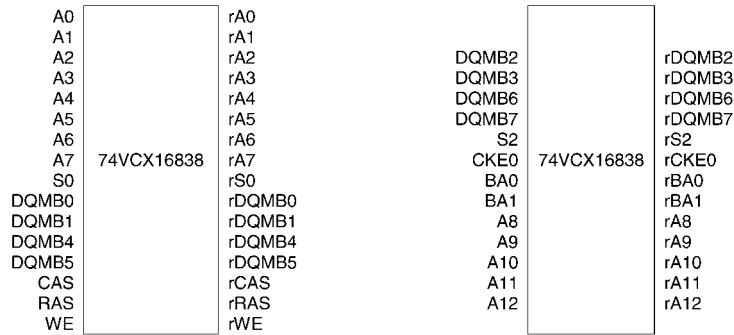


FIGURE 2. Wiring Options for 2 Register DIMMs

Option 4 - 2 VCX16838's



Note: A12 is only used with 256 Mbits SDRAMs

FIGURE 3. Wiring Options for 2 Register DIMMs

Register Wiring (Continued)**Register Wiring on Raw Card Version 'B', 'C', 'D' DIMMS**

Option 1: - 3 - VCXF162835 - (JEDEC Specification (Rev.1.1) Solution)

Option 2: - 3 - VCX16839s

Option 3: - 2 - VCX16839 AND 1 - VCX16838

A0		rA0A	A0	rA0B	DQMB0	rDQMB0		
A1		rA1A	A1	rA1B	DQMB1	rDQMB1		
A2		rA2A	A2	rA2B	DQMB2	rDQMB2		
A3		rA3A	A3	rA3B	DQMB3	rDQMB3		
A4		rA4A	A4	rA4B	DQMB4	rDQMB4		
A5		rA5A	A5	rA5B	DQMB5	rDQMB5		
A6		rA6A	A6	rA6B	DQMB6	rDQMB6		
A7	VCX16839	rA7A	A7	VCX16839	rA7B	DQMB7	VCX16839	rDQMB7
A8		rA8A	A8	OR	rA8B	S0		rS0
A9		rA9A	A9	VCX16838	rA9B	S1		rS1
A10		A10A	A10		A10B	S2		rS2
A11		A11A	A11		A11B	S3		rS3
BA0		BA0A	BA0		BA0B	WE		rWEA
BA1		BA1A	BA1		BA1B	WE		rWEB
RAS		RASA	RAS		RASB	A12		rA12A
CAS		CASA	CAS		CASB	A12		rA12B
CKE0		CKE0A				CKE1		rCKE1A
CKE0		CKE0B				CKE1		rCKE1B

Note: A12 is only used with 256 Mbits SDRAMs**Note:** CKE1 usage is an option on Raw Card Version "D" only.**FIGURE 4. Wiring Options for 3 Register DIMMs****Layout Modifications for using the VCX16839**

Using the VCX16839 instead of a '162835 function can easily be accomplished through minimal changes to the standard JEDEC gerber files. Figure 5 and Figure 6 provide a comparison of the pinout of the VCXF162835 function and the VCX162839 function. By examining these pinouts, it can be seen that the input and output data pins of a '162835 function will map to data pins of the VCX162839 function. The only pins that are not in the right location are the LE, REGE pins and the CLK signal; and only the CLK net is critical. The procedure listed in the adjacent column provides step by step directions on modifying the standard gerber files.

The clock net between the PLL and registers would need to be modified and re-balanced for proper operation. While this is a critical net the modification is relatively minor and the standard timing of the gerber module will be able to be maintained. Figure 7 shows an example of how the clock net could be modified. The clock nets between the PLL's and the SDRAMs do not need to be adjusted.

What Does Not Change:

1. All V_{CC} connections are identical.
2. GND connections to Pins 4, 11, 18, 25, 32, 39, 46 and 53 are identical.
3. Data input and output nets remain identical.

Required Changes:

1. CLK net moves from Pin 30 of the VCXF162835 to Pin 56 of the VCX16839.
2. Tiny Gate Inverter in REGE path must be eliminated from module and replaced with jumper. REGE signal is rerouted to Pin 29 of VCX16839. (Non Critical Change)
3. Pin 1 (\overline{OE}) of VCX16839 should be connected to GND. OE signal moves from Pin 27 of '16835 to Pin 1 of VCX16839.
4. Pins 2, 27, 28 of VCX16839 should be left to float.
5. Pins 30 and 55 of VCX16839 should be connected to GND to prevent floating inputs.

Layout Modifications for using the VCX16839 (Continued)

VCXF162835 Pinout

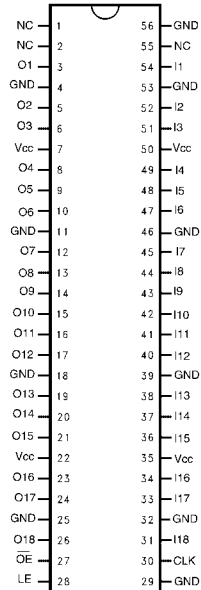


FIGURE 5.

VCX16839 Pinout

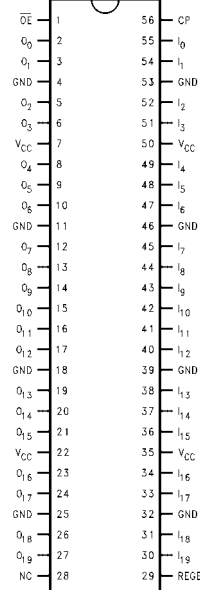


FIGURE 6.

Clock Net Rerouting Example

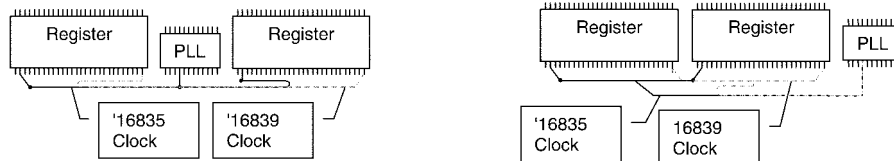


FIGURE 7.

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