AN-5841

Applying SG5841 to Control a Flyback Power Supply

Summary

This application note describes a detailed design strategy for a high-efficiency, compact flyback converter. Design considerations, mathematical equations, and guidelines for a printed circuit board layout are provided.

Features

- Green-Mode PWM Controller
- Low Startup Current: 14µA
- Low Operating Current: 4mA
- Programmable PWM Frequency with Hopping
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Synchronized Slope Compensation
- Leading-Edge Blanking (LEB)
- Constant Output Power Limit
- Totem-Pole Output with Soft Driving
- V_{DD} Over-Voltage Clamping
- Programmable Over-Temperature Protection (OTP)
- Internal Open-Loop Protection
- V_{DD} Under-Voltage Lockout (UVLO)
- GATE Output Maximum Voltage Clamp: 18V

Description

The SG5841 is a highly integrated PWM controller IC. It provides features to satisfy the need for low standby power consumption. With low startup current and low operating current, high-efficiency power conversion is achieved. Typical startup current is only 14µA and operating current is around 4mA. In nominal loading conditions, the SG5841 operates at fixed PWM frequency. As the load decreases, its proprietary green-mode circuit gradually reduces the PWM frequency. This green-mode function dramatically cuts the power loss in no-load and light-load conditions, enabling the power supply to meet power conservation requirements.

Additionally, the controller incorporates many protection functions. Once the power supply is overloaded, the controller forces the power supply into "hiccup" mode to limit output power. The built-in line-voltage compensation circuit maintains constant maximum output power for a wide input line voltage range. An external negative-temperature-coefficient (NTC) thermistor can be connected to the RT pin for over-temperature protection.

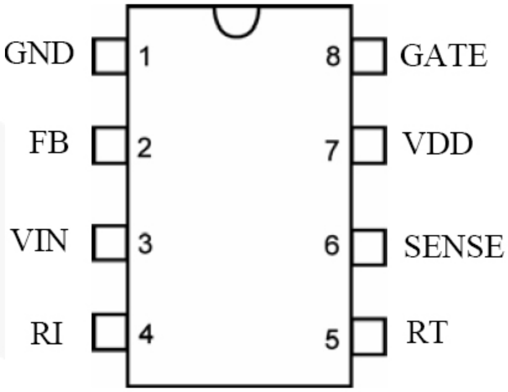

Figure 1. Pin Configuration

Block Diagram

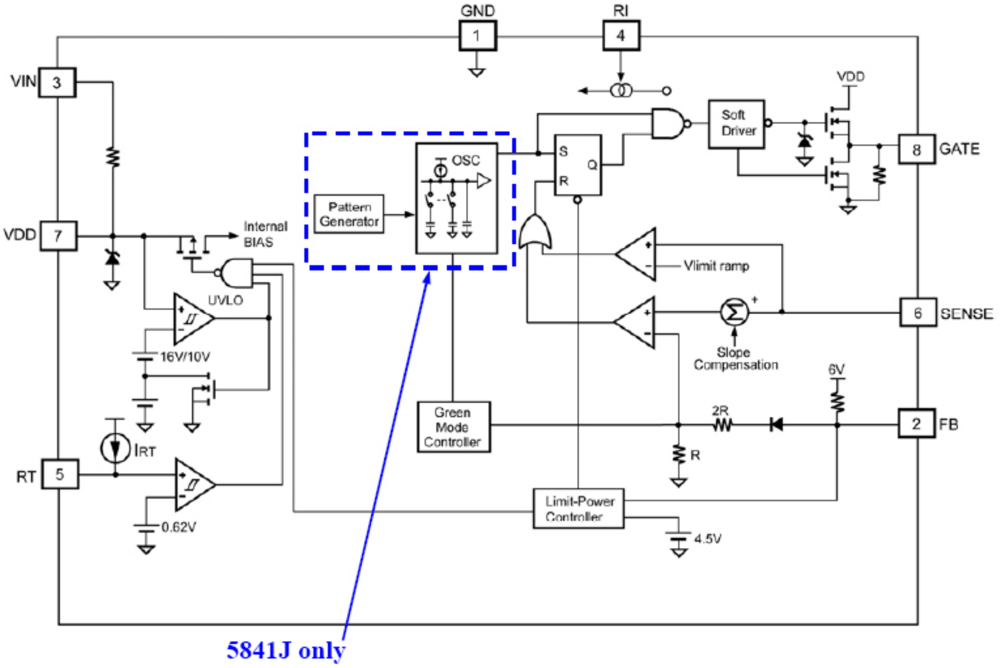

Figure 2. Block Diagram

Startup Circuitry

When the power is turned on, the input rectified voltage V_{DC} charges the hold-up capacitor C1 via a startup resistor R_{IN}. R_{IN} can be connected to the VIN or VDD pin directly. As the voltage of VDD pin reaches the start threshold voltage $V_{DD\text{-}ON}$, the SG5841 activates and drives the entire power supply to work.

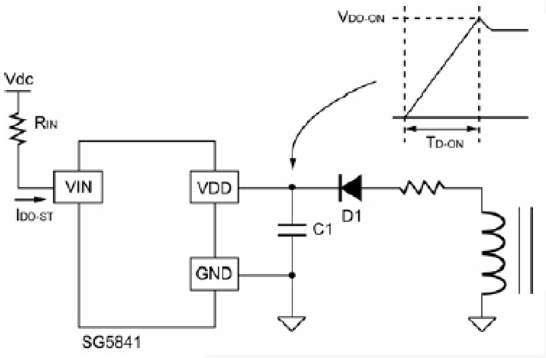

Figure 3. Single-Step Circuit Providing Power

The maximum power-on delay time is determined as:

$$V_{DD-ON} = (V_{DC} - I_{DD-ST} \bullet R_{IN})\left[1 - e^{-\frac{t_{D-ON}}{R_{IN}\bullet C1}}\right] \qquad (1)$$

where:

$I_{DD\text{-}ST}$ is the startup current of the SG5841; $t_{D\text{-}ON}$ is the power-on delay of the power supply.

Due to the low startup current, a large R_{IN}, such as 1.5MΩ, can be used. With a hold-up capacitor of 4.7µF, the power-on delay t_{D_ON} is less than 3.3s for $90V_{AC}$ input.

If a shorter startup time is required, a two-step startup circuit, as shown in Figure 4, is recommended. In this circuit, a smaller C1 capacitor can be used to reduce the startup time without using a smaller startup resistor R_{IN} and increasing the power dissipation on R_{IN}. The energy supporting the SG5841 after startup is mainly from a bigger capacitor C2.

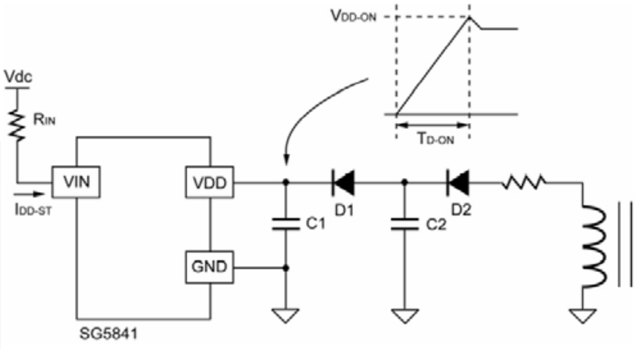

Figure 4. Two-Step Circuit Providing Power

The maximum power dissipation of R_{IN} is:

$$P_{RIN,max} = \frac{(V_{DC,max} - V_{DD})^2}{R_{IN}} \cong \frac{V^2_{DC,max}}{R_{IN}} \qquad (2)$$

where $V_{DC,max}$ is the maximum rectified input voltage.

Take a wide-range input ($90V_{AC}$-$264V_{AC}$) as an example:

V_{DC}=100V~380V

$$P_{RIN,max} = \frac{380^2}{1.5\times10^6} \cong 96\text{mW} \qquad (3)$$

In addition to the low startup current, SG5841 consumes less normal operating current than traditional UC384x.

To achieve a successful startup and keep a no-load input power low enough to meet the power-saving requirements; the voltage level of V_{DD} is recommended to be designed above 12V at no load.

If the voltage of V_{DD} falls below UVLO during "adaptive off-time modulation," the unit enters "hiccup" operation.

Oscillation and Green Mode

Resistor R_I programs the frequency of the internal oscillator. A 26KΩ resistor R_I generates PWM frequency as 65KHz:

$$f_{PWM}(\text{KHz}) = \frac{1690}{R_I(\text{K}\Omega)} \qquad (4)$$

The range of the PWM frequency is recommended between 47KHz ~ 109KHz.

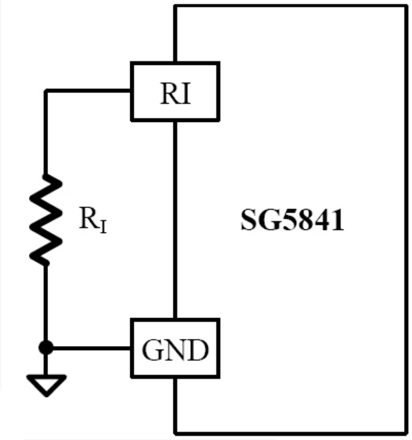

Figure 5. Setting PWM Frequency

The proprietary green mode provides off-time modulation to reduce the PWM frequency at light-load and no-load conditions. The feedback voltage of the FB pin is taken as a reference. When the feedback voltage is lower than ~2.1V, the PWM frequency decreases. Because most losses in a switching-mode power supply are proportional to the PWM frequency, off-time modulation reduces the power consumption of the power supply at light-load and no-load conditions. For a typical case of R_I = 26KΩ, the PWM frequency is 65KHz at nominal load and decreases to 22KHz at light load, about one-third the nominal PWM frequency. The power supply enters "adaptive off-time modulation" in zero-load conditions.

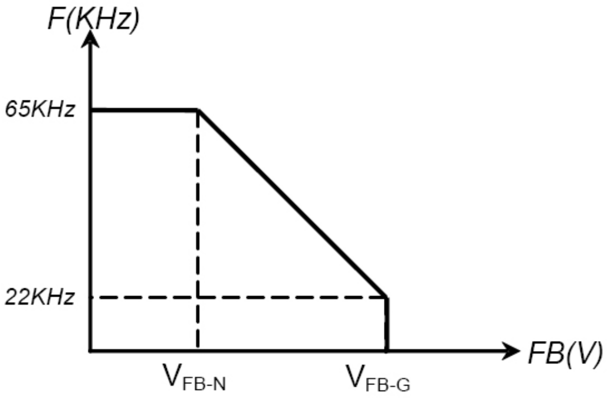

Figure 6. PWM Frequency vs. FB Voltage (R_I=26KΩ)

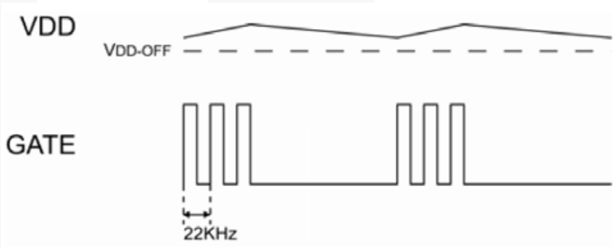

Figure 7. Adaptive Off-Time Modulation

A frequency hopping function improves the system level of EMI performance. The PWM switching frequency hops between 65KHz +/- 4.2KHz, with a hopping period of around 4.4ms (5841J only).

The FB Input

The SG5841 is designed for peak-current-mode control. A current-to-voltage conversion is done externally with a current-sense resistor R_S. Under normal operation, the peak inductor current is controlled by FB level:

$$I_{pk} = \frac{V_{FB} - 1.2}{3 \bullet R_S} \qquad (5)$$

where V_{FB} is the voltage of the FB pin.

When V_{FB} is less than 1.2V, the SG5841 terminates the output pulses.

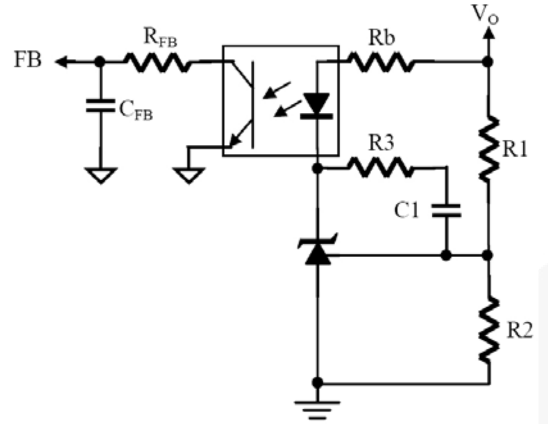

Figure 8. Feedback Circuit

Figure 8 is a typical feedback circuit consisting mainly of a shunt regulator and an opto-coupler. R_1 and R_2 form a voltage divider for the output voltage regulation. R3 and C1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}= 47Ω, C_{FB}= 1nF) from FB to GND can increase stability. The maximum sourcing current of FB pin is 2mA. The phototransistor must be capable of sinking this current to pull FB level down at no load. The value of biasing resistor R_b is determined as:

$$\frac{V_O - V_D - V_Z}{R_b} \bullet K \geq 2mA \tag{6}$$

where:

V_D is the drop voltage of photodiode, about 1.2V;
V_Z is the minimum operation voltage, 2.5V of the shunt regulator; and
K is the current transfer rate (CTR) of the opto coupler.

For and output voltage V_O=5V with CTR=100%, the maximum value of R_b is 650Ω.

Built-in Slope Compensation

A flyback converter can be operated in discontinuous current mode (DCM) or continuous current mode (CCM). There are many advantages to operating the converter in CCM. With the same output power, a converter in CCM exhibits smaller peak inductor current than in DCM. Therefore, a small sized transformer and a low-rating MOSFET can be applied. On the secondary side of the transformer, the rms output current of DCM can be up to twice of CCM. Larger wire gauge and output capacitors with larger ripple current rating are required. DCM operation also results in higher output voltage spikes. A large LC filter has also to be added. Therefore, a flyback converter in CCM achieves better performance with lower component cost.

Despite the above advantages of CCM operation, there is one concern – stability. In CCM operation, the output power is proportional to the average inductor current, while the peak current is controlled. This causes the well-known sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent this oscillation. The SG5841 introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. Therefore, the SG5841 allows design of cost-effective, highly efficient, compact flyback power supplies operating in CCM without adding any external components.

The positive ramp added is:

$$V_{SLOPE} = V_{SL} \bullet D \tag{7}$$

where:
V_{SL}=0.33V;
D=Duty Cycle.

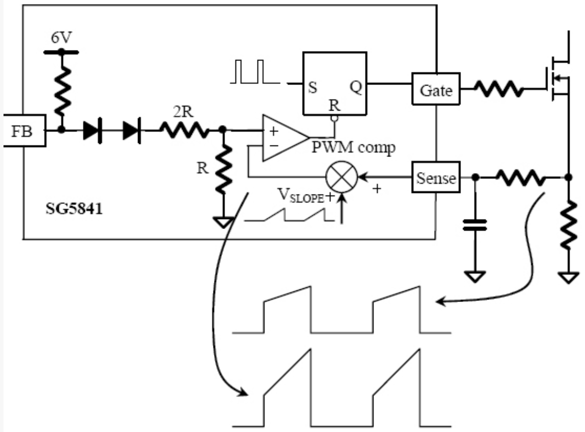

Figure 9. Synchronized Slope Compensation

Leading Edge Blanking (LEB)

A voltage signal proportional to the MOSFET current develops on the current-sense resistor R_S. Each time the MOSFET is turned on, a spike induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, occurs on the sensed signal. A leading-edge blanking time of about 270ns is introduced to avoid premature termination of MOSFET. Therefore, only a small-value RC filter (e.g. 100Ω + 470pF) is required between the SENSE pin and R_S. Still, a non-inductive resistor for the R_S is recommended.

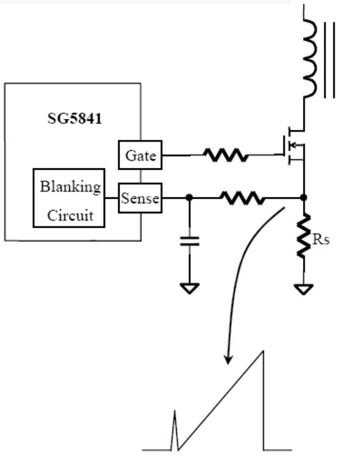

Figure 10. Turn-on Spike

Output Driver / Soft Driving

The output stage is a fast totem-pole gate driver capable of directly driving external MOSFETs. An internal Zener diode clamps the driver voltage under 18V to protect MOSFET's against over voltage. The maximum duty cycle is around 65%. By integrating special circuits to control the slew rate of switch-on rising time, the external resistor R_G may not be necessary to reduce switching noise, improving EMI performance.

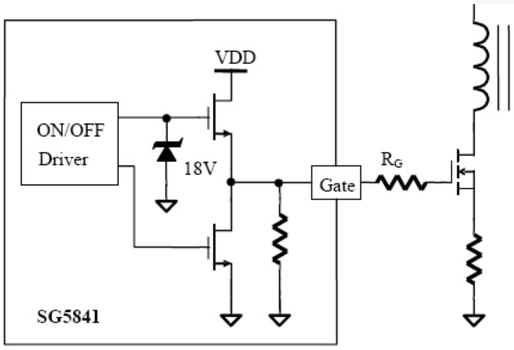

Figure 11. Gate Drive

Constant Output Power Limit

The maximum output power of a flyback converter can generally be determined from the current-sense resistor RS. When the load increases, the peak inductor current increases accordingly. Once the output current arrives at the protection value, the OCP comparator dominates the current control loop. OCP occurs when the current-sense voltage reaches the threshold value. The output GATE driver is turned off after a small propagation delay, t_{PD}. The delay time results in unequal power-limit level under universal input. A sawtooth power-limiter (saw limiter) is designed to solve the unequal power-limit problem. As shown in Figure 12, the saw limiter is designed as a positive ramp signal (V_{LIMIT_RAMP}) and is fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs. However, with fixed propagation delay, tPD, the peak primary current would be the same for various line input voltages; therefore, the maximum output power can practically be limited to a constant value within a wide input voltage range without adding any external circuitry.

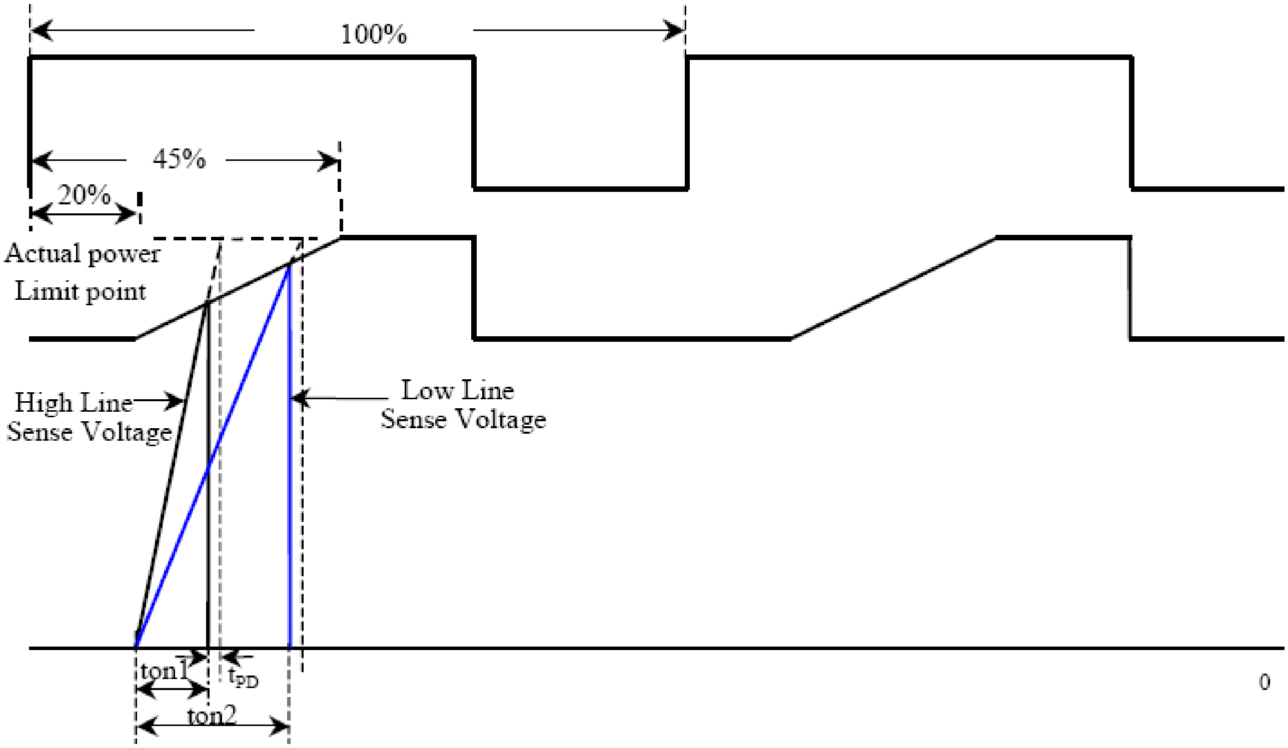

Figure 12. Constant Power Limit Compensation

V_{DD} Over-Voltage Clamping

V_{DD} over-voltage clamping prevents damage due to abnormal conditions. Once the V_{DD} voltage is over the V_{DD} over-voltage clamping voltage ($V_{DD\text{-}CLAMP}$) and lasts for $t_{D\text{-}VDDCLAMP}$, PWM pulses are disabled until V_{DD} drops below the V_{DD} over-voltage clamping voltage.

Thermal Protection

A constant current I_{RT} is provided from pin RT. The resistor connected to pin RI decides its magnitude as:

$$I_{RT} = 100\mu A \bullet \left(26K\Omega / R_I\right) \tag{8}$$

For example,
$I_{RT} = 100\mu A$ if $R_I = 26K\Omega$.

For over-temperature protection, an NTC thermistor RT in series with a resistor R_A can be connected between the RT pin and ground. When V_{RT}, the voltage level of RT pin, is less than 0.62V, PWM output is turned off.

If the thermal protection is not used, connect a small capacitor (around 1nF is recommended) from the RT pin to the GND pin to prevent interference by noise. This RT capacitor cannot be larger than 4.7nF or the thermal protection is triggered before a successful startup of output voltage.

Lab Note

Before rework or solder/desolder on the power supply, discharge primary capacitors by external bleeding resistor; otherwise, the PWM IC may be destroyed by external high-voltage during solder/desolder. This device is sensitive to ESD discharge. To improve production yield, production line should be ESD protected according to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1

Printed Circuit Board Layout

High-frequency switching current/voltage makes printed circuit board layout a very important design issue. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD tests.

Common guidelines:

- To get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C1 first, then to the switching circuits.
- The high-frequency current loop is in **C1 – Transformer – MOSFET – RS – C1**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High-voltage traces related the drain of MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for MOSFET, connect this heatsink to ground.
- As indicated by 3, the ground of control circuits should be connected first, then to other circuitry.
- As indicated by 2, the area enclosed by **transformer aux winding, D1, and C2** should also be kept small. Place C2 close to the SG5841 for good decoupling.

Two suggestions with different pros and cons for ground connections are recommended:

- GND3→2→4→1: This could avoid common impedance interference for sense signals.
- GND3→2→1→4: This could be better for ESD testing where the earth ground is not available on the power supply. The ESD discharge path goes from secondary through the transformer stray capacitance to GND2 first. Then the charges go from GND2 to GND1 and back to mains. It should be noted that control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and increase ESD immunity.
- Should a Y-cap between primary and secondary be required, connect this Y-cap to the **positive terminal of C1 (V_{DC})**. If this Y-cap is connected to the primary GND, it should be connected to the **negative terminal of C1 (GND1)** directly. Point discharge of this Y-cap also helps ESD; however, the creepage between these two pointed ends should be at least 5mm according to safety requirements.

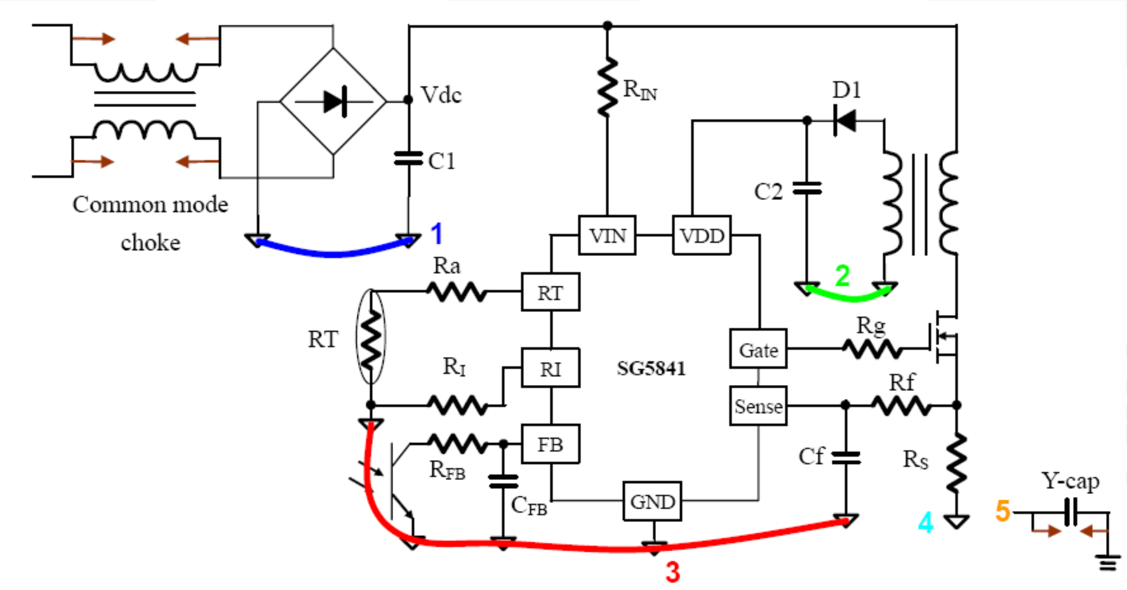

Figure 13. Layout Conciderations

Related Datasheets

SG5841/J — Highly Integrated Green-Mode PWM Controller