

## Terminations for Advanced CMOS Logic

### Introduction

Advanced CMOS logic such as Fairchild Semiconductor's FACT® (Fairchild Advanced CMOS Technology) logic, has extended CMOS performance to the level of advanced bipolar technologies. While high-performance design rules that are currently utilized for bipolar designs are also applicable to CMOS, power consumption becomes a new area of concern in high-performance system designs.

One advantage of using advanced CMOS logic is its low power consumption. However careless circuit design can increase power consumption, possibly by several orders of magnitude. A simple FACT gate typically consumes 625  $\mu\text{W}/\text{MHz}$  of power; at 10 MHz, this translates to 6.25 mW. A 50 $\Omega$  parallel termination on the line will use over 361 mW with a 50% duty cycle.

The use of high-performance system board design guidelines is important when designing with advanced CMOS families. Because of advanced CMOS logic edge rates (less than 3 ns–4 ns), many signal traces will exhibit transmission line characteristics.

A PCB trace begins to act as a transmission line when the propagation delay ( $t_{PD}$ ) across the trace approaches one third of the driver's edge rate. For advanced CMOS, lines

as short as 6 to 8 inches may exhibit these effects. This rule encompasses many traces on a standard PCB. With older CMOS technologies which have lower edge rates, this critical length is much longer: 18 inches for 74HC and 5 feet for CD4000 series and 74C devices. A transmission line terminating into a mismatched impedance could result in transient noise which adversely affects signal integrity.

The FACT family also features guaranteed line driving capability. The  $I_{OLD}/I_{OHD}$  specifications guarantee that a FACT device can drive incident wave voltage steps into line impedances as low as 50 $\Omega$ . The  $I_{OLD}$  specifications do not guarantee incident wave switching into bipolar level inputs since the input low thresholds are 500 mV to 850 mV lower than CMOS. Due to the relatively linear behavior of the outputs below 1V, CMOS devices can drive incident voltages, adequate for bipolar inputs, into line impedances as low as 80 $\Omega$ . For line impedances lower than 80 $\Omega$ , termination can be used to provide adequate input levels. Thus besides reducing noise transients, terminations could also be used to interface between devices from different technologies.

Five possible termination schemes are presented with their impact on power dissipation and noise reduction. Figure 1 illustrates these schemes.

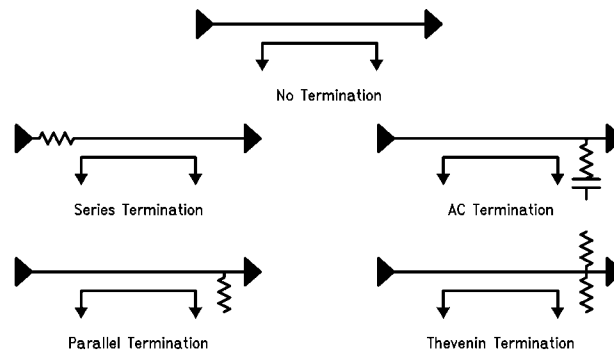


FIGURE 1. Termination Schemes

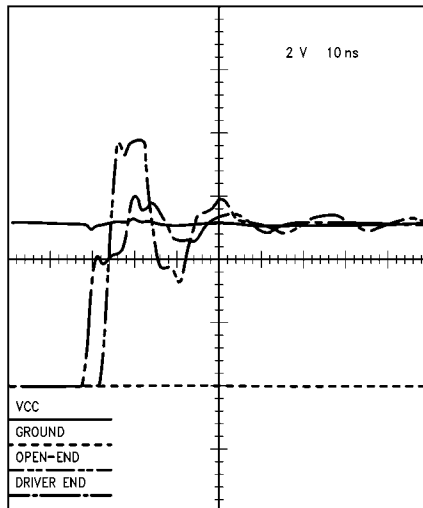
### No Termination

No termination is the lowest cost option and features the easiest design. For line lengths 8 inches or less, this is often the best choice. For lines longer than 8 inches, transmission line effects (line delays and ringing) may exist. Figure 2 illustrates the effect of a FACT device driving a 3-foot open-ended coaxial line. Clamp diodes at the inputs of

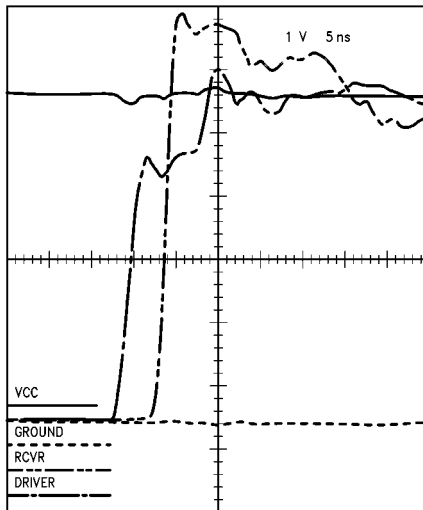
most logic devices tend to reduce the ringing and overshoots. Often, these clamp diodes are sufficient to insure reliable system operation. Figure 3 illustrates the impact of these diodes on the same 3-foot coaxial line. However, it is not uncommon to find logic devices like DRAMs, D-to-A converters and PLDs, that have no input clamp diodes.

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## No Termination (Continued)



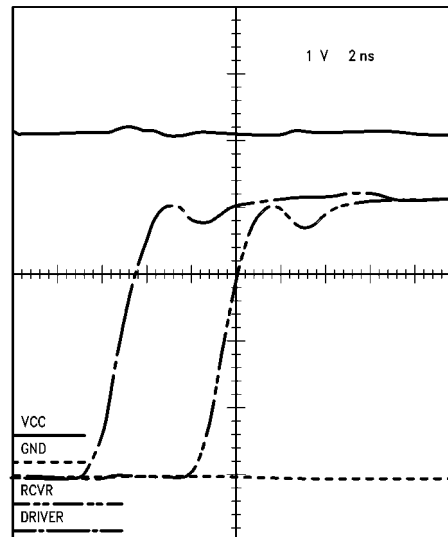
**FIGURE 2. Transmission Line Effects**  
FACT Driving 3 Foot Open-Ended Coax



**FIGURE 3. Effects of Input Clamp Diodes**  
FACT Driving FACT with No Termination

## Parallel Termination

Parallel termination provides an AC and DC current path back to the power supply for switching currents. While it effectively reduces ringing (Figure 4), the DC path to ground or to  $V_{CC}$  will dissipate power. The power consumption for this type of a termination scheme has some important implications. For proper impedance matching the value of this terminating resistor should be equal to the characteristic impedance of the line.



**FIGURE 4. FACT Driving FACT with**  
Parallel Termination

The DC component to the power consumption is a function of the signal duty cycle. Signals with lower duty cycles will dissipate less DC power. Since the load seen by the driving device is resistive, not capacitive, load capacitance does not affect power consumption. Therefore, parallel termination dissipates less AC power. Because of this lower AC power at high frequencies, parallel terminations may consume less power than no termination. Depending upon the load capacitance, signal duty cycle, and line impedance, this frequency can be as low as 40 MHz.

There are drawbacks associated with parallel termination. The maximum DC current allowed into or out of any FACT output is 50 mA. This limits the allowable resistor values to greater than  $100\Omega$ . Even though this ringing may not be excessive, imperfect impedance matching may cause ringing on lines with an impedance less than  $100\Omega$ . However, because the high-power dissipation of this termination scheme negates the advantages of advanced CMOS logic, this is not an intended advanced CMOS application.

Parallel termination tends to unbalance CMOS outputs. Using a resistor to ground, the CMOS device will achieve a 0.0V output low voltage ( $V_{OL}$ ). But due to the high DC load in the logic HIGH state, the output high voltage ( $V_{OH}$ ) will be degraded (Figure 4). This degraded high level output will be above the input high voltage ( $V_{IH}$ ) of both CMOS and bipolar inputs due to the guaranteed dynamic current ( $V_{OHD}$ ) specifications (75 mA @ 3.85V,  $V_{CC} = 5.5V$ ). This lower  $V_{OH}$  level may cause an increase in  $I_{CC}$  if the driven device is CMOS; however, this increase should be minimal.

## Thevenin Termination

Thevenin termination is similar to parallel termination, except that both pull-up and pull-down resistors are used. Power consumptions are also similar for both of these schemes. The difference is that the DC power consumption is a function of duty cycle and resistor ratios. If the resistors are matched, DC power consumption is not dependent upon duty cycle. One advantage Thevenin termination has over parallel termination is that lines with impedances as low as  $50\Omega$  can be terminated in their characteristic impedances. For proper impedance matching, the equivalent thevenin resistance should be the same as the line characteristic impedance.

Thevenin termination does not create unbalanced CMOS outputs, although it reduces the output swing (Figure 5). This limited output swing may increase current consumption in a driven CMOS device however this increase is minimal.

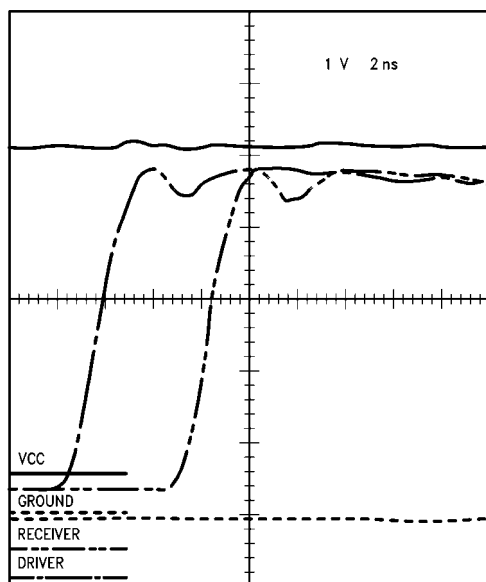


FIGURE 5. FACT Driving FACT with Thevenin Termination

Busses using Thevenin termination should not be left floating. A floating bus level is determined by the ratio of the resistors. If this level is close to any input threshold, output oscillations and  $I_{CC}$  increase may occur. If the bus must be left floating, the resistor ratio should be chosen so that an adequate noise margin is insured. The bus could be left floating by either turning off the driver or by placing the bus in a high impedance state.

Other terminations which do not introduce DC current paths may be more suitable to CMOS systems. These include series and AC parallel terminations.

## Series Termination

Series termination works by limiting the current that is put into a line. While other termination circuits dissipate extra power, series termination reduces power consumption and dissipates less energy than no termination. This is a recommended termination scheme for the FACT family because of its low power dissipation.

Series termination assumes that any voltage step driven into a transmission line will double at the receiver. Therefore, the initial voltage step driven into the line is one-half of the receiver input voltage. The resistor value can be computed by  $R_S = Z_O - R_D$ , where  $R_S$  is the resistor value,  $Z_O$  is the line impedance and  $R_D$  is the driver resistance. Figure 6 illustrates the waveforms associated with series termination.

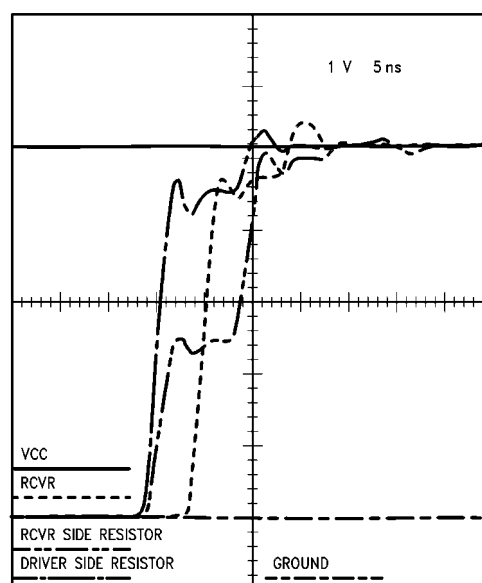


FIGURE 6. FACT Driving FACT with Series Termination

While the device output produces a full output step, only half of that is driven into the line. At the receiver end, the edge doubles, thus recreating the full output swing. The initial step then reflects back, fixing the full output voltage applied on the entire line. A voltage plateau is created at the input to the line whose width will be twice the line  $t_{pd}$ .

Series termination is well suited for lines with a single driver receiver pair. Series termination limits the initial voltage step, which offers several benefits: reduced power consumption and decreased cross-coupled radiated noise.

One possible drawback to series termination is that any other receiver located near the driver will see the voltage plateau. Because the plateau level may be very close to the typical CMOS threshold (50% of  $V_{CC}$ ), any such input could see multiple input switching. Combinatorial outputs may oscillate, or clocked inputs may experience multiple clocking.

One solution is to choose the resistor value that keeps the initial voltage step away from the input thresholds. Larger resistor values will require one or more reflections to settle out, while still maintaining valid  $V_{IN}$  levels at the inputs. Smaller values will generate overshoot and undershoot.

## AC Parallel Termination

AC Parallel termination is another technique which blocks the DC path to ground. A capacitor in series with the parallel termination resistor blocks the DC path, while maintaining the AC path. This is a highly recommended termination scheme for the FACT family because of its negligible DC power consumption.

After the initial voltage step, the capacitor will charge up to the rail voltage at a rate determined by the RC time constant of the circuit (Figure 7).

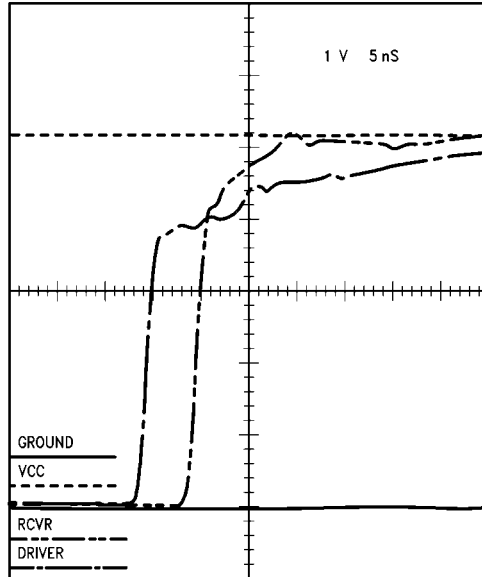


FIGURE 7. FACT Driving FACT with AC Termination

The capacitor value needs to be carefully determined. If the RC time constant is too small, the RC circuit will act as an edge generator and will create overshooting and undershooting. While increasing the capacitor reduces overshoot, it also increases power consumption. As a rule, the RC time constant should be greater than 3 times the line delay.

When driving TTL-level inputs, the same threshold concerns arise as with no termination. The  $I_{OLD}$  current specifications guarantee incident wave switching into CMOS inputs on line impedances as low as  $50\Omega$ . For TTL-level inputs, this minimum line impedance rises to  $80\Omega$ . When the line impedance is less than  $80\Omega$ , a termination value greater than the line impedance will increase the amplitude of the initial voltage step; this can be used to guarantee

incident wave switching into both TTL and CMOS-level inputs. Large resistor values will cause ringing on the line, but the amplitude should be small and not present any problems.

At lower frequencies, this termination capacitance increases the total signal trace impedance; therefore, it also increases the slope of the power consumption curve. At higher frequencies, the capacitor is unable to fully charge or discharge, and the slope of the curve falls off. At very high frequencies, AC parallel termination acts like a parallel resistor tied to an intermediate voltage supply, with the voltage level determined by the signal duty cycle. The slope of the power consumption curve is dependent on  $C_{PD}$  (Power dissipation capacitance) of the device. The power crossover point between no termination and AC termination may be as low as 15 MHz, depending upon the system capacitive loading and the signals' duty cycle.

## Power Consumption

The use of one of these termination schemes will affect the power consumption of the system. Power consumption depends upon the circuit used, signal frequency, device and signal trace loads, signal duty cycle, system  $V_{CC}$  and component values.

Figure 8 shows the power consumption of each type of termination circuit over a frequency range. For low frequency signals, termination circuits without DC components will usually use less power (no termination, series termination and AC parallel termination). At higher frequencies, parallel termination or AC termination may consume less power because of lower AC power consumption. The AC power consumption of these two termination schemes is a function of the device  $C_{PD}$ , while the AC power consumption of the other termination schemes is a function of both the device  $C_{PD}$  and the system capacitive loading ( $C_L$ ). The AC power consumption of AC parallel termination at low frequencies also includes the termination capacitance. The signal used for these curves has a 50% duty cycle. The DC power consumption of the parallel termination will drop as duty cycles drops. For very low duty cycle signals, this scheme may consume the least amount of power.

For low frequencies, the slope of the AC parallel termination curve is greater than any other. This is because it is a function of the device  $C_{PD}$ , the capacitive loading ( $C_L$ ), and the termination capacitance ( $C_T$ ). But at higher frequencies where the pulse width is less than the RC time constant, the slope drops off. At some frequency less than that of parallel termination, AC parallel termination will use less power than using no termination. At some higher frequency, this circuit uses less power than series termination.

## Summary

With new advanced CMOS logic families, power consumption has become an important issue in high-performance systems. Because of the need to use termination, system designers need to be aware of how these circuits affect the power consumption of their systems. The power consumption of the termination scheme will vary, depending upon frequency, duty cycle, line impedance, loading and other factors (Figure 8).

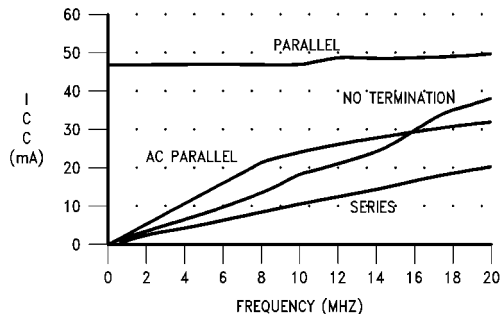


FIGURE 8. Power Consumption

Power consumption is not the only concern when choosing a termination circuit. Part-count and board space are also important concerns. It is up to system designers to choose which, if any, termination circuit is best suited to their circuit. Table 1 shows the recommended values for the various termination schemes. It is highly recommended that the designer use these values as a starting point and adapt it for the most feasible and optimum results.

TABLE 1. Recommended Termination Values

• Parallel:	Resistor = $Z_0$
• Thevenin:	Resistor = $2 \times Z_0$
• Series:	Resistor = $Z_0 - Z_{OUT}$
• AC:	Resistor = $Z_0$
	Capacitor = $C \geq \frac{3td}{Z_0}$
• Active:	Resistor = $2 \times Z_0$

For additional information on terminations, refer to these Fairchild Semiconductor publications.

1. FAST Applications Handbook, 1987.
2. F100K ECL User's Handbook, 1986.

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