

AN-6861

Applying FAN6861 to a Flyback Power Supply with Peak Load Current Profile

1. Introduction

Highly integrated PWM controller, FAN6861, is optimized for applications with motor load, such as printers and scanners, that inherently impose some kind of overload condition on the power supply during acceleration mode. The two-level OCP function allows the SMPS to stably deliver peak power during the motor acceleration without causing premature shutdown, while protecting the SMPS from overload condition.

The green-mode and burst-mode functions with a low operating current (2.2mA maximum in green mode) maximize the light-load efficiency so that the power supply can meet stringent standby power regulations.

The frequency-hopping function reduces electro-magnetic interference (EMI) of a power supply by spreading the energy over a wider frequency range. The constant power limit function minimizes the component stress in abnormal condition and helps to optimize the power stage. Protection functions; such as OCP, OLP, OVP, and OTP are fully integrated into FAN6861, which improves the SMPS reliability without increasing system cost.

This application note presents design considerations to apply FAN6861 to a flyback power supply with peak load current profile. It covers designing the transformer, selecting the components, and closing the feedback loop. Figure 1 shows a typical application circuit using FAN6861.

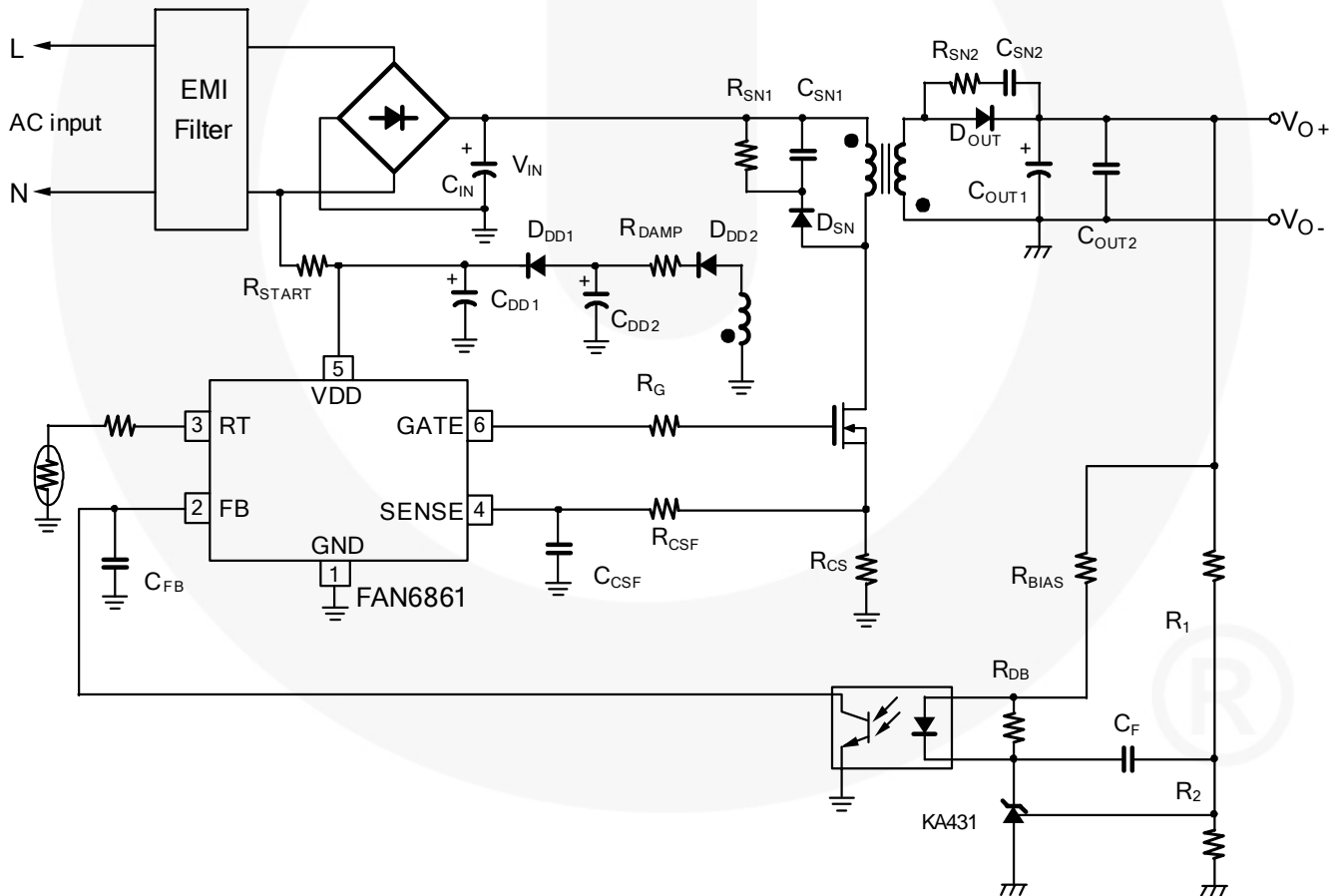


Figure 1. Typical Application

2. Design Considerations

Flyback converters have two operation modes; continuous conduction mode (CCM) and discontinuous conduction mode (DCM). CCM and DCM have their own advantages and disadvantages, respectively. In general, DCM provides better switching conditions for the rectifier diodes, since the diodes are operating at zero current just before becoming reverse biased and the reverse recovery loss is minimized. The transformer size can be reduced using DCM because the average energy storage is low compared to CCM. However, DCM inherently causes high RMS current, which increases the conduction loss of the MOSFET severely for low line condition. Thus, especially for applications with peak load profile, such as printer and scanner; it is typical to design the converter such that the converter operates in CCM for low line and peak load condition to maximize efficiency.

In this section, a design procedure is presented using the schematic of Figure 1 as a reference. An off line SMPS with 20W/32V nominal output power and 50W/32V peak output power has been selected as a design example.

[STEP-1] Define the System Specifications

Designing a power supply with peak load current profile, the following specifications should be determined first:

- Line voltage range (V_{LINE}^{MIN} and V_{LINE}^{MAX})
- Line frequency (f_L).
- Nominal output power (P_{NO})
- Peak output power (P_{PO}) and its duration (t_{PO})
- Estimated efficiencies for nominal load (η_N) and peak load (η_P): The power conversion efficiency must be estimated to calculate the input powers for each condition. Typically, the efficiency at peak load condition is lower than that of nominal load since most of the components of power supply are selected for nominal load condition. If no reference data is available, set $\eta_N = 0.7\sim 0.75$ and $\eta_P = 0.65\sim 0.7$ for low-voltage output applications and $\eta_N = 0.8\sim 0.85$ and $\eta_P = 0.75\sim 0.8$ for high-voltage output applications.

With the estimated efficiency, the input power for peak load condition is given by:

$$P_{INP} = \frac{P_{PO}}{\eta_P} \quad (1)$$

The input power for nominal load condition is given by:

$$P_{INN} = \frac{P_{NO}}{\eta_N} \quad (2)$$

(Design Example) The specifications of the target system are:

- $V_{LINE}^{MIN} = 90V_{RMS}$ $V_{LINE}^{MAX} = 264V_{RMS}$
- Line frequency (f_L) = 60Hz
- Nominal output power (P_{NO}) = 20W (32V/0.625A)
- Peak output power (P_{PO}) = 50W (32V/1.56A)
- Peak load duration (t_{PO}) < 500ms
- Estimated efficiency: $\eta_N = 0.87$ and $\eta_P = 0.82$

$$P_{INP} = \frac{P_{PO}}{\eta_P} = \frac{50}{0.82} = 61W$$

$$P_{INN} = \frac{P_{NO}}{\eta_N} = \frac{20}{0.87} = 23W$$

FAN6861 can be used for this application because the peak load duration is less than the OCP delay time of 780ms.

[STEP-2] Determine the Input Capacitor (C_{IN}) and the Input Voltage Range

It is typical to select the input capacitor as 1.5~2 μ F per watt of peak input power for universal input range (85~265 V_{RMS}) and 0.7~0.8 μ F per watt of peak input power for European input range (195V~265 V_{RMS}). With the input capacitor chosen, the minimum input capacitor voltage at peak load condition is obtained as:

$$V_{INP}^{MIN} = \sqrt{2 \cdot (V_{LINE}^{MIN})^2 - \frac{P_{INP} \cdot (1 - D_{CH})}{C_{IN} \cdot f_L}} \quad (3)$$

The minimum input capacitor voltage at nominal load condition is obtained as:

$$V_{INN}^{MIN} = \sqrt{2 \cdot (V_{LINE}^{MIN})^2 - \frac{P_{INN} \cdot (1 - D_{CH})}{C_{IN} \cdot f_L}} \quad (4)$$

where D_{CH} is the input capacitor charging duty ratio defined as shown in Figure 2, which is typically about 0.2.

The maximum input capacitor voltage is given as

$$V_{IN}^{MAX} = \sqrt{2} V_{LINE}^{MAX} \quad (5)$$

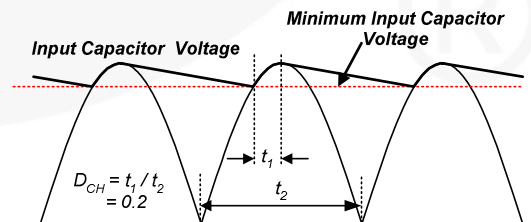


Figure 2. Input Capacitor Voltage Waveform

(Design Example) By choosing a 100 μ F capacitor for the input capacitor, the minimum input voltages for peak and nominal load are obtained, respectively, as:

$$V_{INP}^{MIN} = \sqrt{2 \cdot (V_{LINE}^{MIN})^2 - \frac{P_{INP} \cdot (1 - D_{CH})}{C_{IN} \cdot f_L}}$$

$$= \sqrt{2 \cdot (90)^2 - \frac{61 \cdot (1 - 0.2)}{100 \times 10^{-6} \cdot 60}} = 90V$$

$$V_{INN}^{MIN} = \sqrt{2 \cdot (V_{LINE}^{MIN})^2 - \frac{P_{INN} \cdot (1 - D_{CH})}{C_{IN} \cdot f_L}}$$

$$= \sqrt{2 \cdot (90)^2 - \frac{23 \cdot (1 - 0.2)}{100 \times 10^{-6} \cdot 60}} = 115V$$

The maximum input voltage is obtained as

$$V_{IN}^{MAX} = \sqrt{2} \cdot V_{LINE}^{MAX} = \sqrt{2} \cdot 264 = 373V$$

[STEP-3] Determine the Reflected Output Voltage (V_{RO})

When the MOSFET is turned off, the input voltage (V_{IN}), together with the output voltage reflected to the primary, (V_{RO}) are imposed across the MOSFET, as shown in Figure 3. With a given V_{RO} , the maximum duty cycle (D_{MAX}) and the maximum nominal MOSFET voltage (V_{DS}^{NOM}) are obtained as:

$$D_{MAX} = \frac{V_{RO}}{V_{RO} + V_{INP}^{MIN}} \quad (6)$$

$$V_{DS}^{NOM} = V_{IN}^{MAX} + V_{RO} \quad (7)$$

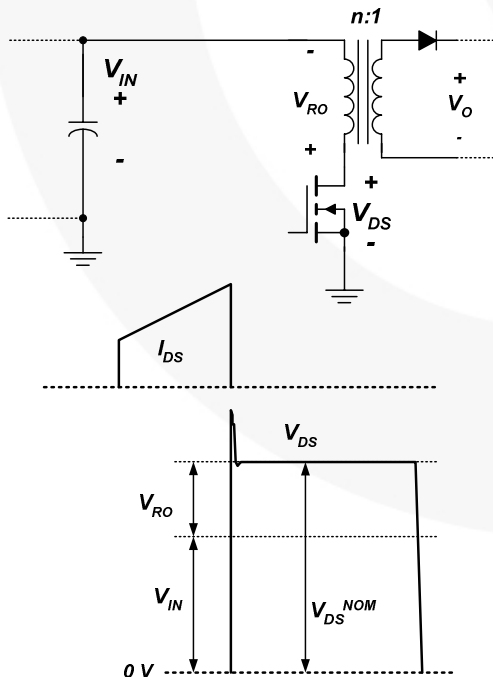


Figure 3. The Output Voltage Reflected to the Primary

As can be seen in Equation (7), the voltage stress across the MOSFET can be reduced by reducing V_{RO} . However, this increases the voltage stresses on the rectifier diodes in the secondary side. Therefore, V_{RO} should be determined by a trade-off between the voltage stresses of MOSFET and diode. Because the actual drain voltage rises above the nominal MOSFET voltage due to the leakage inductance of the transformer, as shown in Figure 3, it is typical to set V_{RO} around 70~100V so that V_{DS}^{NOM} is 430~450V for 600V MOSFET (73~78% of MOSFET voltage rating).

(Design Example) By determining V_{RO} as 100V:

$$D_{MAX} = \frac{V_{RO}}{V_{RO} + V_{INP}^{MIN}} = \frac{100}{100 + 90} = 0.53$$

$$V_{DS}^{NOM} = V_{IN}^{MAX} + V_{RO} = 273 + 100 = 473V$$

[STEP-4] Determine the Transformer Primary-Side Inductance (L_M)

The transformer primary-side inductance is determined for the minimum input voltage and peak load condition. With the D_{MAX} from Step-3, the primary-side inductance (L_M) of the transformer is obtained as

$$L_M = \frac{(V_{INP}^{MIN} \cdot D_{MAX})^2}{2P_{INP} f_{SW} K_{RF}} \quad (8)$$

where f_{SW} is the switching frequency and K_{RF} is the ripple factor at peak load and minimum input voltage condition, as shown in Figure 4.

The ripple factor is closely related to the transformer size and the RMS value of the MOSFET current. Even though the conduction loss in the MOSFET can be reduced by reducing the ripple factor, too small a ripple factor forces an increase in transformer size. From practical point of view, it is reasonable to set $K_{RF} = 0.3\sim 0.6$ for the universal input range and $K_{RF} = 0.4\sim 0.8$ for the European input range.

Once L_M is calculated by determining K_{RF} from Equation (8), the peak current and RMS current of the MOSFET for minimum input voltage and peak load condition are obtained as:

$$I_{DS}^{PK} = I_{EDC} + \frac{\Delta I}{2} \quad (9)$$

$$I_{DS}^{RMS} = \sqrt{\left[3(I_{EDC})^2 + \left(\frac{\Delta I}{2}\right)^2 \right] \frac{D_{MAX}}{3}} \quad (10)$$

where:
$$I_{EDC} = \frac{P_{INP}}{V_{INP}^{MIN} \cdot D_{MAX}} \quad (11)$$

and
$$\Delta I = \frac{V_{INP}^{MIN} D_{MAX}}{L_M f_{SW}} \quad (12)$$

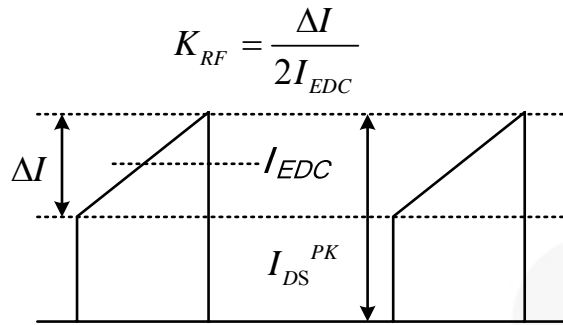


Figure 4. MOSFET Current and Ripple Factor (K_{RF})

(Design Example) Determining the ripple factor as 0.57

$$L_M = \frac{(V_{INP}^{MIN} \cdot D_{MAX})^2}{2P_{INP} f_{SW} K_{RF}} = \frac{(90 \cdot 0.53)^2}{2 \cdot 61 \cdot 65 \times 10^3 \cdot 0.57} = 503 \mu H$$

$$I_{EDC} = \frac{P_{INP}}{V_{INP}^{MIN} \cdot D_{MAX}} = \frac{61}{90 \cdot 0.53} = 1.28 A$$

$$\Delta I = \frac{V_{INP}^{MIN} D_{MAX}}{L_M f_{SW}} = \frac{90 \cdot 0.53}{503 \times 10^{-6} \cdot 65 \times 10^3} = 1.46 A$$

$$I_{DS}^{PK} = I_{EDC} + \frac{\Delta I}{2} = 1.28 + 0.73 = 2.01 A$$

$$I_{DS}^{RMS} = \sqrt{\left[3(I_{EDC})^2 + \left(\frac{\Delta I}{2}\right)^2 \right] \frac{D_{MAX}}{3}} = \sqrt{\left[3(1.28)^2 + (0.73)^2 \right] \frac{0.53}{3}} = 0.98 A$$

[STEP-5] Determine the Sensing Resistor Value

The current sensing resistor value should be determined considering the over-current protection threshold and the pulse-by-pulse current limit threshold, as shown in Figure 5. The peak value of current sensing voltage (V_{CS}) should be lower than the pulse-by-pulse current limit level for peak load condition. It should be lower than the OCP threshold for nominal load conditions to prevent false triggering of OCP protection during normal operation.

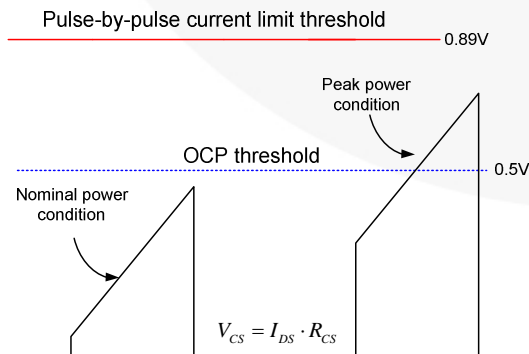


Figure 5. Determining Current Sensing Resistor

The peak drain current at minimum input voltage and peak load condition was obtained from Equation (9) in Step-4. The peak drain current at minimum input voltage and nominal load condition is given as:

$$I_{DS.N}^{PK} = \frac{P_{INN} \cdot (V_{IN}^{MIN} + V_{RO})}{V_{INN}^{MIN} \cdot V_{RO}} + \frac{V_{INN}^{MIN} \cdot V_{RO}}{2L_M f_{SW} \cdot (V_{INN}^{MIN} + V_{RO})} : CCM \quad (13)$$

$$I_{DS.N}^{PK} = \sqrt{\frac{2 \cdot P_{INN}}{f_{SW} \cdot L_M}} : DCM \quad (14)$$

Whether the converter operates in CCM or DCM at minimum input voltage and nominal load condition is determined by:

$$\sqrt{2P_{INN} L_M f_{SW}} \cdot \frac{(V_{INN}^{MIN} + V_{RO})}{V_{INN}^{MIN} \cdot V_{RO}} > 1 : CCM \quad (15)$$

$$\sqrt{2P_{INN} L_M f_{SW}} \cdot \frac{(V_{INN}^{MIN} + V_{RO})}{V_{INN}^{MIN} \cdot V_{RO}} < 1 : DCM$$

The condition for the sensing resistor is given as:

$$R_{CS} < \frac{0.5}{I_{DS.N}^{PK}} \quad (16)$$

$$R_{CS} < \frac{0.89}{I_{DS}^{PK}}$$

(Design Example) For minimum input voltage and nominal load condition, the operation mode is DCM as:

$$\sqrt{2P_{INN} L_M f_{SW}} \cdot \frac{(V_{INN}^{MIN} + V_{RO})}{V_{INN}^{MIN} \cdot V_{RO}} = \sqrt{2 \cdot 23 \cdot 503 \times 10^{-6} \cdot 65 \times 10^3} \cdot \frac{(115 + 100)}{115 \cdot 100} < 1$$

The peak drain current at minimum input voltage and nominal power condition is given as:

$$I_{DS.N}^{PK} = \sqrt{\frac{2 \cdot P_{INN}}{f_{SW} \cdot L_M}} = \sqrt{\frac{2 \cdot 23}{65 \times 10^3 \cdot 503 \times 10^{-6}}} = 1.19 A$$

The conditions for the sensing resistor are given as:

$$R_{CS} < \frac{0.5}{I_{DS.N}^{PK}} = \frac{0.5}{1.19} = 0.42 \Omega$$

$$R_{CS} < \frac{0.89}{I_{DS.P2}^{PK}} = \frac{0.89}{2.01} = 0.44 \Omega$$

Thus, a 0.39Ω resistor is selected for the current-sensing resistor

[STEP-6] Determine the Minimum Primary Turns

With a given core, the minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_P^{\min} = \frac{L_M I_{LIM}}{B_{SAT} A_e} \times 10^6 = \frac{L_M \cdot 0.89 / R_{CS}}{B_{SAT} A_e} \times 10^6 \quad (17)$$

where A_e is the cross-sectional area of the core in mm^2 , I_{LIM} is the pulse-by-pulse current limit level determined by 0.89V threshold, R_{CS} is current sensing resistor, and B_{SAT} is the saturation flux density in Tesla.

The pulse-by-pulse current limit level is included in Equation (17) because the inductor current reaches the pulse-by-pulse current limit level during the load transient or overload condition. Figure 6 shows the typical characteristics of ferrite core from TDK (PC40). Since the saturation flux density (B_{SAT}) decreases as the temperature goes high, the high temperature characteristics should be considered. If there is no reference data, use $B_{MAX}=0.3\text{T}$.

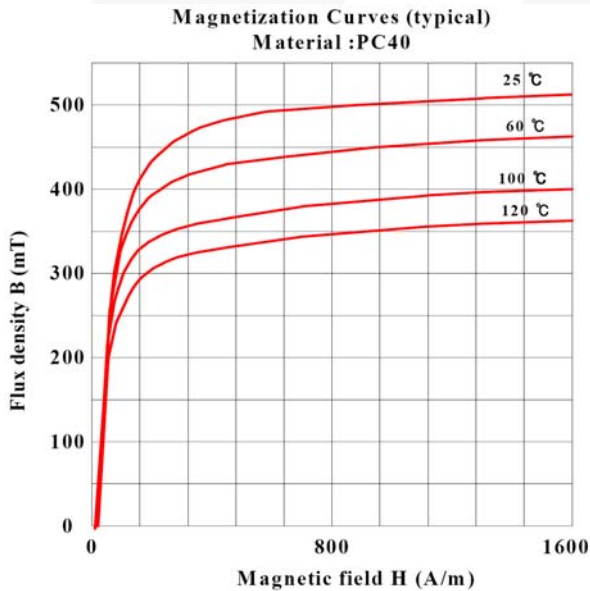


Figure 6. Typical B-H Characteristics of Ferrite Core (TDK/PC40)

(Design Example) A EF25/13/11 core is selected, whose effective cross-sectional area is 78mm^2 . Choosing the saturation flux density as 0.25T, the minimum number of turns for the primary side is obtained as:

$$\begin{aligned} N_P^{\min} &= \frac{L_M \cdot 0.89 / R_{CS}}{B_{SAT} A_e} \times 10^6 \\ &= \frac{503 \times 10^{-6} \cdot 0.89 / 0.39}{0.25 \cdot 78} \times 10^6 = 59 \end{aligned}$$

[STEP-7] Determine the Number of Turns for Each Winding

Figure 7 shows a simplified diagram of the transformer. First, calculate the turn ratio (n) between the primary side and the secondary side from the reflected output voltage determined in Step-3, as:

$$n = \frac{N_P}{N_S} = \frac{V_{RO}}{V_O + V_F} \quad (18)$$

where N_P and N_S are the number of turns for primary side and secondary side, respectively, V_O is the output voltage; and V_F is the diode (D_O) forward-voltage drop. Then, determine the proper integer for N_S such that the resulting N_P is larger than N_P^{\min} obtained from Equation (17).

The number of turns for the auxiliary winding for V_{DD} supply is determined as:

$$N_A = \frac{V_{DD}^* + V_F}{V_O + V_{FA}} \cdot N_{S1} \quad (19)$$

where V_{DD} is the nominal value of the supply voltage and V_{FA} is the forward voltage drop of D_{DD} as defined in Figure 7. Since V_{DD} increases as the output load increases, it is proper to set V_{DD} at 3~5V higher than V_{DD} UVLO level (9.5V) to avoid the over-voltage protection condition during the peak load operation.

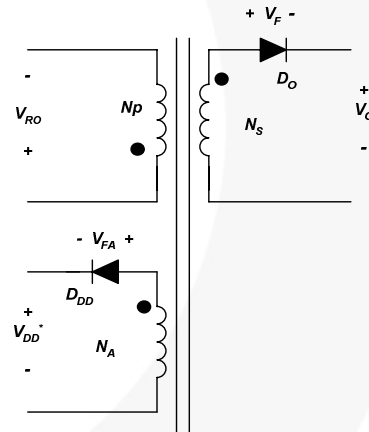


Figure 7. Simplified Transformer Diagram

(Design Example) Assuming the diode forward-voltage drop is 1V, the turn ratio is obtained as:

$$n = \frac{N_P}{N_S} = \frac{V_{RO}}{V_O + V_F} = \frac{100}{32 + 1} = 3.03$$

Then, determine the proper integer for N_S such that the resulting N_P is larger than N_P^{\min} as:

$$N_S = 20, N_P = n \cdot N_S = 61 > N_P^{\min}$$

Setting V_{DD}^* as 12.5V, the number of turns for the auxiliary winding is obtained as:

$$N_A = \frac{V_{DD}^* + V_F}{V_O + V_{FA}} \cdot N_S = \frac{12.5 + 1}{32 + 1} \cdot 20 = 8$$

$$\frac{V_O - V_{OPD} - V_{KA}}{R_{BIAS}} \cdot CTR > 325 \times 10^{-6} \quad (26)$$

where V_{OPD} is the drop voltage of photodiode, about 1.2V; V_{KA} is the minimum cathode to anode voltage of shunt regulator (2.5V); and CTR is the current transfer rate of the opto-coupler.

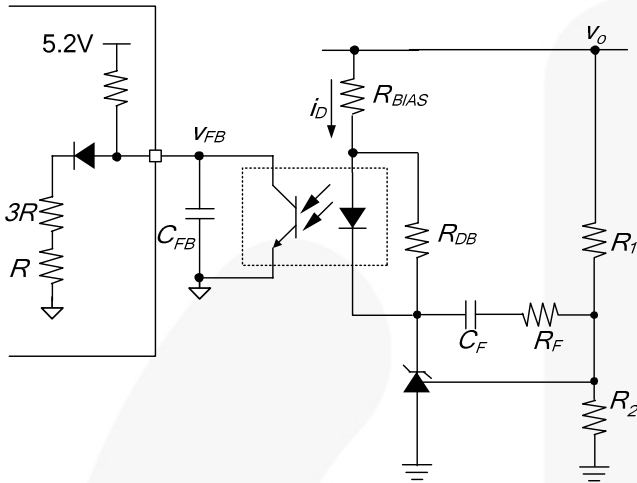


Figure 9. Feedback Circuit

The feedback compensation network transfer function of Figure 9 is obtained as:

$$\frac{\hat{v}_{FB}}{\hat{v}_o} = -\frac{\omega_I}{s} \cdot \frac{1 + s/\omega_{ZC}}{1 + s/\omega_{PC}} \quad (27)$$

$$\text{where } \omega_I = \frac{R_B}{R_1 R_{DB} C_F}, \quad \omega_{ZC} = \frac{1}{(R_F + R_1) C_O}$$

$$\omega_{PC} = \frac{1}{R_B C_{FB}}$$

R_B is the internal feedback bias resistor of FAN6861; and R_I , R_D , R_F , C_F , and C_{FB} are shown in Figure 9.

(Design Example) Assuming CTR is 100%;

$$\frac{V_O - V_{OPD} - V_{KA}}{R_{BIAS}} \cdot CTR > 325 \times 10^{-6}$$

$$R_{BIAS} < \frac{V_O - V_{OPD} - V_{KA}}{325 \times 10^{-6}} = \frac{32 - 1.2 - 2.5}{325 \times 10^{-6}} = 87k\Omega$$

3kΩ resistor is selected for R_{DB} .

The voltage divider resistors for V_O sensing are selected as 120kΩ and 10kΩ.

[STEP-11] Design the Startup Circuit

Figure 10 shows the typical startup circuit for FAN6861. Connecting startup resistor to AC line allows the reset of latch protection by unplugging the AC line from the power supply. Two-stage hold-up capacitor configuration (C_{DD1} and C_{DD2}) is typically used to increase the hold-up time while minimizing the startup time.

Initially, FAN6861 consumes only startup current (maximum 15μA) before it begins normal switching operation. Therefore, the current supplied through the startup resistor (R_{START}) can charge capacitor C_{DD1} while supplying the startup current to FAN6861. When V_{DD} reaches turn-on voltage of 17.5V (V_{DD-ON}), FAN6861 begins switching operation and the current consumed by FAN6861 increases to normal operating current (typical 3mA). Then, the current required by FAN6861 is supplied from the auxiliary winding of transformer.

The average current supplied through the startup resistor for minimum line voltage condition is

$$I_{RST} = \left(\frac{\sqrt{2}V_{LINE}^{MIN}}{\pi} - \frac{V_{DD-ON}}{2} \right) \frac{1}{R_{START}} > I_{DD-ST} \quad (28)$$

$$T_{START}^{MAX} = C_{DD1} \frac{V_{DD-ON}}{I_{RST} - I_{DD-ST}} \quad (29)$$

The maximum power dissipation of R_{START} is:

$$P_{RST} \cong \frac{(V_{LINE}^{MAX})^2}{2R_{START}} \quad (30)$$

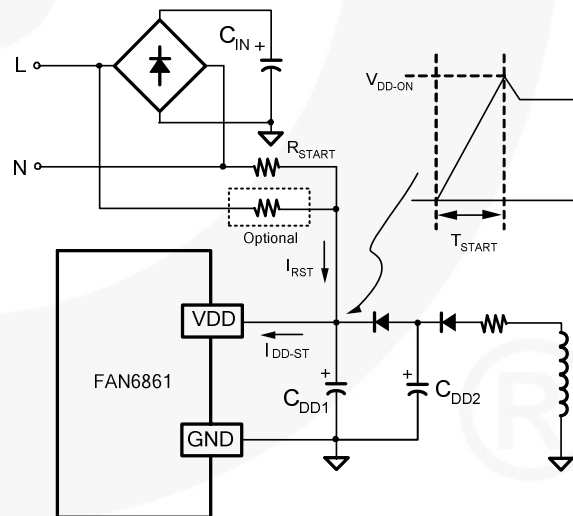


Figure 10. Startup Circuit

(Design Example) 510kΩ resistor and 10μF capacitor are selected for R_{START} and C_{DD1} , respectively. Then, the current through the startup resistor for minimum line voltage is:

$$I_{RST} = \left(\frac{\sqrt{2}V_{LINE}^{MIN}}{\pi} - \frac{V_{DD-ON}}{2} \right) \frac{1}{R_{START}}$$

$$= \left(\frac{\sqrt{2} \cdot 90}{\pi} - \frac{17.5}{2} \right) \frac{1}{510 \times 10^3} = 62 \mu A$$

Then, the maximum startup time is obtained as

$$T_{START}^{MAX} = C_{DD1} \frac{V_{DD-ON}}{I_{RST} - I_{DD-ST}^{MAX}}$$

$$= 10 \times 10^{-6} \frac{17.5}{(62 - 15) \times 10^{-6}} = 3.7 \text{ sec}$$

The maximum power dissipation of R_{START} is:

$$P_{RST} \cong \frac{(V_{LINE}^{MAX})^2}{2R_{START}} = \frac{265^2}{2 \cdot 510 \times 10^3} = 68 \text{ mW}$$

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sense resistor, caused by primary-side capacitance and secondary-side rectifier reverse recovery. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period (360ns), the PWM comparator is disabled and cannot switch off the gate driver. Thus, an RC filter with a small RC time constant is enough for current sensing (e.g. 200Ω + 470pF). A non-inductive resistor is recommended for R_{CS} .

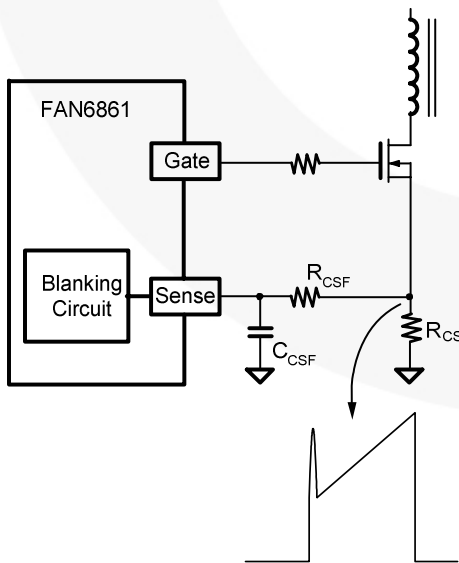


Figure 11. Current sensing

Thermal Protection

Figure 12 shows the internal blocks for thermal protection. A constant current, I_{RT} , of 99μA is provided from the RT pin. For over-temperature protection, an NTC thermistor in series with a resistor can be connected between the RT and GND pins. As temperature increases, the impedance of NTC thermistor decreases and RT pin voltage drops. When the voltage of the RT pin is less than 1V longer than 17ms ($t_{DOTP-LATCH}$), OTP is triggered. When RT pin voltage is less than 0.7V, OTP is triggered after the 100μs debounce time.

If the thermal protection is not used, connect a small capacitor (around 0.47nF is recommended) from the RT pin to the GND pin to prevent noise interference. This RT capacitor should not be larger than 1nF; otherwise, the thermal protection is triggered before a successful build-up of output voltage.

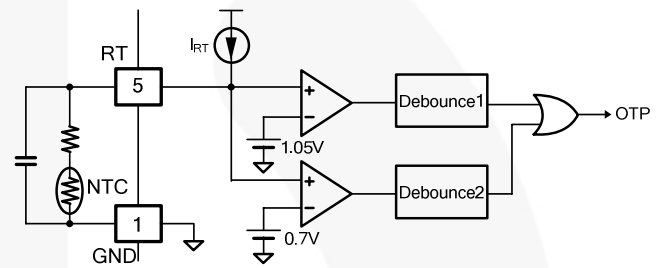


Figure 12. Thermal Protection Circuit

Printed Circuit Board (PCB) Layout

PCB layout is a very important design issue for high-frequency switching current/voltage application. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD tests.

Guidelines:

- To get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C1 first, then to the switching circuits.
- The high-frequency current loop is in **C1 – transformer – MOSFET – R_S – C1**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially **4 → 1**) short, direct, and wide. High-voltage traces related to the drain of MOSFET and RCD snubber should be kept far away from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, connect this heatsink to ground.
- As indicated by **3**, the ground of control circuits should be connected first, then to other circuitry.
- As indicated by **2**, the area enclosed by **transformer auxiliary winding, D1, C2, D2, and C3** should also be kept small. Place C3 close to the FAN6861 for good decoupling.

Two suggestions with different pro and cons for ground connections are offered:

- GND3 → 2 → 4 → 1**: This could avoid common impedance interference for sense signal.
- GND3 → 2 → 1 → 4**: This could be better for ESD testing where the earth ground is not available on the power supply. Regarding the ESD discharge path, the charges go from secondary through the transformer stray capacitance to **GND2** first. The charges then go from **GND2** to **GND1** and back to the mains. Note that control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and increase ESD immunity.
- Should a Y-cap between primary and secondary be required, connect this Y-cap to the **positive terminal of C1**. If this Y-cap is connected to the primary GND, it should be connected to the **negative terminal of C1 (GND1)** directly. Point discharge of this Y-cap also helps for ESD. However, the creepage between these two pointed ends should be large enough to satisfy the requirements of applicable standards.

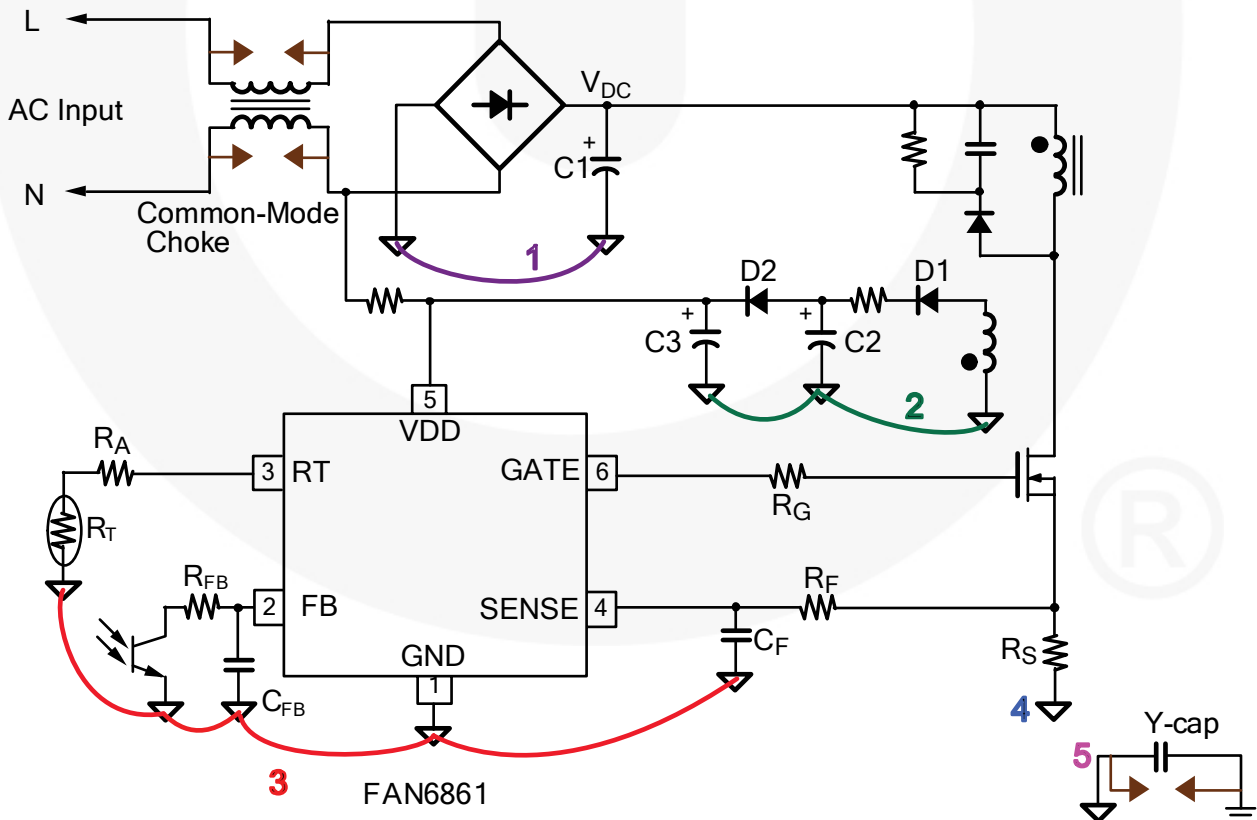


Figure 13. Layout Considerations

Design Summary

Figure 1 shows the final schematic of the 20W (50W peak) power supply of the design example.

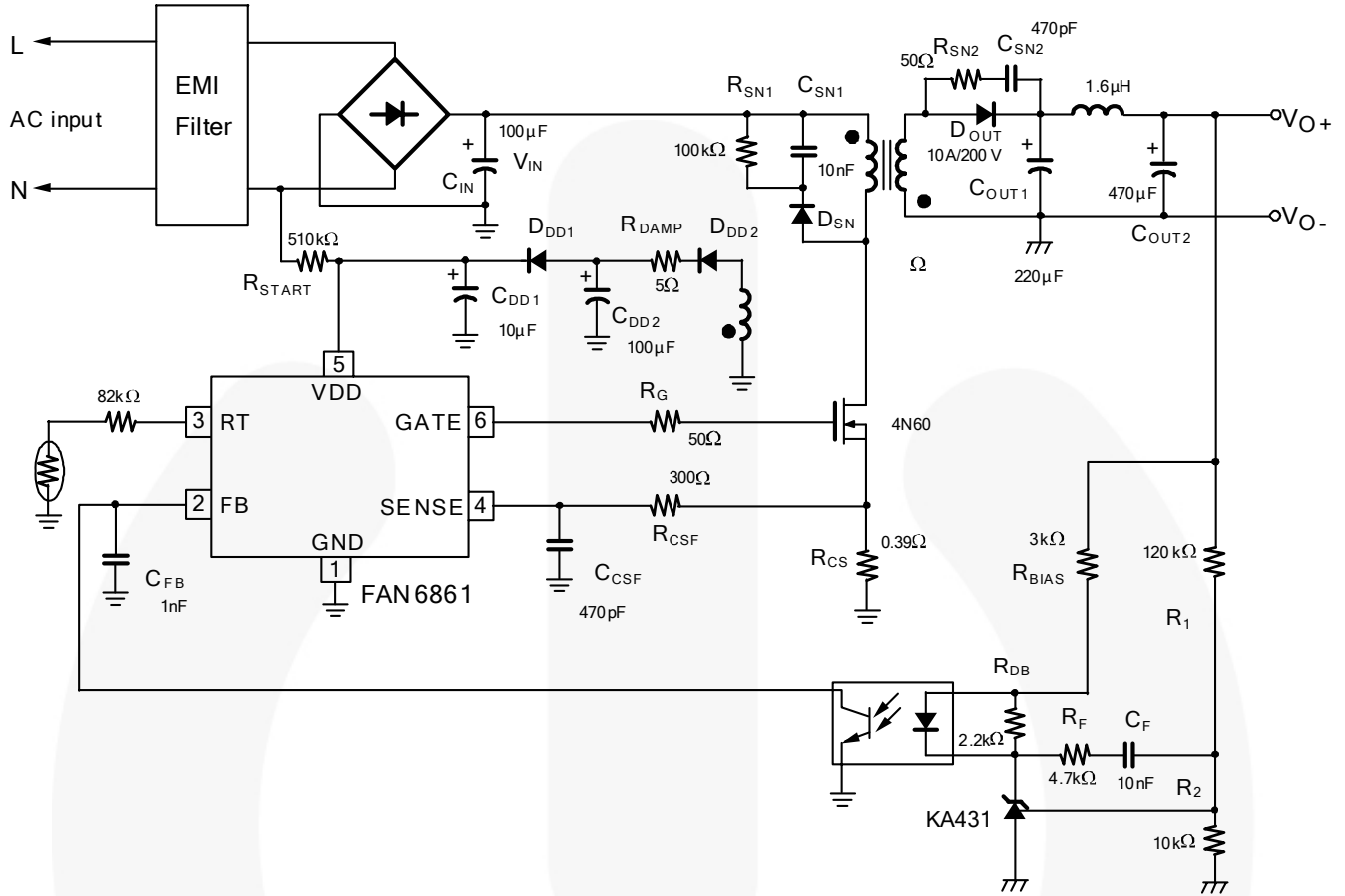


Figure 14. Final Schematic of Design Example

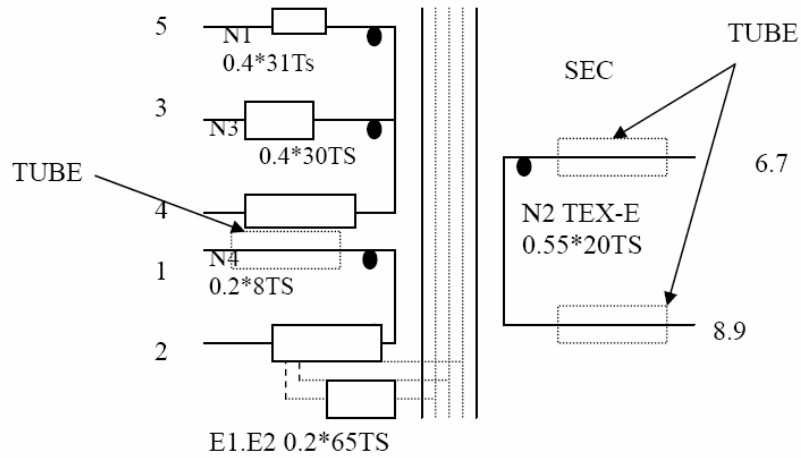


Figure 14.

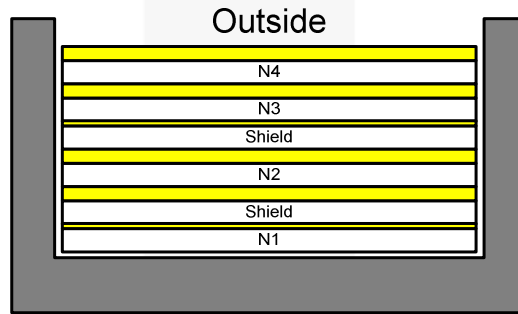


Figure 15. Transformer Specification

Winding Specification

	Pin	Diameter / Thickness	Turns
N1	5 → 3	0.4mm	31
	Insulation Tape		1
	Shielding lead to Pin 2		1
	Insulation Tape		3
N2	6, 7 → 8, 9	0.55mm	20
	Insulation Tape		3
	Shielding lead to Pin 2		1
	Insulation Tape		1
N3	3 → 4	0.4mm	30
	Insulation Tape		3
N4	1 → 2	0.2mm	8
	Insulation Tape		3

Core: EF25/13/11 ($A_e=78 \text{ mm}^2$)
 Bobbin: EF25/13/11
 Inductance: 500 μ H

Related Datasheets

FAN6861 — Low Cost and Highly Integrated Green-Mode PWM Controller for Peak Power Management

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