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A Combined Single Pulse and Repetitive UIS Rating System

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A rating system for Unclamped Inductive Switching in PowerMOS transistors already widely accepted and implemented on Fairchild PowerMOS transistor data sheets can be applied to a wide range of applications very easily and expanded to cover repetitive UIS pulses by the simple technique of superposition. This allows PowerMOS transistor users to determine if their application lies within the rated capability of a power transistor. Two examples are given of the analysis of UIS stress level in representative applications.

The ability of PowerMOS transistors to withstand unclamped inductive switching (UIS) has been recognized since 1985. Although Blackburn has clearly shown [1] UIS stress level is not directly related to energy, many manufacturers of PowerMOS transistors persist in rating their devices in terms of energy capability. Since the energy capability varies with the operating conditions, this rating is valid only at the condition specified and the PowerMOS transistor user has no way to calculate whether the particular application exceeds the device rating. Ronan has defined a rating system [3], herein after called simply the UIS Rating System, which allows manufacturers to specify the capability of their PowerMOS transistors for single pulse UIS in such a way that users can easily determine if their application exposes the device to more UIS stress than is guaranteed in the device data sheet.

The Single Pulse UIS Rating System

This UIS Rating System, requires the user to determine only the peak current through the PowerMOS transistor (I_{AS}), the junction temperature at the start of the UIS pulse (T_J) and the time the transistor remains in avalanche (t_{AV}). It allows the easy determination of the conformance of any application to a specified UIS capability where the worst case conditions can be simulated. It is also quite feasible to calculate the UIS stresses for circuits not yet constructed or conditions not easily simulated.

The UIS rating for a PowerMOS transistor (see Figure 1) is presented as a chart with a vertical axis of (I_{AS}) maximum avalanche current vs (t_{AV}) time in avalanche as the horizontal axis. Two lines are shown, one for 25°C and one for the maximum junction temperature. It is fairly easy in most applications to determine the avalanche current and time in avalanche in an existing application by using a current probe. If the time in avalanche and avalanche current plotted on the UIS rating curve fall above and to the right of the 25°C line, the application is beyond the UIS rating of the device and the user stands a risk of device failure. If the time and current plotted on the rating curve fall below and to the left of the maximum junction temperature line the application is within the UIS rating of the device. In either case no further analysis is needed. If the time and current plotted on the rating chart falls between the 25°C and the maximum junction temperature lines further analysis is required.

To analyze those cases where the starting temperature and time in avalanche fall between the 25°C and maximum temperature line, first we must determine the junction temperature of the PowerMOS transistor at the start of the UIS pulse. If the UIS stress occurs after a long period in conduction it may be sufficient to just measure the case temperature of the device and calculate the temperature rise between the case and junction from the dissipation and thermal resistance of the device. Any other approach may be used. Once the junction temperature at the start of the pulse has been determined we can extrapolate between the two published rating curves to determine the UIS capability at that starting junction temperature.

Ronan [3], Stoltenburg [2] and Blackburn [1] have all indicated that the UIS capability $I^2_{AS} x t_{AV}$ is a simple linear function of temperature. Using this allows a straight line extrapolation of the UIS capability of the device at the calculated junction temperature. Then simply compare the calculated capability to the stress determined to determine if the device is within ratings. This simple approach allows users to find out if their application is safe for any single UIS pulse.

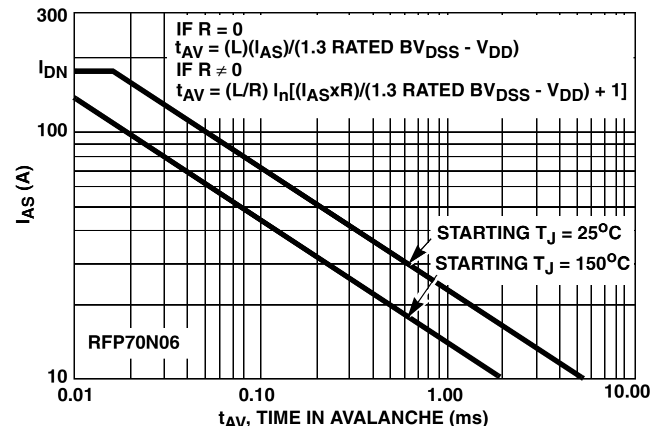

FIGURE 1. UNCLAMPED-INDUCTIVE-SWITCHING (SINGLE PULSE UIS)

Multiple or Repetitive UIS

The handling of repetitive UIS pulses has been ignored by the PowerMOS transistor manufacturers except for an attempt by one manufacturer to rate repetitive UIS at 0.01% of the 25°C power rating with no further qualifications. The UIS rating system outlined in Ronan's paper [3] is quite applicable to repetitive pulses by using the technique of superposition as is commonly done in evaluating repetitive SOA pulses. Each UIS pulse is considered a separate event

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and evaluated as if no other pulse existed. It is necessary only to determine I_{AV} (avalanche current), t_{AV} (time in avalanche) and T_J (junction temperature at the start of the pulse), just as in the single pulse case. Usually the last pulse in a series occurs at the highest junction temperature and is therefore the most severe stress. If the PowerMOS transistor is within the specified UIS rating for that pulse, it is certainly within the UIS ratings for previous pulses which occurred at a lower junction temperature.

Usually the junction temperature variation of a PowerMOS transistor over a full repetitive period is very small. The device has a thermal capacitance and does not change temperature instantaneously, so usually using the average junction temperature for the starting temperature to evaluate the avalanche stress does not result in appreciable error. In those cases where the period is long other means must be used to determine the junction temperature at the start of the UIS pulse.

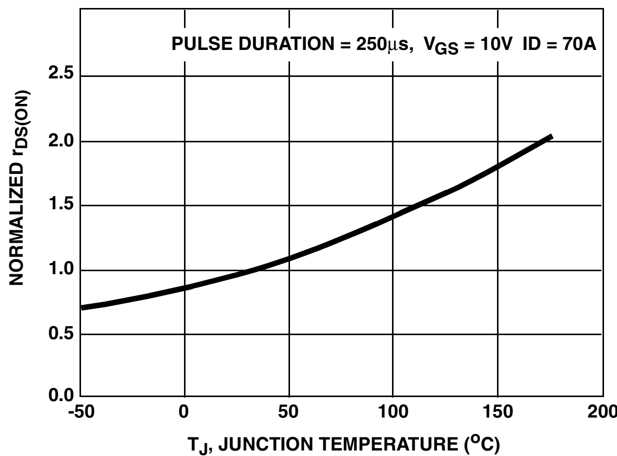
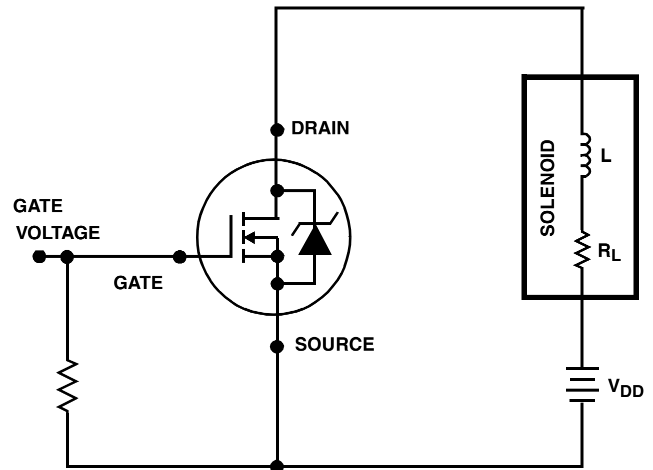


FIGURE 2. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

Examples

The two examples shown below are intended only to illustrate the techniques used to calculate whether a PowerMOS transistor is within its UIS rating or not. Since UIS capability is an interactive function of other environmental stresses, it is necessary to include some calculation of other operating conditions as part of this analysis. The operating conditions in both examples are calculated rather than measured since the determination of UIS capability using measured values for I_{AV} and t_{AV} seemed trivial and self explanatory. The first example is a "single" pulse stress with sufficient time between stresses so that there is no interaction between subsequent pulses, and the second has a period short enough so that the temperature variation over a period is small.

Example 1



SCHEMATIC

Solenoid Driver: Single Pulse

Given: V_{DD} = 28V
R_L = 2.5Ω
Pulse width = Steady state "on"
Transistor = RFP70N06
Gate "on" drive = 10V
Maximum T_J = 150°C
$T_{AMBIENT}$ = 90°C

Calculate: L (Maximum allowable inductance)
θ_{CA} (Required case to ambient thermal resistance)

$R_{TOTAL} = R_L + r_{DS(ON)}$ = 2.5 + (0.014 x 1.8) See Figure 2
R_{TOTAL} = 2.525Ω
$I_{AVALANCHE}$ = 28/2.525 = 11.09A
(Peak avalanche current)

Using the rule of thumb that the avalanche voltage is equal to the rated breakdown rating multiplied by 1.3 we can write:

$V_{AVALANCHE}$ = 60 x 1.3 = 78V
$t_{AVALANCHE}$ = (L/R) x ln[(I_{AV} x R)/(V_{AV} - V_{DD}) +1]
$t_{AVALANCHE}$ = (L/2.525) x ln[(11.09 x 2.525)/(78 - 28) +1]
L = $t_{AVALANCHE}$/0.176

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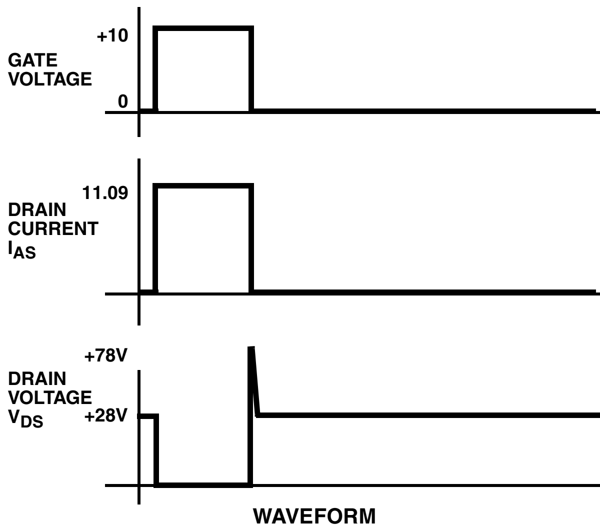


Entering the Unclamped Inductive Switching Chart (See Figure 1) at 150°C and 11.09A we read an allowable $t_{AVALANCHE}$ of 1.5ms. This gives us a maximum allowable L of:

L = (1.5E-3)/0.176 = 8.53mH
maximum allowable inductance

Now to calculate the required heat sink thermal resistance:

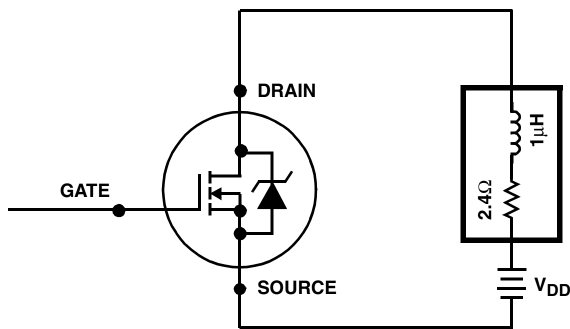
$Pd = (I^2 \times r_{DS(ON)}) = (11.09^2) \times 0.025 = 3.07W$

$\theta_{CA} = [T_{JMAX} - P_D \times \theta_{JC} - T_{AMBIENT}]/P_D$

$\theta_{CA} = [150 - (3.07 \times 1.0) - 40]/3.07$

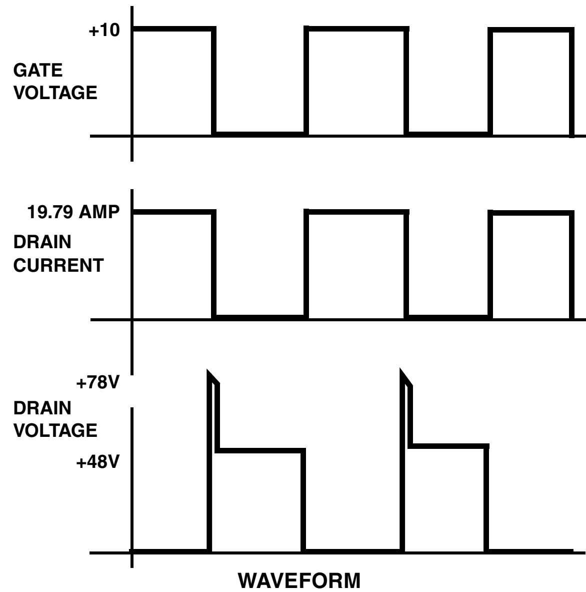
θ_{CA} = 18.5 °C/W required thermal resistance, case to ambient.

Example 2



SCHEMATIC

Switching Regulator - 100kHz
Given:
Frequency = 100kHz
Duty Cycle = 50%
$R_L = 2.4\Omega$
$V_{DD} = 48V$
$T_{AMBIENT} = 40^oC$
$T_{JUNCTION} = 150^oC$ Maximum junction temperature
L = 1µH (Leakage Inductance)
PowerMOS transistor = RFP70N06



Determine:
Is the PowerMOS transistor within UIS rating?
What θ_{CA} is required?

$I_{AVALANCHE} = V_{DD}/(R_L + r_{DS(ON)})$

$I_{AVALANCHE} = 48/(2.4 + (0.014 \times 1.8))$ See Figure 2

$I_{AVALANCHE} = 19.79A$

$t_{AVALANCHE} = (L/R) \times \ln[(I_{AV} \times (R_L + r_{DS(ON)}))/V_{AV} - V_{DD}) + 1]$

$t_{AVALANCHE} = (1E\text{-}6/2.425) \times \ln[19.79 \times 2.425/(78 - 48) + 1]$

$t_{AVALANCHE} = 0.395\mu s$

Entering the Unclamped Inductive Switching Curve (See Figure 1) at 19.79A, we find the device has a $t_{AVALANCHE}$ capability at 150°C of 500µs. Obviously this application does not challenge the UIS capability of the RFP70N06.

Now to calculate the required heat sink thermal resistance:

$E_{AVALANCHE} = (V_{AVALANCHE} \times I_{AVALANCHE} \times t_{AVALANCHE}) /2$

$E_{AV} = ((60 \times 1.3) \times 19.79 \times (0.395\ e\text{-}6))/2$

$E_{AV} = 304.8\mu J$ per avalanche

$P_{AVALANCHE} = E_{AVALANCHE} \times$ Frequency

$P_{AVALANCHE} = 304.8e\text{-}6 \times 100e3$

$P_{AVALANCHE} = 30.4W$

$P_{CONDUCTION} = (I_{AV}^2 \times r_{DS(ON)})/2$

$P_C = ((19.79)^2 \times 0.025)/2$

$P_C = 4.90W$

$P_{TOTAL} = P_{AV} + P_C$

$P_{TOTAL} = 30.4 + 4.9$

$P_{TOTAL} = 35.3W$

$\theta_{CA} = [T_{JMAX} - (P_{TOTAL} \times \theta_{JC}) - T_{AMBIENT}]/P_{TOTAL}$

$\theta_{CA} = [150 - (35.3 \times 1.0) - 40]/35.3$

$\theta_{CA} = 2.12^oC/W$ Obviously the heat sink is more of a problem than the UIS capability.

Application to Other Circuits

Usually the designer of a circuit has carefully determined the temperature of the devices in his circuit over the entire range of operating conditions. Using only the junction temperature of the device at the start of a UIS pulse, the duration of the pulse and the current level of the pulse the designer can determine whether or not his/her application exceeds the UIS rating on the device. These quantities are easily measured or calculated. By superposition this rating can be applied to multiple or repetitive pulses as illustrated in the two examples shown. Any circuit can be analyzed for UIS stress using this approach. There is no need for a separate repetitive UIS rating.

References

For Fairchild documents available on the internet, see web site
http://www.Fairchildsemi.com AnswerFAX (321) 724-7800.

[1] D.L. Blackburn, *"Turn-off Failure of Power MOSFETS,"* Proc. 1985 IEEE Power Electronics Specialists Conference, pp 429-435, June, 1985.

[2] Rodney R. Stoltenburg, *"Boundary of Power-MOSFET Unclamped Inductive Switching (UIS) Avalanche Current Capability,"* Proc. 1989 Applied Power Electronics Conference, pp 359-364, March 1989.

[3] Harold R. Ronan, *"Rating System Compares Single Pulse Unclamped Inductive Switching for MOSFETS,"* Power Conversion and Intelligent Motion, pp 32-40, September 1991.

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