

AN-8014

FMS6419 Evaluation Board Application Note

Description

The FMS6419 offers comprehensive filtering for set top box or DVD applications. This part consists of a triple 6th order filter with selectable 32MHz and 8MHz frequencies and a dual filter for filtering Y, C with a composite summer. 2-to-1 multiplexers are provided on the triple filters as well as provisions for auxiliary input to the composite channel. The triple filters are intended for either YPbPr, RGB, or YUV signals. All channels accept DC coupled ground-referenced 1Vpp signals. The filters outputs 2Vpp signals into AC coupled terminated loads. The low-pass filters are powered by 3.3V and output buffers are powered by 5.0V.

The FMS6419 is a next generation filter solution from Fairchild Semiconductor addressing the expanding filtering needs for set top boxes and DVD players. The product provides selectable filtering from 32MHz and 8MHz on the RGB channels. Thus, the FMS6419 addresses the requirement for a single set top box to be compatible with a variety of resolution standards. Additionally, the product provides additional filters for Y,C, and Composite Video (CV) outputs. Multiplexers on the RGB and CV channels provide further flexibility.

For DVD applications, the product provides filtering and output drive amplification for 6 channels of outputs. These include R/Pr, G/Y, B/Pb, Y, C, and CV outputs.

For set top boxes, this product provides for 2 channels of video to be filtered, as well as the flexibility of selectable high order filtering for multiple resolution standards. Additional flexibility is provided by the Y (Luma) and C (Chroma) filters with a composite summer.

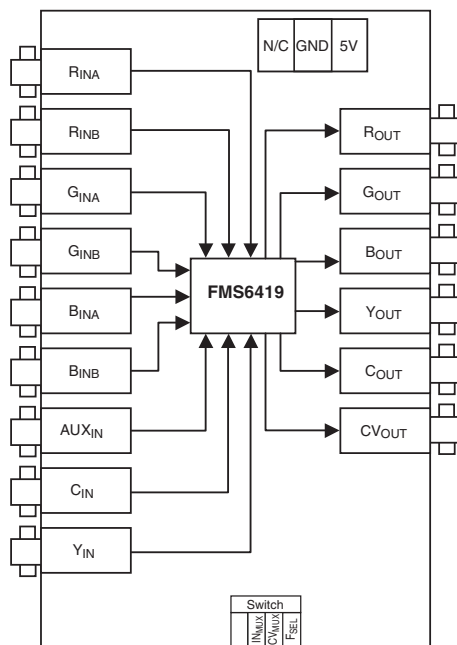
All channels provide 6dB gain, accept 1V ground referenced inputs, and drive AC coupled loads. The filters for all channels are powered from a 3.3V supply and the outputs from 5V.

Applications

- Cable set top boxes
- Satellite set top boxes
- DVD players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

For a complete description of the FMS6419 please refer to the FMS6419 data sheet.

Evaluation Board Block Diagram



Evaluation Kit Contents

The FMS6419 Evaluation Kit contains the following items:

- AN-8014 – FMS6419 Evaluation Board Application Note
- The latest revision of the FMS6419 data sheet, which also can be obtained from <http://www.fairchildsemi.com>.
- Fully functional FMS6419 eval board
- Female power connector

Board Setup and Test

The following test equipment is necessary to test the FMS6419 eval board.

- One power supply +5V \pm 5%, 250mA
- One high resolution CRT monitor (2 channel with RGB)
- One HDTV
- One NTSC or PAL video signal source capable of generating necessary outputs (RGB, Y, C & Composite)
- One HD signal source
- One video measurement set (VM700)
- One VM5000HD video measurement set
- Assorted video cables

Use the following procedure to verify that the FMS6419 eval board is functional.

SD Verification

1. Verify that the switches are in the correct position.
2. SW1-1 through SW1-3 should be off. All toggles should be in the up position. SW1-4 should always be on (down).
3. See Table 1 and Table 2 for all switch configurations.

DO NOT turn on power supply until all connections are completed.

1. Set the power supply to 5.0V. Connect the power supply to the input voltage terminals of the evaluation board.
2. Connect RGB signal source to the appropriate input BNC connectors. (RGB_{IN})

Table 1. Switch Setting for RGB Channels

Control		Outputs		
IN _{MUX} (SW1-3)	F _{SEL} (SW1-1)	R _{OUT}	G _{OUT}	B _{OUT}
Off	Off	R _{INA} (SD)	G _{INA} (SD)	B _{INA} (SD)
On	Off	R _{INB} (SD)	G _{INB} (SD)	B _{INB} (SD)
Off	On	R _{INA} (HD)	G _{INA} (HD)	B _{INA} (HD)
On	On	R _{INB} (HD)	G _{INB} (HD)	B _{INB} (HD)

Table 2. Switch Setting for Y, C, and AUX_{IN} Channels

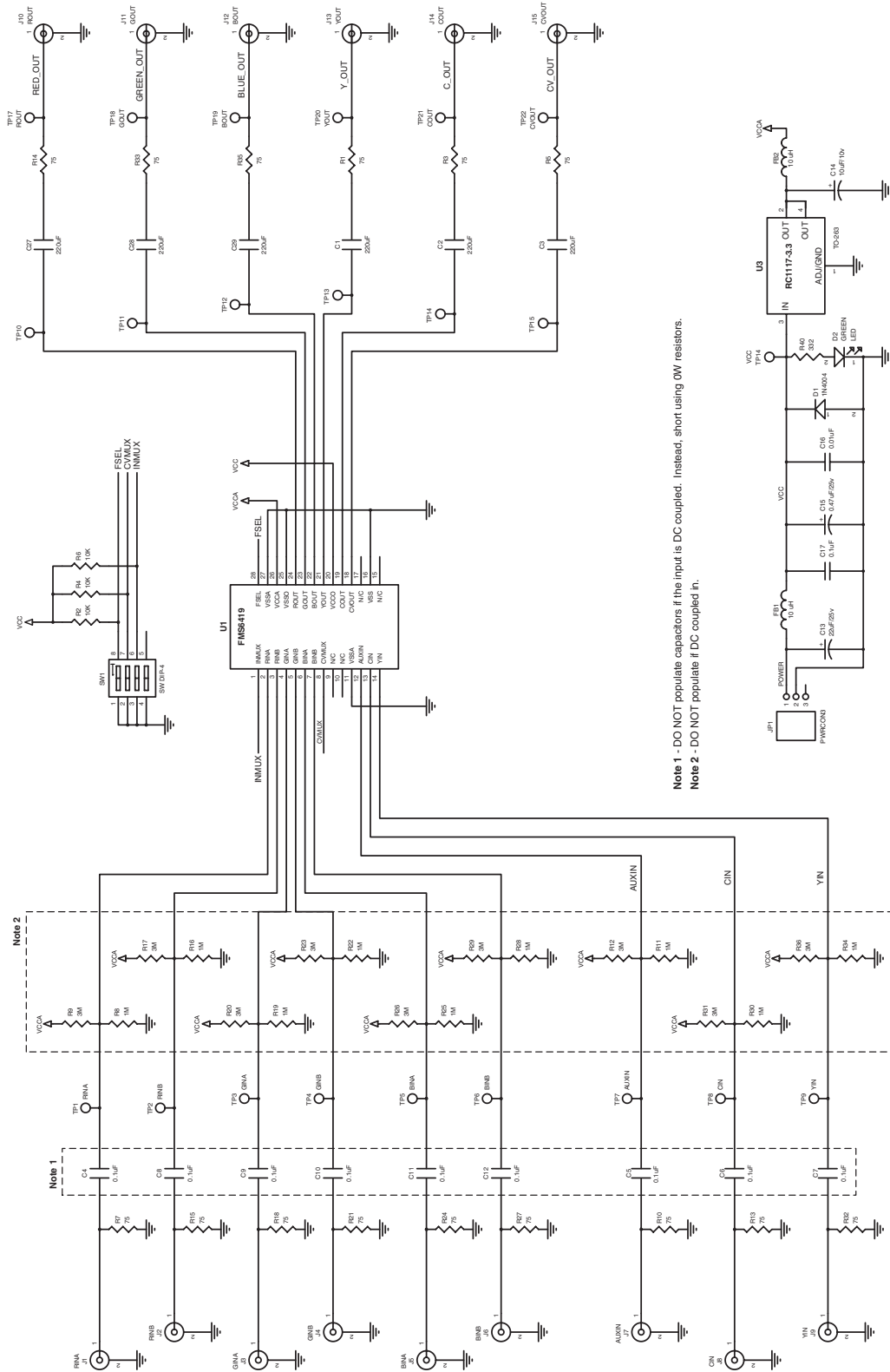
Control	Outputs		
CV _{MUX} (SW1-2)	Y _{OUT}	C _{OUT}	CV _{OUT}
Off	Y _{IN}	C _{IN}	Y _{IN} /C _{IN}
Off	Y _{IN}	C _{IN}	Y _{IN} /C _{IN}
On	AUX _{IN}	N/A	AUX _{IN}
On	AUX _{IN}	N/A	AUX _{IN}

Note: There will not be any output on C_{OUT} while using AUX_{IN}.

3. Connect the appropriate monitor cables to the output BNC connectors. (RGB_{OUT})
4. Connect a composite signal into the AUX_{IN}.
5. Connect Y_{IN} and C_{IN}.
6. Connect Channel A of monitor to CV_{OUT}.
7. Turn power on.
8. Press RGB channel on monitor and verify test pattern as the same going into RGB_{IN}.
9. Switch SW1-1 on and verify loss of signal.
10. Switch cables from R_{INA} to R_{INB}, G_{INA} to G_{INB} and B_{INA} to B_{INB}, signal will return.
11. Press channel A on monitor to verify signal going in through Y_{IN} and C_{IN}.
12. Switch SW1-3 on (down) to switch to AUX_{IN}. Now CV_{OUT} is coming from AUX_{IN}.
13. Press channel B on monitor and verify test pattern.
14. Switch SW1-3 off to switch source back to Y_{IN} & C_{IN}.
15. Turn power supply off.

HD Verification

1. Verify that the switches are in the correct position. Refer to Tables 1 and 2.
2. Connect HD signal source to the appropriate input BNC connectors. (RGB_{IN})
3. Connect appropriate HDTV cables to the output BNC connectors
4. Turn power on
5. Verify test pattern is on the HDTV.
6. Switch SW1-3 on and verify loss of signal.
7. Switch cables to RGB_{INB} and verify test pattern is back
8. Testing is now complete.



Note 1 - DO NOT populate capacitors if the input is DC coupled. Instead, short using 0W resistors.
Note 2 - DO NOT populate if DC coupled in.

Figure 1. FMS6419 Schematic Diagram

Bill of Materials

Item	Quantity	Reference	Part
1	6	C1, C2, C3, C27, C28, C29	220 μ F
2	10	C4, C5, C6, C7, C8, C9, C10, C11, C12, C17	0.1 μ F
3	1	C13	22 μ F/25V
4	1	C14	10 μ F/10V
5	1	C15	0.47 μ F/25V
6	1	C16	0.01 μ F
7	1	D1	1N4004
8	1	D2	GREEN
9	2	FB1, FB2	10 μ H
10	1	JP1	PWRCON3
11	2	TP1, J1	RINA
12	2	TP2, J2	RINB
13	2	TP3, J3	GINA
14	2	TP4, J4	GINB
15	2	TP5, J5	BINA
16	2	TP6, J6	BINB
17	2	TP7, J7	AUXIN
18	2	TP8, J8	CIN
19	2	TP9, J9	YIN
20	2	TP17, J10	ROUT
21	2	TP18, J11	GOUT
22	2	TP19, J12	BOUT
23	3	TP13, TP20, J13	YOUT
24	2	TP21, J14	ROUT
25	3	TP15, TP22, J15	CVOUT
26	15	R1, R3, R5, R7, R10, R13, R14, R15, R18, R21, R24, R27, R32, R33, R35	75 Ω
27	3	R2, R4, R6	10K Ω
28	9	R8, R11, R16, R19, R22, R25, R28, R30, R34	1M Ω
29	9	R9, R12, R17, R20, R23, R26, R29, R31, R36	3M Ω
30	1	R40	332 Ω
31	1	SW1	SW DIP-4
32	1	TP10	RED_OUT
33	1	TP11	GREEN_OUT
34	1	TP12	BLUE_OUT
35	1	TP14	C_OUT
36	1	TP24	VCC
37	1	U1	FMS6419
38	1	U3	RC1117-3.3

Applications

DC Levels

At any given time, the input signal's DC levels must be between 0.0V and 1.3V to utilize the optimal headroom and to avoid clipping on the outputs. The Y_{IN} channel should nominally have the Sync Tip at ground and be a 1V signal. The C_{IN} channel should ride around the 0.3V level. This will ensure that the filter will utilize the optimal headroom and avoid clipping. At any given time, the sum of Y_{IN} and C_{IN} must be 0.0V to 1.3V otherwise the CV_{OUT} may be clipped.

Driving the Digital Pins with 3.3V or 5V Logic

Either is allowed as long as the V_{IH} and V_{IL} are adhered to.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance and thermal characteristics. The FMS6419DEMO board is a 4-layer board with a full power and ground plane. Following this layout configuration will provide the optimum performance and thermal characteristics. For optimum results, follow the steps below as a basis for high frequency layout.

- Include 10 μ F and 0.1 μ F ceramic bypass capacitors.
- Place the 10 μ F capacitor within 0.75 inches of the power pin
- Place the 0.1 μ F capacitor within 0.1 inches of the power pin
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For 2 layer boards, use a ground plane that extends beyond the device by at least 0.5 inches
- Minimize all trace lengths to reduce series inductance

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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