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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/008,326	11/09/2006	6249876	10414-25	7651

7590 07/01/2009

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EXAMINER

ART UNIT PAPER NUMBER

DATE MAILED: 07/01/2009

Please find below and/or attached an Office communication concerning this application or proceeding.



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(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. 90/008,326.

PATENT NO. 6249876.

ART UNIT 3992.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Office Action in Ex Parte Reexamination	Control No. 90/008,326	Patent Under Reexamination 6249876	
	Examiner Christopher E. Lee	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

- a Responsive to the communication(s) filed on 30 January 2009. b This action is made FINAL.
c A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 2 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- | | |
|--|---|
| 1. <input type="checkbox"/> Notice of References Cited by Examiner, PTO-892. | 3. <input type="checkbox"/> Interview Summary, PTO-474. |
| 2. <input type="checkbox"/> Information Disclosure Statement, PTO/SB/08. | 4. <input type="checkbox"/> _____. |

Part II SUMMARY OF ACTION

- 1a. Claims 1 and 17-19 are subject to reexamination.
1b. Claims 2-16 and 20-32 are not subject to reexamination.
2. Claims _____ have been canceled in the present reexamination proceeding.
3. Claims _____ are patentable and/or confirmed.
4. Claims 1 and 17-19 are rejected.
5. Claims _____ are objected to.
6. The drawings, filed on _____ are acceptable.
7. The proposed drawing correction, filed on _____ has been (7a) approved (7b) disapproved.
8. Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some* c) None of the certified copies have
1 been received.
2 not been received.
3 been filed in Application No. _____
4 been filed in reexamination Control No. _____
5 been received by the International Bureau in PCT application No. _____
* See the attached detailed Office action for a list of the certified copies not received.
9. Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. Other: _____

cc: Requester (if third party requester)

DETAILED ACTION

Ex Parte Reexamination

1. This is an *Ex Parte* Reexamination of US 6,249,876 B1 (hereinafter '876 Patent).
2. The Patent Owner filed petition under 37 CFR §1.182 on 24th of March 2009 for the
5 **continuation** of the instant reexamination proceeding. The petition has been granted such that
the prosecution of the instant proceeding for *Ex Parte* Reexamination of '876 Patent is
continued. Therefore, the closing of prosecution rendered via the *Ex Parte* REX Final Office
Action mailed on 3rd of December 2008 has been withdrawn and prosecution of the instant
proceeding has been reopened.

10 3. Per the decision on the petition, the Response filed on 30th of January 2009 to the *Ex*
Parte REX Final Office Action mailed on 3rd of December 2008 is entered and considered by the
Examiner. The Response is treated as a response by Patent Owner received **after** a first Office
action.

Receipt Acknowledgement

15 4. Receipt is acknowledged of the Response filed on 30th of January 2009. Claims 1, 17,
and 18 have been amended; no claim has been canceled; and no claim has been newly added
since the *Ex Parte* REX Final Office Action was mailed on 3rd of December 2008. Currently, the
claims 1 and 17-19 are subject to reexamination and the claims 2-16 and 20-32 are not subject
to reexamination in this *Ex Parte* Reexamination.

20 **Claim Rejections - 35 USC § 102**

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the
basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

25 (b) the invention was patented or described in a printed publication in this or a foreign country or in public
use or on sale in this country, more than one year prior to the date of application for patent in the United
States.

30 6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Martin, Jr. et al. [US
4,638,417; hereinafter "Martin"].

Referring to claim 1, Martin discloses a digital frequency jittering circuit (i.e., power
density spectrum controller) for varying the switching frequency of a power supply (i.e., DC-to-
DC converter 15 of Figure; in fact, a circuit maintaining the average power of a large number of

operating frequencies of the circuit within the dynamic range of the switching mode of a power supply; See col. 1, lines 49-53 and col. 2, lines 12-15), comprising:

- an oscillator (i.e., VCO 13 of Figure) for generating a signal (i.e., oscillating signal) having a switching frequency (See col. 2, lines 46-49), the oscillator (i.e., said VCO) having a control input (i.e., input line from D/A 12 in Figure) for varying the switching frequency (See col. 2, lines 39-49);
- a digital to analog converter (i.e., D/A 12 of the Figure) coupled to the control input (i.e., said input line from said D/A) for varying the switching frequency (See col. 2, lines 44-49); and
- a counter (i.e., COUNTER 10 of the Figure) coupled to the output of the oscillator (i.e., feedback line from said VCO in Figure), the digital to analog converter (i.e., said D/A) coupled to the counter (i.e., said COUNTER being coupled to said D/A through EPROM 11 in Figure; See col. 2, lines 39-46), the counter (i.e., said COUNTER) causing the digital to analog converter (i.e., said D/A) to adjust the control input (i.e., said input line from said D/A) and to vary the switching frequency (See col. 2, lines 20-49) of the power supply (i.e., said DC-to-DC converter; See col. 2, lines 55-66).

7. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al.

["Programmed Pulsewidth Modulated Waveforms for Electromagnetic Interference Mitigation in DC-DC Converters," IEEE Transactions on Power Electronics, Vol. 8, No.4 (October 1993) by A.C. Wang and S.R. Sanders, pp. 596-605; hereinafter "Wang"].

Referring to claim 1, Wang discloses a digital frequency jittering circuit (i.e., PWM type power circuit with a time-varying switching frequency) for varying the switching frequency of a power supply (i.e., DC-DC Converter; See page 596, I. Introduction, lines 12-25), comprising:

- an oscillator (i.e., internal wave form generator, in fact, Oscillator between D/A and Comparator, said Comparator, and Simple Control Logic in Fig. 20) for generating a signal (i.e., Internal Waveforms in Fig. 19) having a switching frequency (i.e., switching frequency V_{TR} in Fig. 20), the oscillator (i.e., said internal wave form generator) having a control input (i.e., Ramp Slope in Fig. 20) for varying the switching frequency (See page 604, col. 1, lines 2-7);
- a digital to analog converter (i.e., Subperiod Width D/A in Fig. 20) coupled to the control input (i.e., said Ramp Slope being coupled to output line from said Subperiod Width D/A

in Fig. 20) for varying the switching frequency (in fact, Counter causing said Subperiod Width D/A to adjust said Ramp Slope and to vary said switching frequency V_{TR} in Fig. 20; See pages 603-604); and

- a counter (i.e., Counter in Fig. 20) coupled to the output of the oscillator (i.e., said Counter being coupled to said internal wave form generator, actually, said Simple Control Logic, in Fig. 20), the digital to analog converter (i.e., said Subperiod Width D/A) coupled to the counter (i.e., said Counter being coupled to said Subperiod Width D/A through ROM in Fig. 20), the counter (i.e., said Counter) causing the digital to analog converter (i.e., said Subperiod Width D/A) to adjust the control input (i.e., said Ramp Slope from said Subperiod Width D/A) and to vary the switching frequency of the power supply (i.e., said DC-DC Converter; See Fig. 20 and VII. Implementation and VIII. Conclusion on pages 603-604).

8. Claims 1 and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Habetler et al. ["Acoustic Noise Reduction in Sinusoidal PWM Drives Using a Randomly Modulated Carrier," IEEE Transactions on Power Electronics, Vol. 6, No. 3, p.356-363 (published July 1991) by T.G. Habetler and D. M. Divan; hereafter "Habetler"].

Referring to claim 1, Habetler discloses a digital frequency jittering circuit (i.e., random carrier sinusoidal PWM regulator in Fig. 5) for varying the switching frequency of a power supply (i.e., sinusoidal PWM Inverter in Fig. 5; in fact, for varying the switching frequency of Inverter; See page 359, IV. Implementation), comprising:

- an oscillator (i.e., Triangle Generator of Fig. 5) for generating a signal (i.e., triangle wave) having a switching frequency (i.e., said Triangle Generator generating said triangle wave with a switching frequency, inherently, in Fig. 5), the oscillator (i.e., said Triangle Generator) having a control input (i.e., input from A/D and Average Slope in Fig. 5) for varying the switching frequency (See page 359, IV. Implementation, lines 19+);
- a digital to analog converter (i.e., A/D, in fact, digital to analog converter, in Fig. 5; See page 359, IV. Implementation, lines 28-30) coupled to the control input (i.e., said input from A/D and Average Slope being coupled to output line from said A/D in Fig. 5) for varying the switching frequency (See IV. Implementation, lines 19+ on page 359); and
- a counter (i.e., Counter in Fig. 5) coupled to the output of the oscillator (i.e., said Counter being coupled to said Triangle Generator through Peak Detector in Fig. 5), the digital to

5 analog converter (i.e., said A/D) coupled to the counter (i.e., said Counter being coupled to said A/D through EPROM in Fig. 5), the counter (i.e., said Counter) causing the digital to analog converter (i.e., said A/D) to adjust the control input (i.e., said input from A/D and Average Slope) and to vary the switching frequency of the power supply (i.e., said PWM Inverter; See Fig. 5 and IV. Implementation, lines 19+ and V. Experimental Result, lines 1-2 on page 359).

10 *Referring to claim 17*, Habetler discloses a method for generating a switching frequency (i.e., generating triangle wave having a switching frequency in Fig. 5) in a power conversion system (i.e., sinusoidal PWM Inverter in Fig. 5; See V. Experimental Result, lines 1-2 on page 359); comprising:

- generating a primary voltage (i.e., Average Slope, as a primary voltage, is provided to addition circuit in Fig. 5);
- cycling a counter (i.e., Counter in Fig. 5) coupled to one or more secondary voltage sources (i.e., said Counter being coupled to A/D through EPROM in Fig. 5) to generate a secondary voltage (i.e., analog voltage output from said A/D) which varies over time (See IV. Implementation, lines 28-30); and
- combining the secondary voltage (i.e., said analog output voltage from A/D in Fig. 5) with the primary voltage (i.e., Average Slope in Fig. 5) to be received at a control input of a voltage-controlled oscillator (i.e., input of Triangle Generator in Fig. 5) for generating the switching frequency (i.e., PWM modulation) of the power conversion system (i.e., said sinusoidal PWM Inverter) which is varied over time (See IV. Implementation, lines 19+ on page 359).

25 *Referring to claim 18*, Habetler teaches

- clocking the counter (i.e., Counter of Fig. 5) with the output of the oscillator (i.e., said Counter being clocked by triangle wave generated by Triangle Generator in Fig. 5).

Referring to claim 19, Habetler teaches that

- the primary voltage (i.e., Average Slope, as a primary voltage, is provided to addition circuit in Fig. 5) is V and each of the secondary voltage sources generates a supplemental voltage lower than V (See V. Experimental Results, lines 3-7 on page 359,

wherein in fact that there is very little perceivable difference in the triangle wave with and without random modulation, since the instantaneous frequency is varying only slightly, which anticipates that output voltage from A/D is lower than said Average Slope voltage because the perceivable difference in the triangle waves between the conventional modulation and the random modulation is very little. In other words, the minor output voltage from said A/D is added to the major voltage of said Average Slope in Fig. 5), and

- passing the supplemental voltage to the voltage-controlled oscillator (i.e., said output voltage from A/D being passed to Triangle Generator for random carrier PWM regulation in Fig. 5; See IV. Implementation and V. Experimental Results on page 359).

Response to Arguments

9. The Patent Owner's arguments filed on 30th of January 2009 have been fully considered but they are not persuasive.

In response to the Patent Owner's argument with respect to "Martin does not have a digital to analog converter coupled to the counter as required in claim 1 as proposed in the accompanying clarifying amendment. Instead, Martin separates, i.e. decouples, the counter output and the digital to analog converter by placing an EPROM between the counter and the digital to analog converter. Indeed, in the arrangement shown in Martin the digital to analog converter is coupled to receive the contents of memory locations of the EPROM rather than the output of the counter. Accordingly, Martin fails to disclose, teach or fairly suggest at least the claimed limitations of 'the digital to analog converter coupled to the counter,' as expressly recited in independent claim 1 as proposed." in the Response pages 14-15, the Examiner respectfully disagrees.

Essentially, the claim 1 recites the limitation "the digital to analog converter coupled to the counter." However, the scope of the claimed invention in the claim 1 does not restrict the digital to analog converter is coupled to receive the output of the counter, but the digital to analog converter should be coupled to the counter regardless of directly or indirectly in light of the broadest reasonable interpretation of the claimed invention. In other words, the features upon which the Patent Owner relies (i.e., the digital to analog converter coupled to receive the output of the counter) are not recited in the rejected claim. Although the claim is interpreted in light of the specification, limitations from the specification are not read into the claim. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, even though Martin separates, i.e. decouples, the **counter output** and the digital to analog converter by placing an EPROM between the counter and the digital to analog converter, the structure of Martin's invention clearly discloses that the digital to analog converter is coupled to the **counter** via said EPROM.

5 Thus, the Patent Owner's argument on this point is not persuasive.

In response to the Patent Owner's argument with respect to "Wang does not have a digital to analog converter coupled to the counter as required in claim 1 as proposed. Instead, Wang separates, i.e. decouples, the counter output and the digital to analog converter by
10 *placing a ROM between the counter and the digital to analog converter. Indeed, in the arrangement shown in Wang, the digital to analog converter is coupled to receive the contents of memory locations of the ROM rather than the output of the counter. Accordingly, Wang fails to disclose, teach or fairly suggest at least the claimed limitations of 'the digital to analog converter coupled to the counter,' as expressly recited in independent claim 1 as proposed." in*
15 *the Response page 14, the Examiner respectfully disagrees.*

Essentially, the claim 1 recites the limitation "the digital to analog converter coupled to the counter." However, the scope of the claimed invention in the claim 1 does not restrict the digital to analog converter is coupled to receive the output of the counter, but the digital to analog converter should be coupled to the counter regardless of directly or indirectly in light of
20 the broadest reasonable interpretation of the claimed invention. In other words, the features upon which the Patent Owner relies (i.e., the digital to analog converter coupled to receive the output of the counter) are not recited in the rejected claim. Although the claim is interpreted in light of the specification, limitations from the specification are not read into the claim. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

25 Furthermore, even though Wang separates, i.e. decouples, the **counter output** and the digital to analog converter by placing a ROM between the counter and the digital to analog converter, the structure of Wang's invention clearly discloses that the digital to analog converter is coupled to the **counter** via said ROM.

Thus, the Patent Owner's argument on this point is not persuasive.

30

In response to the Patent Owner's statement with respect to "Habetler does not deal with EMI in a power supply, and thus, Habetler is not the sort of reference that one looking to solve

the EMI of the '876 Patent solves would normally looked to." in the Response page 15, the Examiner notes the followings.

(1) Habetler discloses a sinusoidal PWM Inverter in Fig. 5, which is used as a power supply (a.k.a. a power conversion system) feeding an induction machine in Fig. 1.

5 (2) It is noted that the feature upon which the Patent Owner relies (i.e., EMI in a power supply) is not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

(3) It has been held that a prior art reference must either be in the field of Patentee's endeavor or, if not, then be reasonably pertinent to the particular problem with which the Patentee was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Habetler is reasonably pertinent to the particular problem with which the Patentee was concerned, i.e., varying the switching frequency in PWM regulator (See Habetler, Fig. 5 on page 15 359).

Thus, the reference Habetler is enough to be relied upon as a basis for rejection of the claimed invention.

In response to the Patent Owner's argument with respect to "Habetler is not directed to a power supply and does not disclose, teach or fairly suggest a digital to analog converter coupled to the counter as required in claim 1 as proposed, or a counter coupled to one or more secondary voltages sources as required by claim 17 as proposed. Instead, Habetler is directed to an inverter system and separates, i.e. decouples, the counter output from the digital to analog converter by placing an EPROM between the counter and the digital to analog converter. Indeed, in the arrangement shown in Habetler, the digital to analog converter is coupled to receive the contents of memory locations of the EPROM rather than the output of the counter. ... Habetler fails to disclose, teach or fairly suggest generating and combining the claimed primary and secondary voltages as recited in claim 17 as proposed. Accordingly, Habetler fails to disclose, teach or fairly suggest at least the claimed limitations of 'the digital to analog converter coupled to the counter,' as expressly recited in independent claim 1 as proposed, or the claimed limitation of '...cycling a counter coupled to one or more secondary voltage sources,'

as expressly recited in claim 17 as proposed" in the Response pages 15-16, the Examiner respectfully disagrees.

First of all, the claim 1 recites the limitation "the digital to analog converter coupled to the counter," and the claim 17 recites the limitation "the counter coupled to one or more secondary voltage sources." However, the scope of the claimed invention in the respective claims 1 and 5 17 does not restrict the digital to analog converter (viz., the secondary voltage source) is coupled to receive the output of the counter, but the digital to analog converter (i.e., said secondary voltage source) should be coupled to the counter regardless of directly or indirectly in light of the broadest reasonable interpretation of the claimed invention. In other words, the 10 features upon which the Patent Owner relies (i.e., the digital to analog converter (viz., the secondary voltage source) coupled to receive the output of the counter) are not recited in the rejected claim. Although the claim is interpreted in light of the specification, limitations from the specification are not read into the claim. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

15 Even though Habetler separates, i.e. decouples, the **counter output** and the digital to analog converter (i.e., said secondary voltage source) by placing a EPROM between the counter and the digital to analog converter (i.e., said secondary voltage source), the structure of Habetler's invention clearly discloses that the digital to analog converter (i.e., said secondary voltage source) is coupled to the **counter** via said EPROM.

20 Furthermore, in contrary to the Patent Owner's argument, Habetler teaches a secondary voltage source (i.e., digital to analog converter A/D in Fig. 5) generating a secondary voltage (i.e., the slope of the triangle wave; See Habetler, col. 1, lines 46-48 at page 359), which is a voltage (See Habetler, III. Random Modulation at page 358). In addition, Habetler teaches the average slope in Fig. 5, being regarded as the claimed subject matter "primary voltage," is also 25 shown as a voltage in Fig. 3(b) on page 358.

Thus, the Patent Owner's argument on this point is not persuasive.

Conclusion

10. Patent Owner's amendment filed 30th of January 2009 necessitated the new grounds of 30 rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

A shortened statutory period for response to this action is set to expire TWO(2) MONTHS from the mailing date of this action.

Extensions of time under 37 CFR 1.136(a) do not apply in reexamination proceedings. The provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Further, in 35 U.S.C. 305 and in 37 CFR 1.550(a), it is required that reexamination proceedings "will be conducted with special dispatch within the Office."

Extensions of time in reexamination proceedings are provided for in 37 CFR 1.550(c). A request for extension of time must be filed on or before the day on which a response to this action is due, and it must be accompanied by the petition fee set forth in 37 CFR 1.17(g). The mere filing of a request will not effect any extension of time. An extension of time will be granted only for sufficient cause, and for a reasonable time specified.

The filing of a timely first response to this final rejection will be construed as including a request to extend the shortened statutory period for an additional month, which will be granted even if previous extensions have been granted. In no event however, will the statutory period for response expire later than SIX MONTHS from the mailing date of the final action. See MPEP § 2265.

All correspondence relating to this ex parte reexamination proceeding should be directed:

By EFS: Registered users may submit via the electronic filing system EFS-Web, at <http://sportal.uspto.gov/authenticate/authenticateuserlocalepf.html>

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For EFS-Web transmissions, 37 CFR 1.8(a)(1)(i) (C) and (ii) states that correspondence (except for a request for reexamination and a corrected or replacement request for reexamination) will be considered timely filed if (a) it is transmitted via the Office's electronic filing system in accordance with 37 CFR 1.6(a)(4), and (b) includes a certificate of transmission
5 for each piece of correspondence stating the date of transmission, which is prior to the expiration of the set period of time in the Office action.

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be
10 directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:

/Christopher E. Lee/

15 Primary Patent Examiner (Reexamination)
Central Reexamination Unit / Art Unit 3992

Conferees:

ESK
MA