FAIRCHILD SEMICONDUCTOR®

December 2010

FDD4243_F085

P-Channel PowerTrench® MOSFET

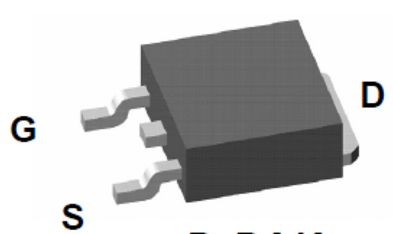
-40V, -14A, 64mΩ

Features

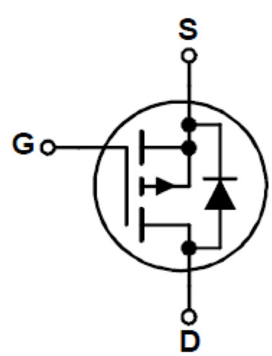
- Typ $r_{DS(on)}$ = 36mΩ at V_{GS} = -10V, I_D = -6.7A
- Typ $r_{DS(on)}$ = 48mΩ at V_{GS} = -4.5V, I_D = -5.5A
- Typ $Q_{g(TOT)}$ = 21nC at V_{GS} = -10V
- High performance trench technology for extremely low $r_{DS(on)}$
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Inverter
- Power Supplies



D-PAK
(TO-252)



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	-40	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C< 130^{o}C, V_{GS} = 10V)	-14	A
	Pulsed	See Figure 4	
E_{AS}	Single Pulse Avalanche Energe (Note 1)	84	mJ
P_D	Power Dissipation	50	W
	Dreate above 25^{o}C	0.34	W/^{o}C
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	^{o}C

Thermal Characteristics

$R_{\theta JC}$	Maximum Thermal Resistance Junction to Case	3	^{o}C/W
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient TO-252, 1in^2 copper pad area	40	^{o}C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD4243	FDD4243_F085	TO252	13”	12mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250μA, V_{GS} = 0V	-40	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	ID = -250μA, referenced to 25°C	-	-32	-	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -32V	-	-	-1	μA
		T_J = 125^{o}C	-	-	-100	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	-1.4	-1.6	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	ID = –250μA, referenced to 25°C	-	4.7	-	mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	I_D = -6.7A, V_{GS}= -10V	-	36	44	mΩ
		I_D = -5.5A, V_{GS}= -4.5V	-	48	64	
		I_D = -6.7A, V_{GS}= -10V, T_J = 150^{o}C	-	57	70	
g_{FS}	Forward Transconductance	I_D = –6.7A, V_{DS} = –5V,	-	23	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -20V, V_{GS} = 0V, f = 1MHz	-	1165	1550	pF
C_{oss}	Output Capacitance		-	165	220	pF
C_{rss}	Reverse Transfer Capacitance		-	90	135	pF
R_G	Gate Resistance	f = 1MHz	-	4	-	Ω
$Q_{g(TOT)}$	Total Gate Charge	V_{DD} = -20V, V_{GS} = -10V I_D = -6.7A	-	21	29	nC
Q_{gs}	Gate to Source Gate Charge		-	3.4	-	nC
Q_{gd}	Gate to Drain “Miller“ Charge		-	4	-	nC

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -20V, I_D = -6.7A V_{GS} = -10V, R_{GEN} = 6Ω	-	6	12	ns
t_r	Rise Time		-	15	26	ns
$t_{d(off)}$	Turn-Off Delay Time		-	22	35	ns
t_f	Fall Time		-	7	14	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Voltage	I_{SD} = -6.7A, V_{GS}=0V	-	-0.86	-1.2	V
t_{rr}	Reverse Recovery Time	I_{SD} = -6.7A, dI_{SD}/dt = 100A/μs	-	29	43	ns
Q_{rr}	Reverse Recovery Charge		-	30	44	nC

Notes:
1: Starting T_J= 25°C, L = 3mH, I_{AS}= 7.5A, V_{GS}= 10V, V_{DD}= 40V during the inductor charging time and 0V during the time in avalanche.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/
All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Typical Characteristics

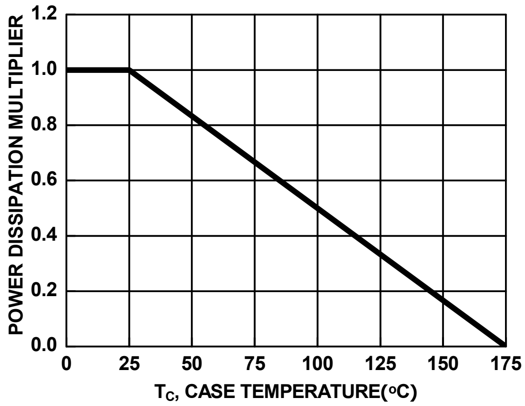


Figure 1. Normalized Power Dissipation vs Case Temperature

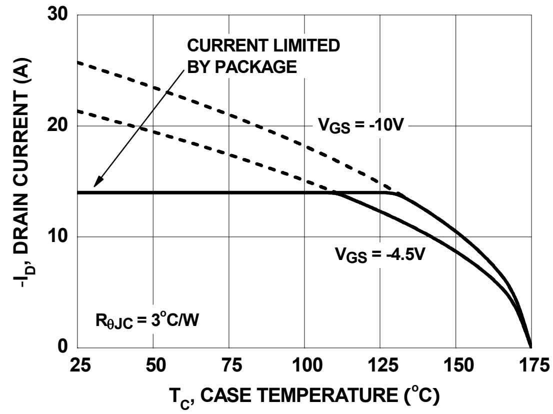


Figure 2. Maximum Continuous Drain Current vs Case Temperature

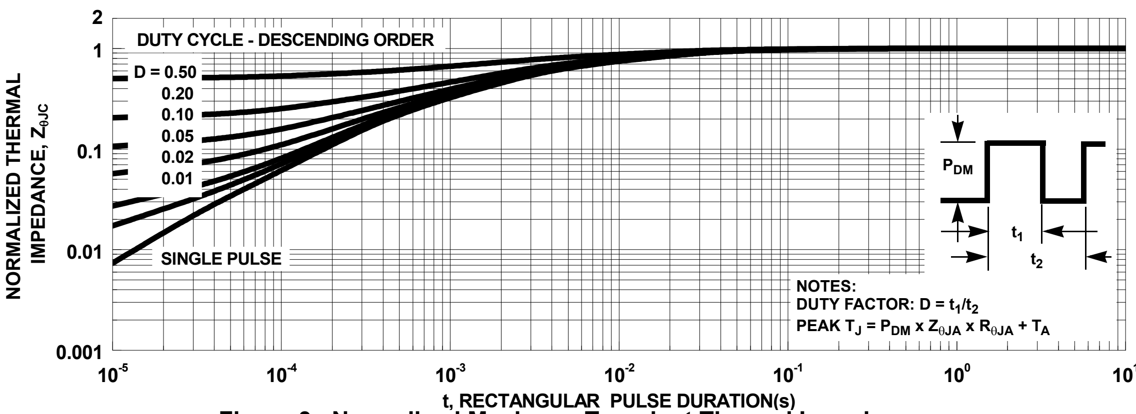


Figure 3. Normalized Maximum Transient Thermal Impedance

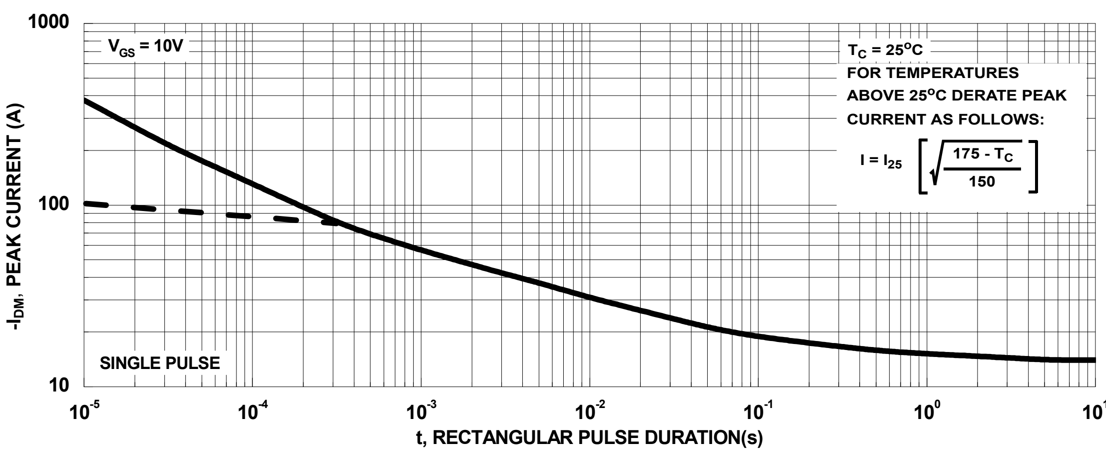


Figure 4. Peak Current Capability

Typical Characteristics

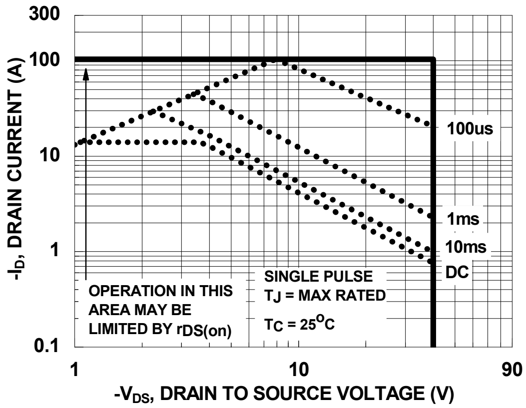
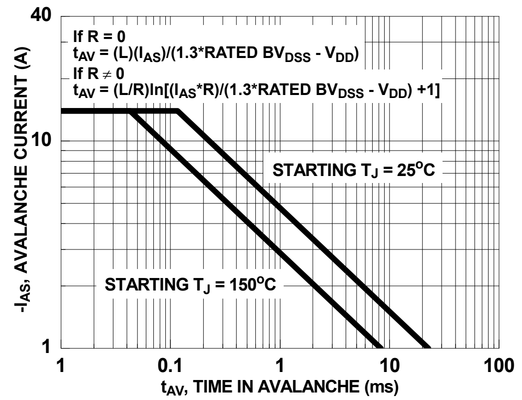


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

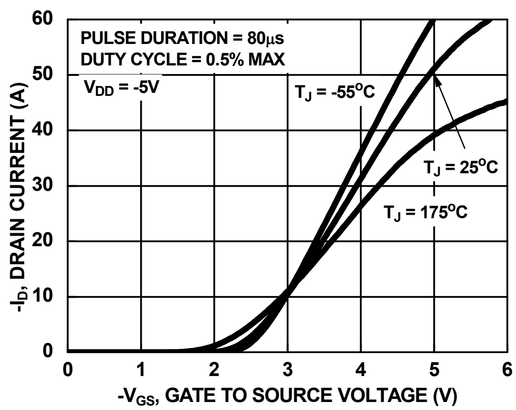


Figure 7. Transfer Characteristics

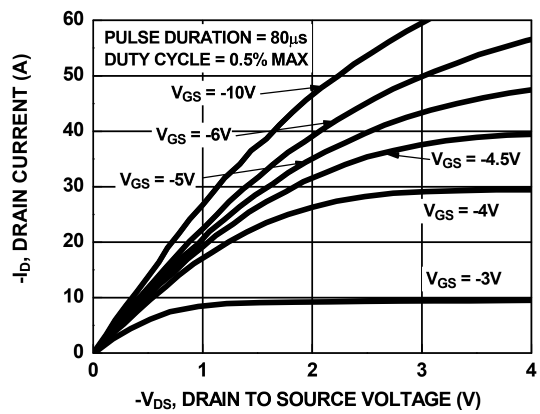


Figure 8. Saturation Characteristics

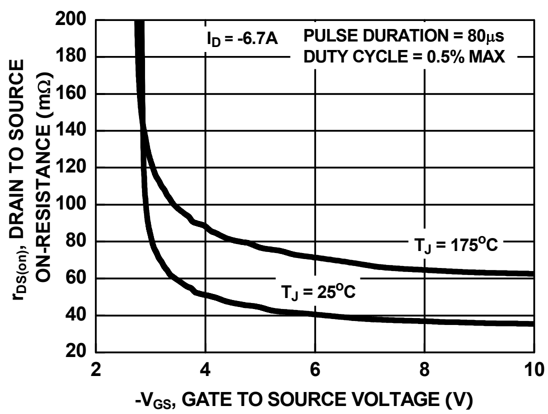


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

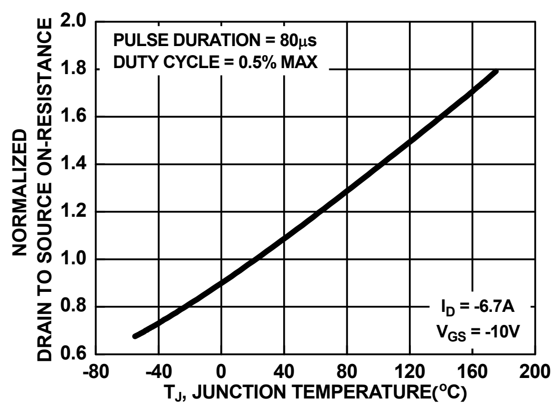


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics

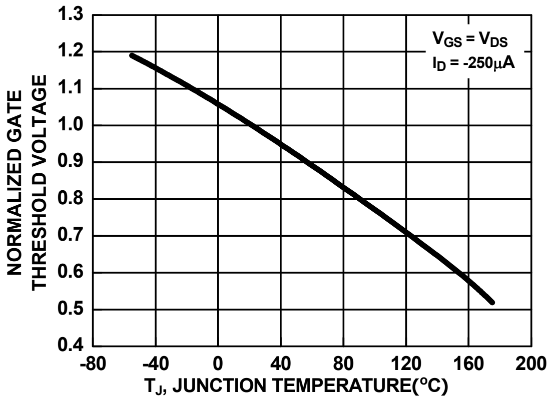


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

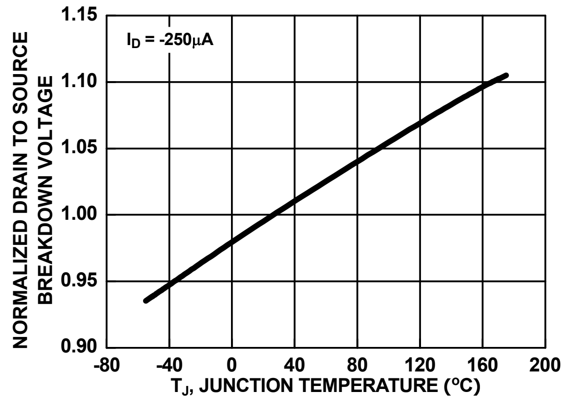


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

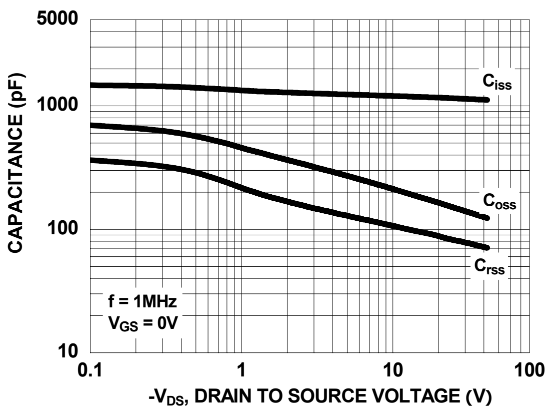


Figure 13. Capacitance vs Drain to Source Voltage

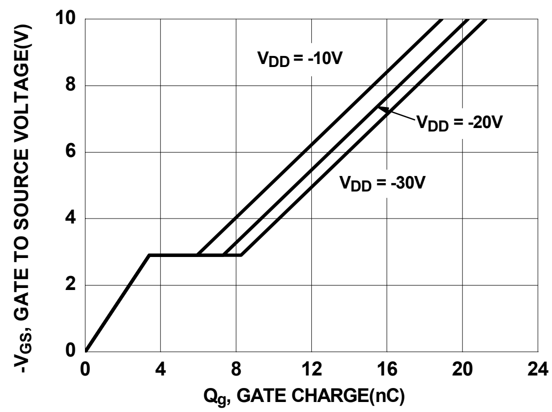


Figure 14. Gate Charge vs Gate to Source Voltage

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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