

FDMC7672

N-Channel Power Trench® MOSFET 30 V, 16.9 A, 5.7 mΩ

Features

- Max $r_{DS(on)}$ = 5.7 mΩ at $V_{GS} = 10$ V, $I_D = 16.9$ A
- Max $r_{DS(on)}$ = 7.0 mΩ at $V_{GS} = 4.5$ V, $I_D = 15.0$ A
- High performance technology for extremely low $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant

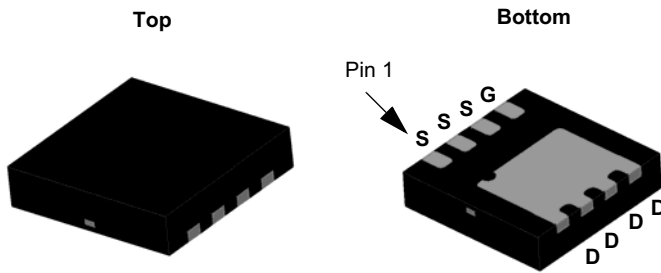


General Description

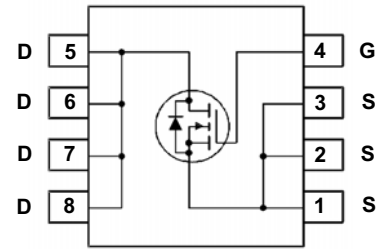
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Application

- DC - DC Buck Converters
- Notebook battery power management
- Load switch in Notebook



MLP 3.3x3.3



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

| Symbol | Parameter | Rated | Units |
|----------------|---|-------------|-------|
| V_{DS} | Drain to Source Voltage | 30 | V |
| V_{GS} | Gate to Source Voltage | ±20 | V |
| I_D | Drain Current -Continuous (Package limited) $T_C = 25$ °C | 20 | A |
| | -Continuous $T_A = 25$ °C (Note 1a) | 16.9 | |
| | -Pulsed | 50 | |
| E_{AS} | Single Pulse Avalanche Energy (Note 3) | 144 | mJ |
| P_D | Power Dissipation $T_A = 25$ °C (Note 1a) | 2.3 | W |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | °C |

Thermal Characteristics

| | | | |
|-----------------|---|----|------|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 53 | °C/W |
|-----------------|---|----|------|

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|----------|-------------|-----------|------------|------------|
| FDMC7672 | FDMC7672 | MLP 3.3x3.3 | 13 " | 12 mm | 3000 units |

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | |
|--------------------------------------|---|---|----|----|----------|----------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$ | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ | | 13 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$ $T_J = 125\text{ }^\circ\text{C}$ | | | 1 250 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$ | | | 100 | nA |

On Characteristics

| | | | | | | |
|--|--|--|-----|-------------------|-------------------|----------------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$ | 1.2 | 1.9 | 3.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ | | -6 | | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS} = 10\text{ V}$, $I_D = 16.9\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 15.0\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 16.9\text{ A}$ $T_J = 125\text{ }^\circ\text{C}$ | | 4.3 5.4 5.5 | 5.7 7.0 6.9 | m Ω |
| g_{FS} | Forward Transconductance | $V_{DD} = 5\text{ V}$, $I_D = 16.9\text{ A}$ | | 82 | | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|--|--|------|------|----------|
| C_{iss} | Input Capacitance | $V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$ | | 2925 | 3890 | pF |
| C_{oss} | Output Capacitance | | | 1050 | 1400 | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 80 | 120 | pF |
| R_g | Gate Resistance | | | 0.9 | 2.7 | Ω |

Switching Characteristics

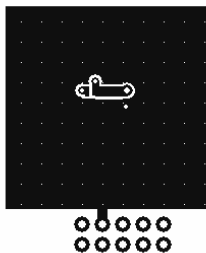
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|--------------|-------------------------------|--|--------------------------------------|----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 15\text{ V}$, $I_D = 16.9\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$ | | 13 | 24 | ns |
| t_r | Rise Time | | | 6 | 12 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 31 | 49 | ns |
| t_f | Fall Time | | | 5 | 10 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | | $V_{GS} = 0\text{ V to }10\text{ V}$ | | 40 | 57 |
| | Total Gate Charge | $V_{GS} = 0\text{ V to }4.5\text{ V}$ | | 18 | 24 | nC |
| Q_{gs} | Total Gate Charge | $V_{DD} = 15\text{ V}$ $I_D = 16.9\text{ A}$ | | 9 | | nC |
| Q_{gd} | Gate to Drain "Miller" Charge | | | 4 | | nC |

Drain-Source Diode Characteristics

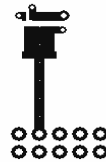
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|----------|---------------------------------------|--|--|------|-----|----|
| V_{SD} | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}$, $I_S = 16.9\text{ A}$ (Note 2) | | 0.83 | 1.2 | V |
| | | $V_{GS} = 0\text{ V}$, $I_S = 1.9\text{ A}$ (Note 2) | | 0.72 | 1.2 | |
| t_{rr} | Reverse Recovery Time | $I_F = 16.9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | | 39 | 62 | ns |
| Q_{rr} | Reverse Recovery Charge | | | 18 | 32 | nC |

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $53\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper



b. $125\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width $< 300\text{ }\mu\text{s}$, Duty cycle $< 2.0\%$.

3. E_{AS} of 144 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1\text{ mH}$, $I_{AS} = 17\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 3\text{ mH}$, $I_{AS} = 7.9\text{ A}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

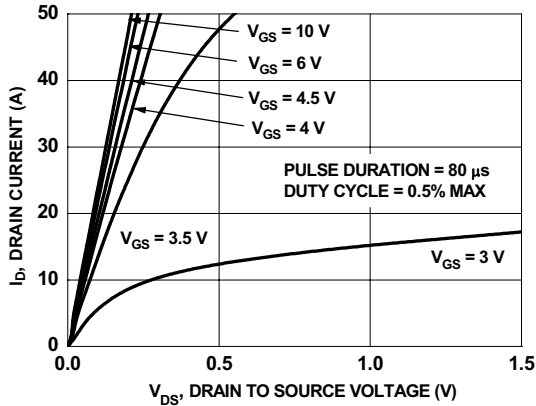


Figure 1. On-Region Characteristics

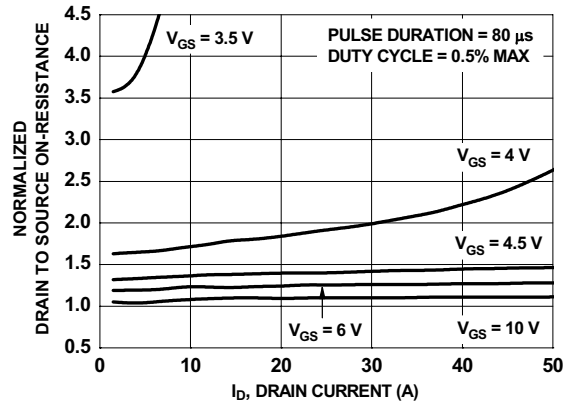


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

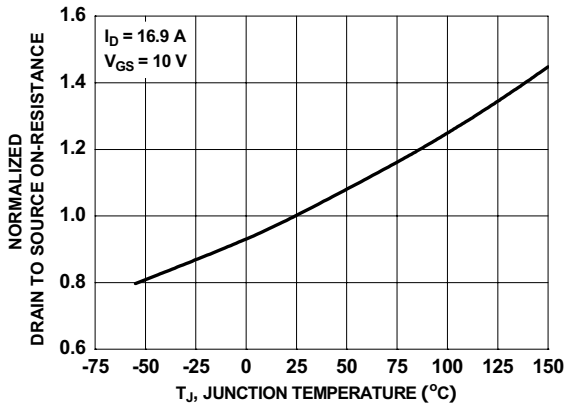


Figure 3. Normalized On-Resistance vs Junction Temperature

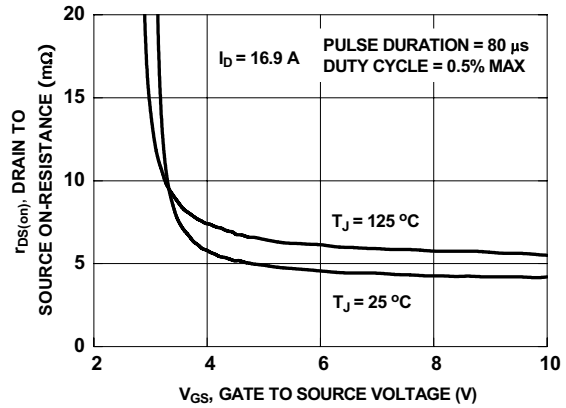


Figure 4. On-Resistance vs Gate to Source Voltage

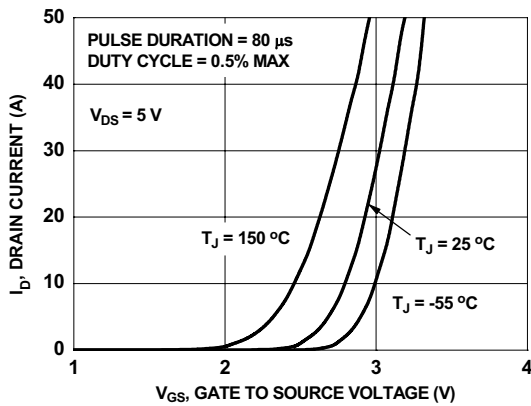


Figure 5. Transfer Characteristics

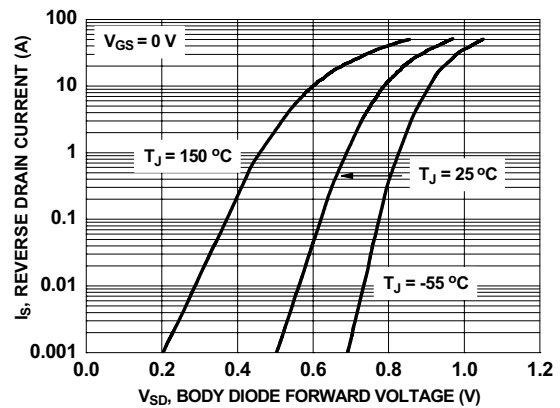


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

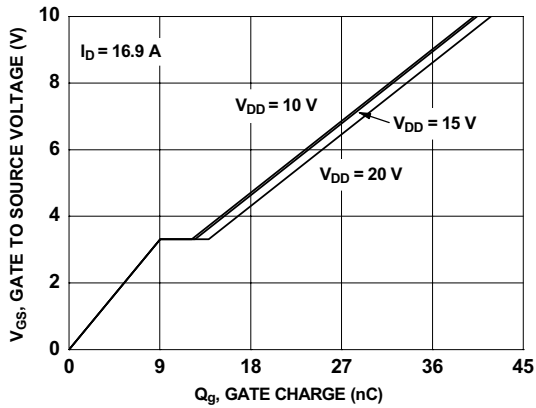


Figure 7. Gate Charge Characteristics

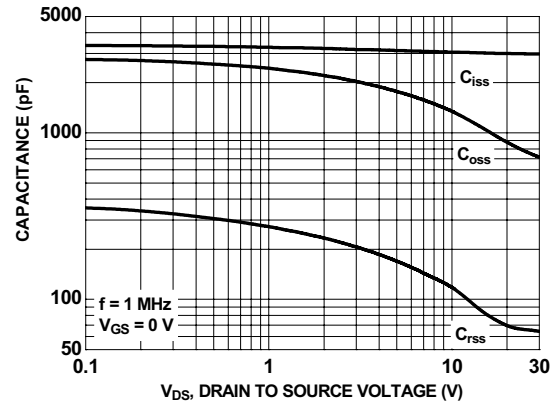


Figure 8. Capacitance vs Drain to Source Voltage

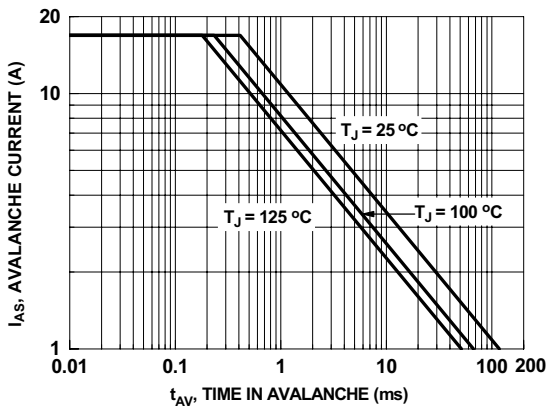


Figure 9. Unclamped Inductive Switching Capability

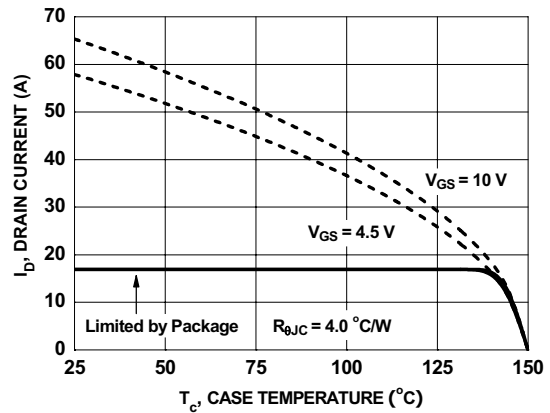


Figure 10. Maximum Continuous Drain Current vs Case Temperature

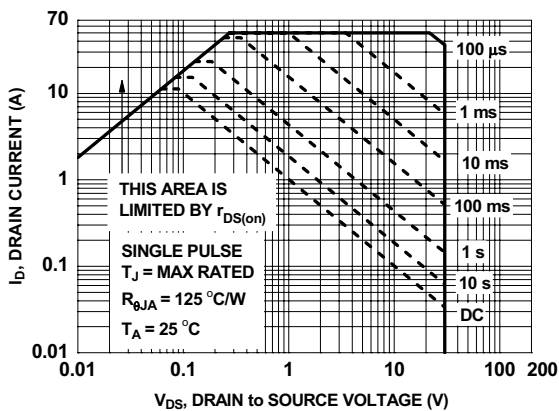


Figure 11. Forward Bias Safe Operating Area

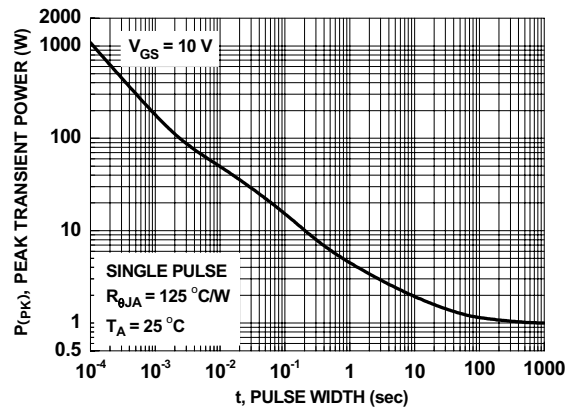


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

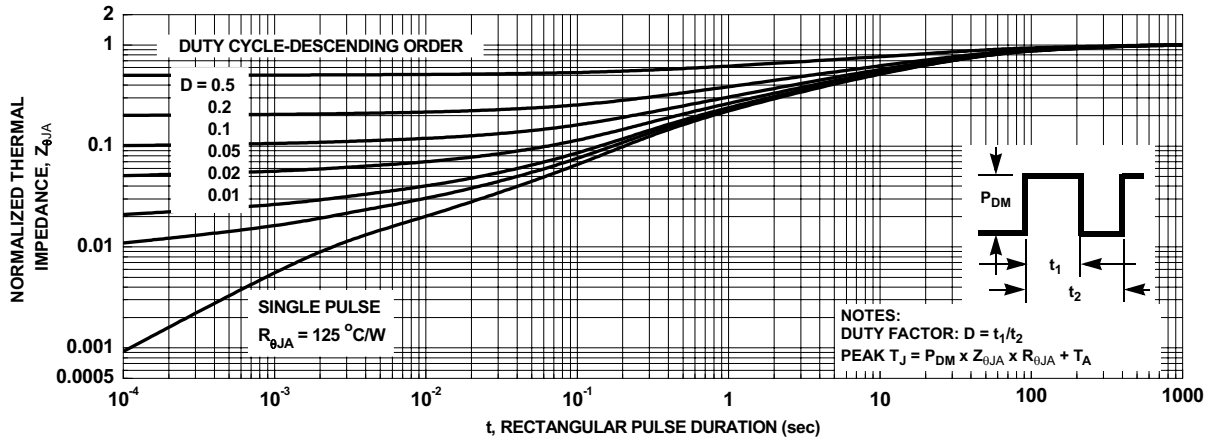
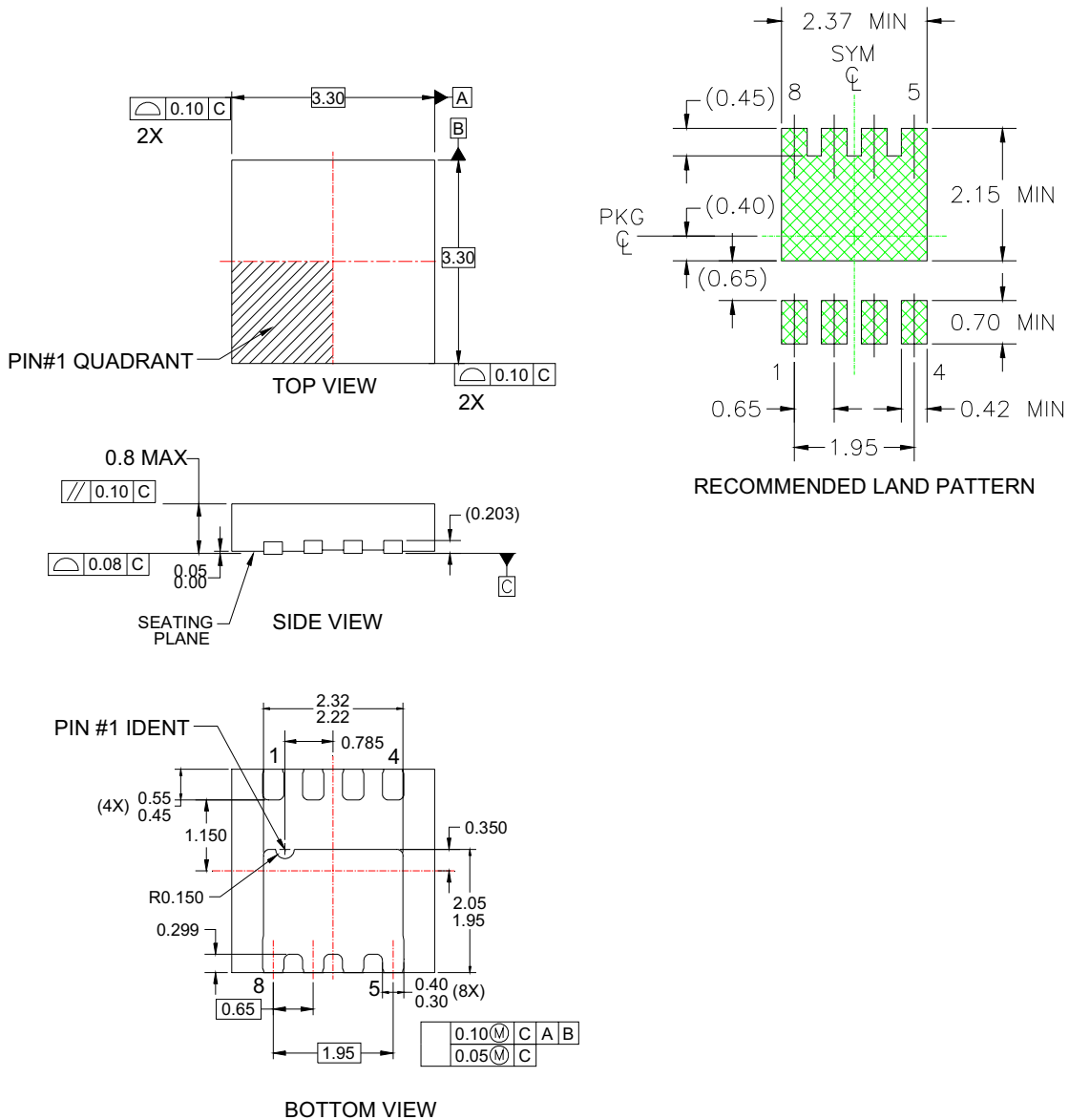


Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout






NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. DRAWING FILE NAME : MLP08SREVA
- E. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY



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