

FDME510PZT

P-Channel PowerTrench® MOSFET

-20 V, -6 A, 37 mΩ

Features

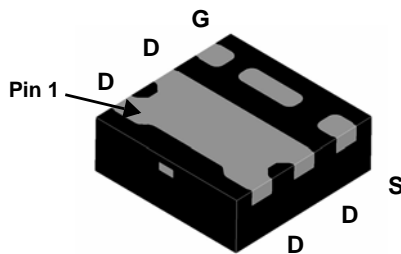
- Max $r_{DS(on)}$ = 37 mΩ at $V_{GS} = -4.5$ V, $I_D = -5$ A
- Max $r_{DS(on)}$ = 50 mΩ at $V_{GS} = -2.5$ V, $I_D = -4$ A
- Max $r_{DS(on)}$ = 65 mΩ at $V_{GS} = -1.8$ V, $I_D = -3$ A
- Max $r_{DS(on)}$ = 100 mΩ at $V_{GS} = -1.5$ V, $I_D = -2$ A
- Low profile: 0.55 mm maximum in the new package MicroFET 1.6x1.6 **Thin**
- Free from halogenated compounds and antimony oxides
- HBM ESD protection level > 2400V (Note3)
- RoHS Compliant



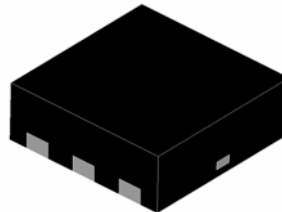
General Description

This device is designed specifically for battery charging or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance.

The MicroFET 1.6x1.6 **Thin** package offers exceptional thermal performance for its physical size and is well suited to switching and linear mode applications.

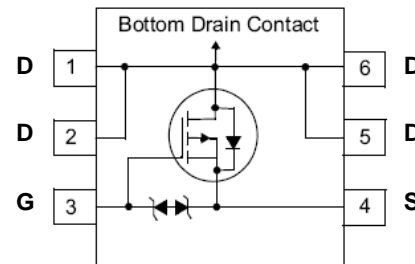


BOTTOM



TOP

MicroFET 1.6x1.6 Thin



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current -Continuous $T_A = 25$ °C (Note 1a)	-6	A
	-Pulsed	-15	
P_D	Power Dissipation for Single Operation $T_A = 25$ °C (Note 1a)	2.1	W
	Power Dissipation for Single Operation $T_A = 25$ °C (Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	175	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
7T	FDME510PZT	MicroFET 1.6x1.6 Thin	7"	8 mm	5000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-13		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8\ \text{V}$, $V_{DS} = 0\ \text{V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\ \mu\text{A}$	-0.4	-0.5	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -4.5\ \text{V}$, $I_D = -5\ \text{A}$		31	37	m Ω
		$V_{GS} = -2.5\ \text{V}$, $I_D = -4\ \text{A}$		38	50	
		$V_{GS} = -1.8\ \text{V}$, $I_D = -3\ \text{A}$		48	65	
		$V_{GS} = -1.5\ \text{V}$, $I_D = -2\ \text{A}$		57	100	
		$V_{GS} = -4.5\ \text{V}$, $I_D = -5\ \text{A}$, $T_J = 125\text{ }^\circ\text{C}$		40	60	
g_{FS}	Forward Transconductance	$V_{DS} = -5\ \text{V}$, $I_D = -5\ \text{A}$		21		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		1120	1490	pF
C_{oss}	Output Capacitance			155	210	pF
C_{rss}	Reverse Transfer Capacitance			140	210	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\ \text{V}$, $I_D = -5\ \text{A}$ $V_{GS} = -4.5\ \text{V}$, $R_{GEN} = 6\ \Omega$		6.5	13	ns
t_r	Rise Time			10	16	ns
$t_{d(off)}$	Turn-Off Delay Time			93	149	ns
t_f	Fall Time			54	86	ns
Q_g	Total Gate Charge			16	22	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = -10\ \text{V}$, $I_D = -5\ \text{A}$		1.6		nC
Q_{gd}	Gate to Drain "Miller" Charge	$V_{GS} = -4.5\ \text{V}$		4		nC

Drain-Source Diode Characteristics

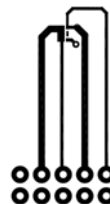
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = -1.6\ \text{A}$ (Note 2)		-0.6	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -5\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		38	61	ns
Q_{rr}	Reverse Recovery Charge			16	29	nC

Notes:

- $R_{\theta JA}$ is determined with the device mounted on a $1\ \text{in}^2$ pad 2 oz copper pad on a $1.5 \times 1.5\ \text{in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $60\text{ }^\circ\text{C/W}$ when mounted on a $1\ \text{in}^2$ pad of 2 oz copper.



b. $175\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < $300\ \mu\text{s}$, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

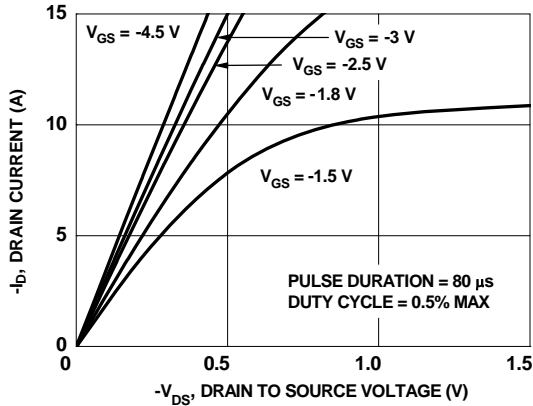


Figure 1. On Region Characteristics

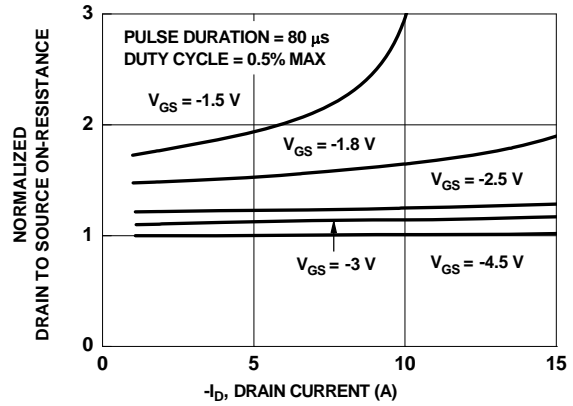


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

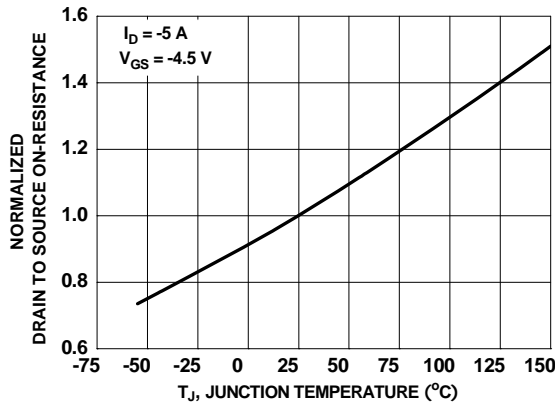


Figure 3. Normalized On Resistance vs Junction Temperature

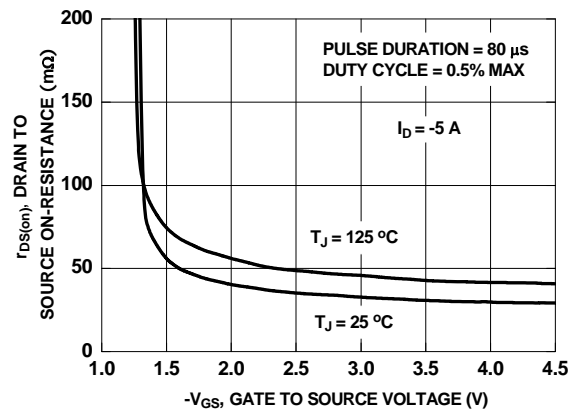


Figure 4. On-Resistance vs Gate to Source Voltage

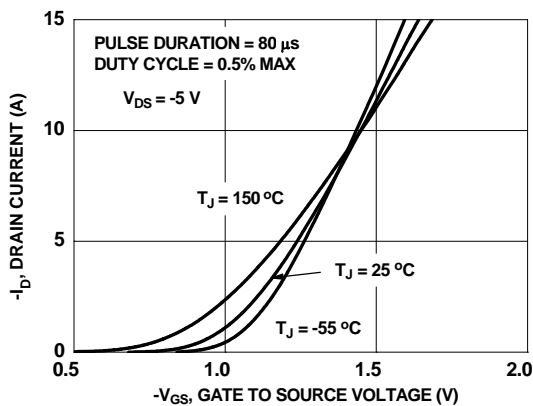


Figure 5. Transfer Characteristics

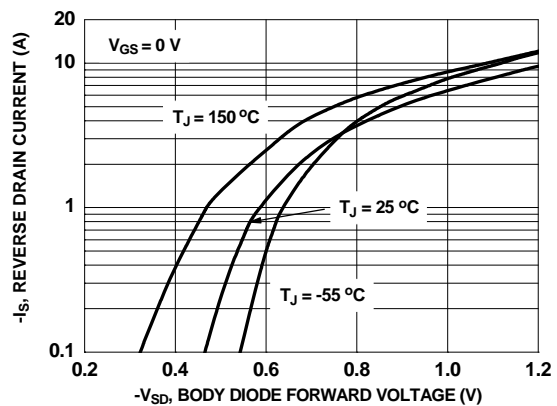


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

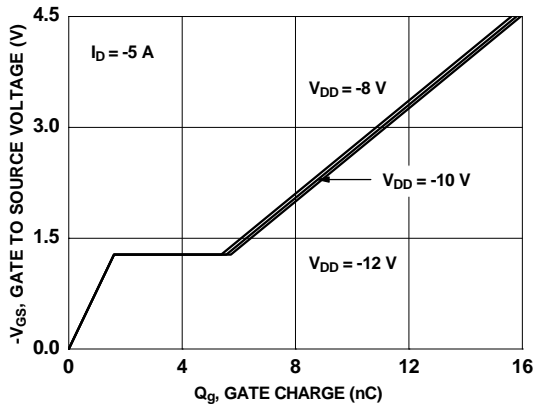


Figure 7. Gate Charge Characteristics

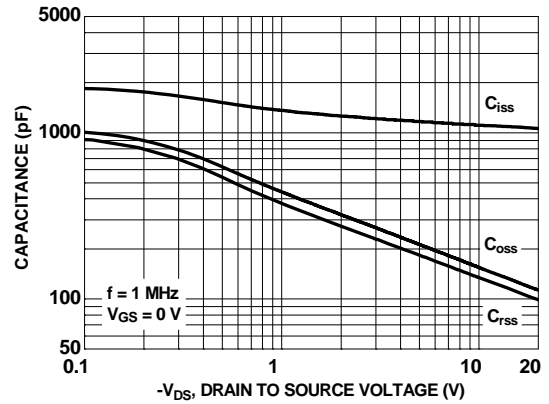


Figure 8. Capacitance vs Drain to Source Voltage

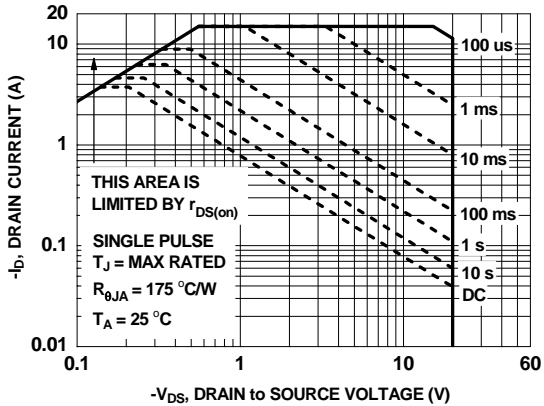


Figure 9. Forward Bias Safe Operating Area

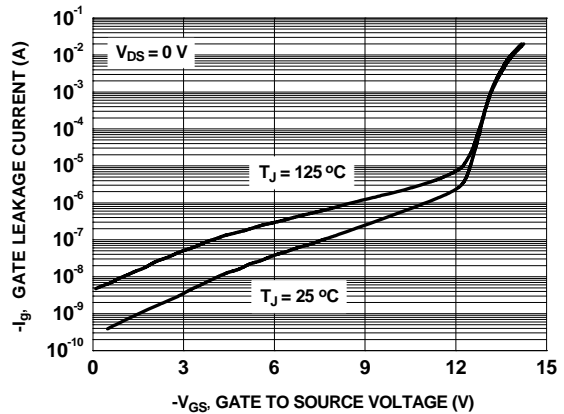


Figure 10. Gate Leakage Current vs Gate to Source Voltage

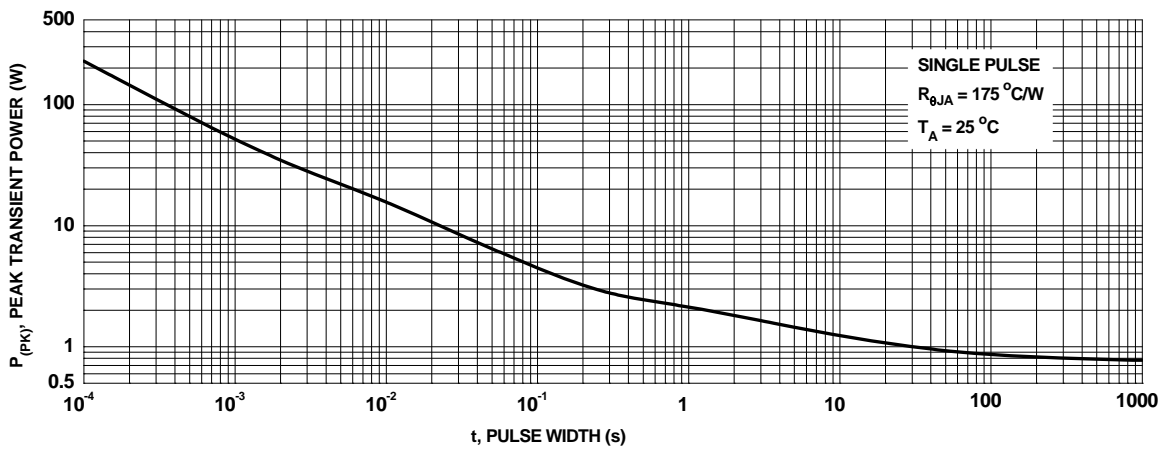


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

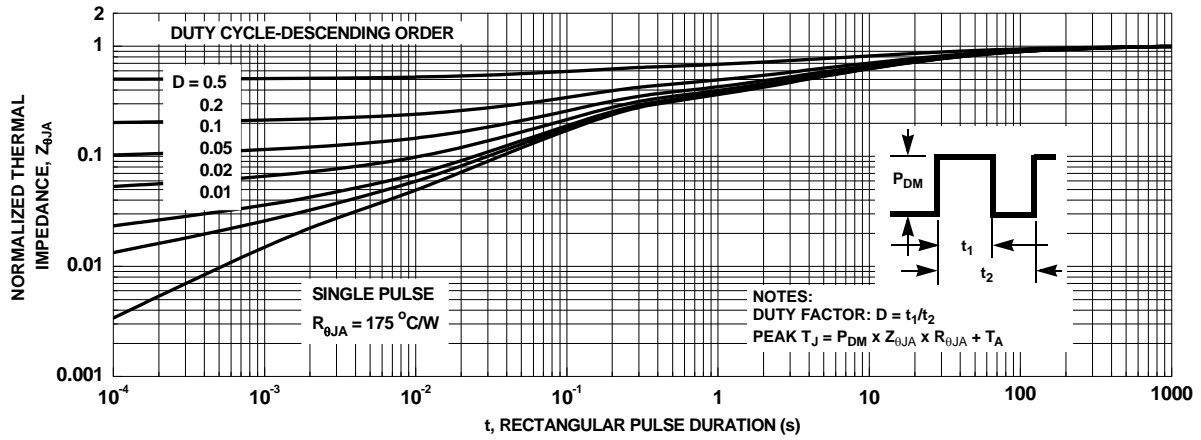
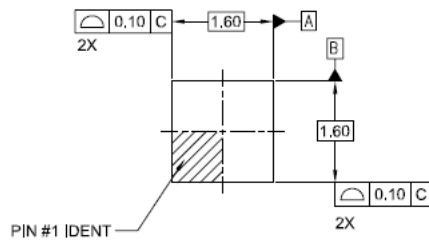
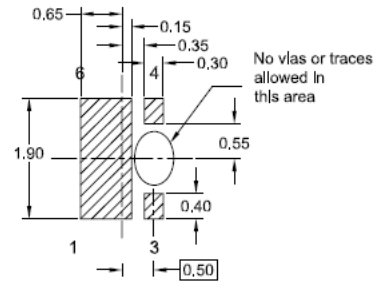


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

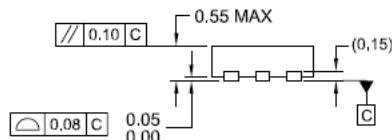
Dimensional Outline and Pad Layout



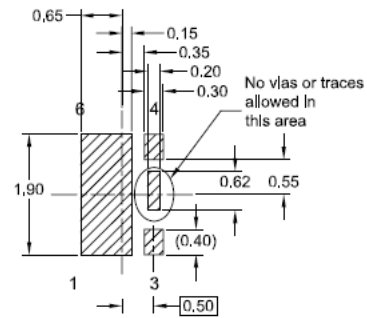
TOP VIEW



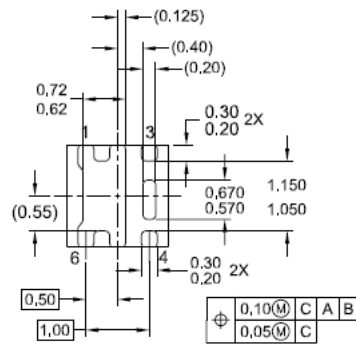
RECOMMENDED LAND PATTERN OPT 1



SIDE VIEW



RECOMMENDED LAND PATTERN OPT 2



BOTTOM VIEW






NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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