

FDS4559_F085

60V Complementary PowerTrench® MOSFET

General Description

This complementary MOSFET device is produced using Fairchild's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

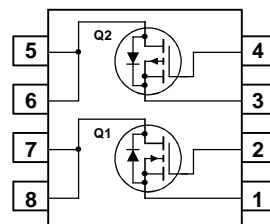
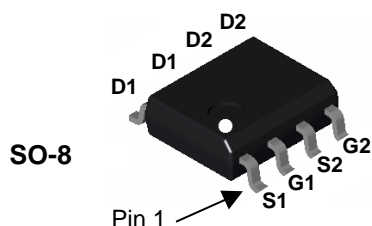
Applications

- DC/DC converter
- Power management
- LCD backlight inverter



Features

- **Q1: N-Channel**
4.5 A, 60 V $R_{DS(on)} = 55 \text{ m}\Omega @ V_{GS} = 10\text{V}$
 $R_{DS(on)} = 75 \text{ m}\Omega @ V_{GS} = 4.5\text{V}$
- **Q2: P-Channel**
-3.5 A, -60 V $R_{DS(on)} = 105 \text{ m}\Omega @ V_{GS} = -10\text{V}$
 $R_{DS(on)} = 135 \text{ m}\Omega @ V_{GS} = -4.5\text{V}$
- Qualified to AEC Q101
- RoHS Compliant



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DSS}	Drain-Source Voltage	60	-60	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous (Note 1a)	4.5	-3.5	A
	- Pulsed	20	-20	
P_D	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1.2		
	(Note 1c)	2		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS4559	FDS4559_F085	13"	12mm	2500 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

Drain-Source Avalanche Ratings (Note 1)

W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 30\text{ V}$, $I_D = 4.5\text{ A}$	Q1			90	mJ
I_{AR}	Maximum Drain-Source Avalanche Current		Q1			4.5	A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	Q1 Q2	60 -60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C $I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	Q1 Q2		58 -49		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}$, $V_{GS} = 0\text{ V}$ $V_{DS} = -48\text{ V}$, $V_{GS} = 0\text{ V}$	Q1 Q2			1 -1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$ $V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$	Q1 Q2			± 100 ± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ $V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	Q1 Q2	1 -1	2.2 -1.6	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C $I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	Q1 Q2		-5.5 4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 4.5\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 4.5\text{ A}$, $T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}$, $I_D = 4\text{ A}$ $V_{GS} = -10\text{ V}$, $I_D = -3.5\text{ A}$ $V_{GS} = -10\text{ V}$, $I_D = -3.5\text{ A}$, $T_J = 125^\circ\text{C}$ $V_{GS} = -4.5\text{ V}$, $I_D = -3.1\text{ A}$	Q1 Q2		42 72 55 82 130 105	55 94 75 105 190 135	m Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 5\text{ V}$ $V_{GS} = -10\text{ V}$, $V_{DS} = -5\text{ V}$	Q1 Q2	20 -20			A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 4.5\text{ A}$ $V_{DS} = -5\text{ V}$, $I_D = -3.5\text{ A}$	Q1 Q2		14 9		S

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1 $V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$	Q1 Q2		650 759		pF
C_{oss}	Output Capacitance	Q1 Q2	Q1 Q2		80 90		pF
C_{riss}	Reverse Transfer Capacitance	$V_{DS} = -30\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$	Q1 Q2		35 39		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 30\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		11 7	20 14	ns
t_r	Turn-On Rise Time		Q1 Q2		8 10	18 20	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -30\text{ V}$, $I_D = -1\text{ A}$, $V_{GS} = -10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		19 19	35 34	ns
t_f	Turn-Off Fall Time		Q1 Q2		6 12	15 22	ns
Q_g	Total Gate Charge	Q1 $V_{DS} = 30\text{ V}$, $I_D = 4.5\text{ A}$, $V_{GS} = 10\text{ V}$	Q1 Q2		12.5 15	18 21	nC
Q_{gs}	Gate-Source Charge		Q1 Q2		2.4 2.5		nC
Q_{gd}	Gate-Drain Charge	$V_{DS} = -30\text{ V}$, $I_D = -3.5\text{ A}$, $V_{GS} = -10\text{ V}$	Q1 Q2		2.6 3.0		nC

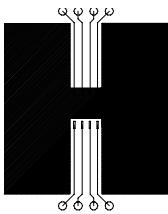
Electrical Characteristics (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1			1.3	A
			Q2			-1.3	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)	Q1		0.8	1.2	V
			Q2		-0.8	-1.2	

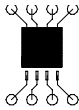
Drain-Source Diode Characteristics and Maximum Ratings

Notes:

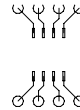
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper



b) 125°C/W when mounted on a $.02\text{ in}^2$ pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty Cycle $< 2.0\%$

Typical Characteristics: Q2

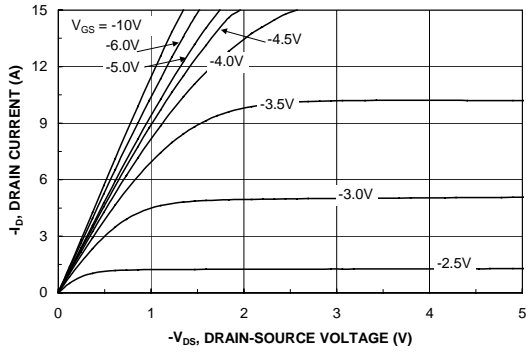


Figure 1. On-Region Characteristics.

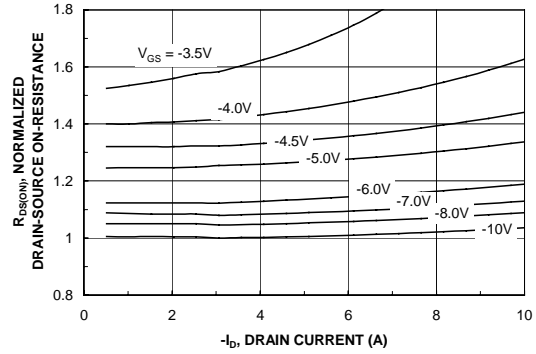


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

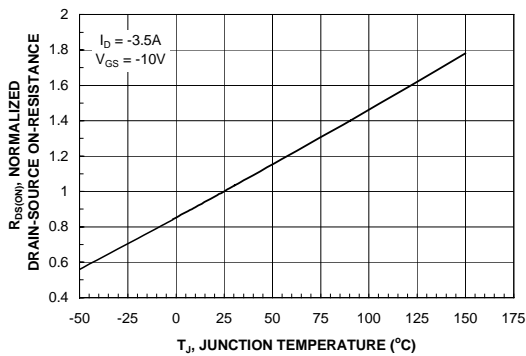


Figure 3. On-Resistance Variation with Temperature.

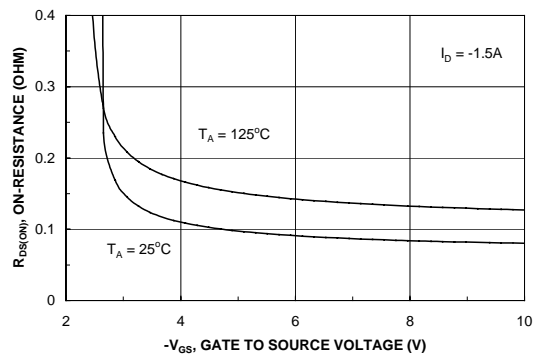


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

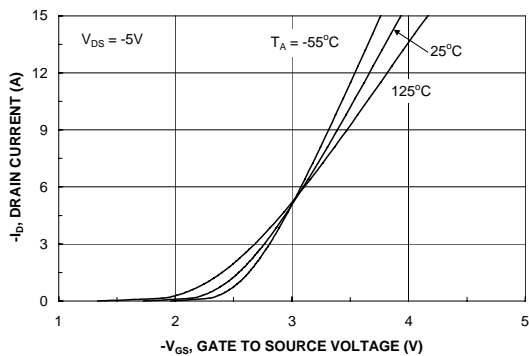


Figure 5. Transfer Characteristics.

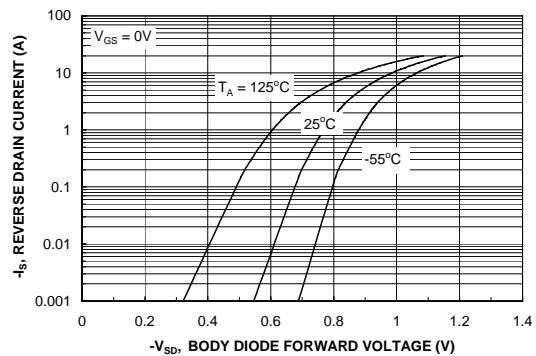


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

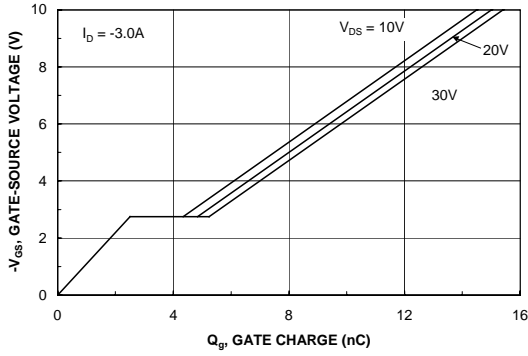


Figure 7. Gate Charge Characteristics.

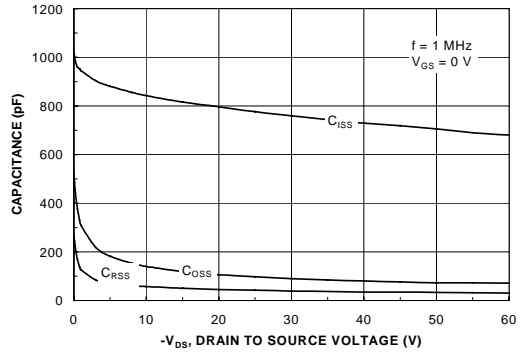


Figure 8. Capacitance Characteristics.

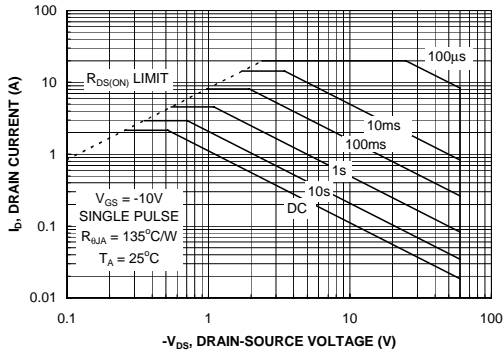


Figure 9. Maximum Safe Operating Area.

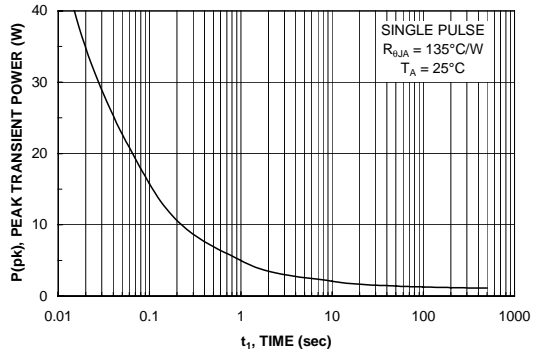


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q1

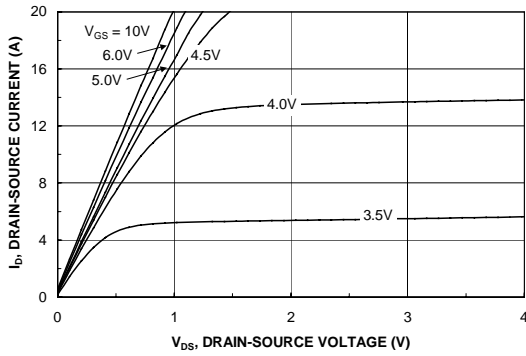


Figure 11. On-Region Characteristics.

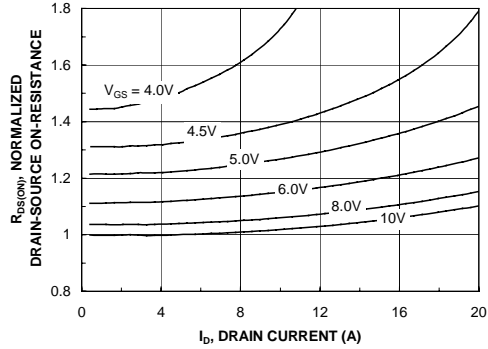


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

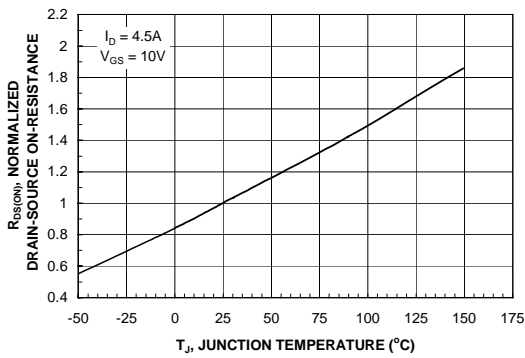


Figure 13. On-Resistance Variation with Temperature.

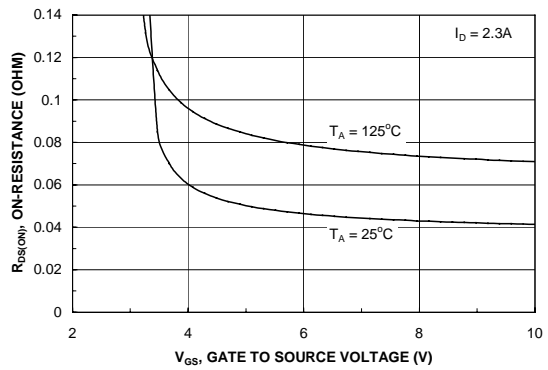


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

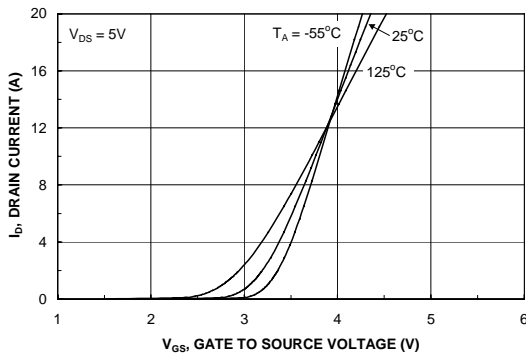


Figure 15. Transfer Characteristics.

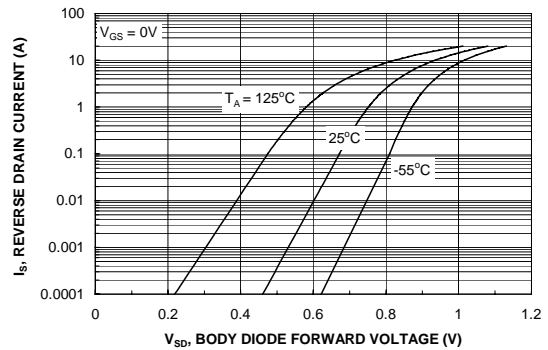


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1

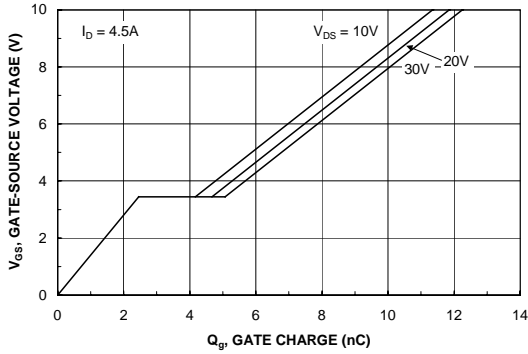


Figure 17. Gate Charge Characteristics.

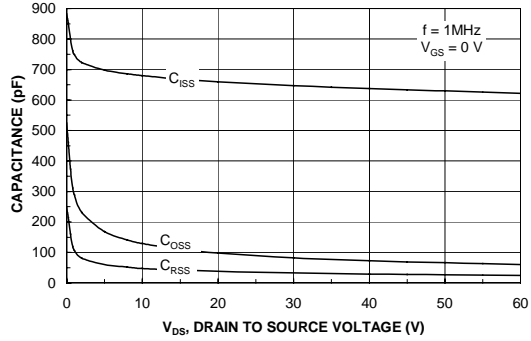


Figure 18. Capacitance Characteristics.

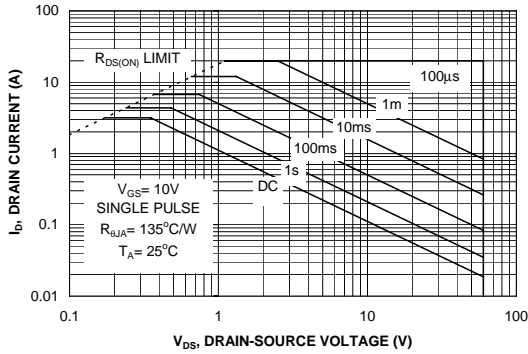


Figure 19. Maximum Safe Operating Area.

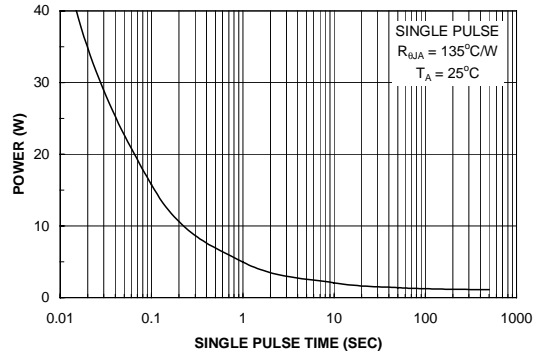


Figure 20. Single Pulse Maximum Power Dissipation.

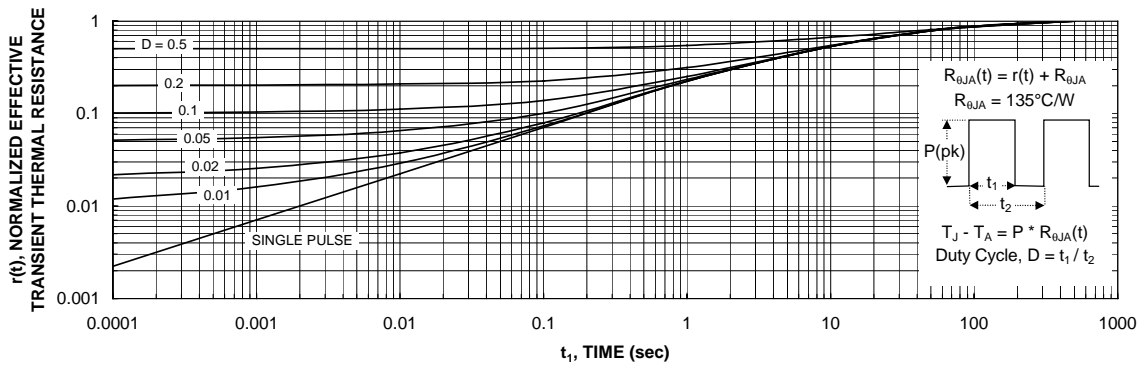







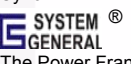
Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- | | | | |
|---|---|---|---|
| Build it Now™ | FRFET® | Programmable Active Droop™ | the power franchise |
| CorePLUS™ | Global Power ResourceSM | QFET® | TinyBoost™ |
| CorePOWER™ | Green FPS™ | QS™ | TinyBuck™ |
| CROSSVOLT™ | Green FPS™ e-Series™ | Quiet Series™ | TinyLogic® |
| CTL™ | GTO™ | RapidConfigure™ | TINYOPTO™ |
| Current Transfer Logic™ | IntelliMAX™ |  Saving our world, 1mW /W /kW at a time™ | TinyPower™ |
| EcoSPARK® | ISOPLANAR™ | SmartMax™ | TinyPWM™ |
| EfficientMax™ | MegaBuck™ | SMART START™ | TinyWire™ |
| EZSWITCH™ * | MICROCOUPLER™ | SPM® | µSerDes™ |
|  | MicroFET™ | STEALTH™ |  |
|  | MicroPak™ | SuperFET™ | UHC® |
| Fairchild® | MillerDrive™ | SuperSOT™-3 | Ultra FRFET™ |
| Fairchild Semiconductor® | MotionMax™ | SuperSOT™-6 | UniFET™ |
| FACT Quiet Series™ | Motion-SPM™ | SuperSOT™-8 | VCX™ |
| FACT® | OPTOLOGIC® | SupreMOS™ | VisualMax™ |
| FAST® | OPTOPLANAR® | SyncFET™ | XS™ |
| FastvCore™ |  |  | |
| FlashWriter® * | PDP SPM™ | The Power Franchise® | |
| FlashWriter® * | Power-SPM™ | | |
| FPS™ | PowerTrench® | | |
| F-PFS™ | PowerXS™ | | |

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.