

FDZ391P

P-Channel 1.5 V PowerTrench® Thin WL-CSP MOSFET

-20 V, -3 A, 85 mΩ

Features

- Max $r_{DS(on)}$ = 85 mΩ at $V_{GS} = -4.5$ V, $I_D = -1$ A
- Max $r_{DS(on)}$ = 123 mΩ at $V_{GS} = -2.5$ V, $I_D = -1$ A
- Max $r_{DS(on)}$ = 200 mΩ at $V_{GS} = -1.5$ V, $I_D = -1$ A
- Occupies only 1.5 mm² of PCB area
- **Ultra-thin package:** less than 0.4 mm height when mounted to PCB
- RoHS Compliant

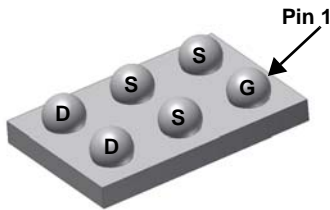


General Description

Designed on Fairchild's advanced 1.5 V PowerTrench process with state of the art "low pitch" Thin WLCSP packaging process, the FDZ391P minimizes both PCB space and $r_{DS(on)}$. This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low $r_{DS(on)}$.

Applications

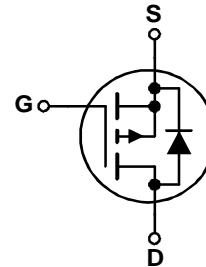
- Battery management
- Load switch
- Battery protection



BOTTOM



TOP



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

| Symbol | Parameter | Rated | Units |
|----------------|---|-------------|-------|
| V_{DS} | Drain to Source Voltage | -20 | V |
| V_{GS} | Gate to Source Voltage | ±8 | V |
| I_D | Drain Current -Continuous $T_A = 25$ °C (Note 1a) | -3 | A |
| | -Pulsed | -15 | |
| P_D | Power Dissipation $T_A = 25$ °C (Note 1a) | 1.9 | W |
| | Power Dissipation $T_A = 25$ °C (Note 1b) | 0.9 | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | °C |

Thermal Characteristics

| | | | |
|-----------------|---|-----|------|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 65 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1b) | 133 | |

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|---------|-------------|-----------|------------|------------|
| 6 | FDZ391P | WL-CSP Thin | 7" | 8 mm | 5000 units |

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | |
|--------------------------------------|---|--|-----|-----|-----------|----------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = -250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$ | -20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ | | -12 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = -16\text{ V}$, $V_{GS} = 0\text{ V}$ | | | -1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = \pm 8\text{ V}$, $V_{DS} = 0\text{ V}$ | | | ± 100 | nA |

On Characteristics

| | | | | | | |
|--|--|--|------|------|------|----------------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}$, $I_D = -250\text{ }\mu\text{A}$ | -0.4 | -0.6 | -1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ | | 2 | | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$ | Drain to Source On Resistance | $V_{GS} = -4.5\text{ V}$, $I_D = -1\text{ A}$ | | 74 | 85 | m Ω |
| | | $V_{GS} = -2.5\text{ V}$, $I_D = -1\text{ A}$ | | 90 | 123 | |
| | | $V_{GS} = -1.5\text{ V}$, $I_D = -1\text{ A}$ | | 140 | 200 | |
| | | $V_{GS} = -4.5\text{ V}$, $I_D = -1\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$ | | 100 | 123 | |
| $I_{D(on)}$ | On to State Drain Current | $V_{GS} = -4.5\text{ V}$, $V_{DS} = -5\text{ V}$ | -10 | | | A |
| g_{FS} | Forward Transconductance | $V_{DS} = -5\text{ V}$, $I_D = -1\text{ A}$ | | 7 | | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|---|--------------------|-----|------|----|
| C_{iss} | Input Capacitance | $V_{DS} = -10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$ | | 800 | 1065 | pF |
| C_{oss} | Output Capacitance | | | 155 | 205 | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 90 | 135 | pF |
| R_g | Gate Resistance | | $f = 1\text{ MHz}$ | | 9 | |

Switching Characteristics

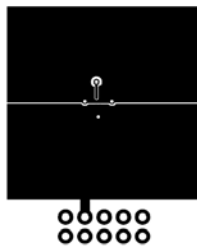
| | | | | | | |
|--------------|-------------------------------|---|--------------------------|----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = -10\text{ V}$, $I_D = -1\text{ A}$ $V_{GS} = -4.5\text{ V}$, $R_{GEN} = 6\text{ }\Omega$ | | 11 | 20 | ns |
| t_r | Rise Time | | | 10 | 20 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 50 | 80 | ns |
| t_f | Fall Time | | | 30 | 48 | ns |
| Q_g | Total Gate Charge | | $V_{GS} = -4.5\text{ V}$ | | 9 | 13 |
| Q_{gs} | Gate to Source Gate Charge | $V_{DD} = -10\text{ V}$ $I_D = -1\text{ A}$ | | 1 | | nC |
| Q_{gd} | Gate to Drain "Miller" Charge | | | 2 | | nC |

Drain-Source Diode Characteristics

| | | | | | | |
|----------|---|--|--|------|------|----|
| I_S | Maximum continuous Drain-Source Diode Forward Current | | | | -1.1 | A |
| V_{SD} | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}$, $I_S = -1.1\text{ A}$ (Note 2) | | -0.7 | -1.2 | V |
| t_{rr} | Reverse Recovery Time | $I_F = -1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | | 21 | | ns |
| Q_{rr} | Reverse Recovery Charge | | | 5 | | nC |

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 65 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b. 133 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

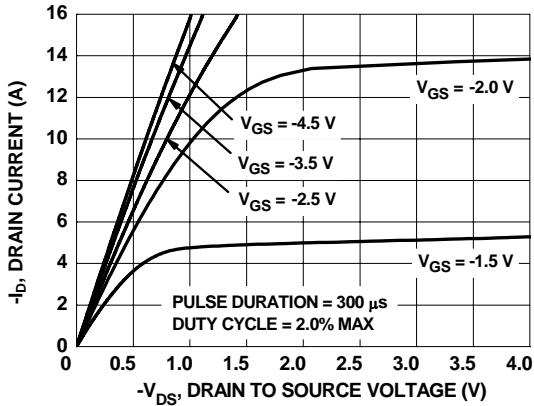


Figure 1. On Region Characteristics

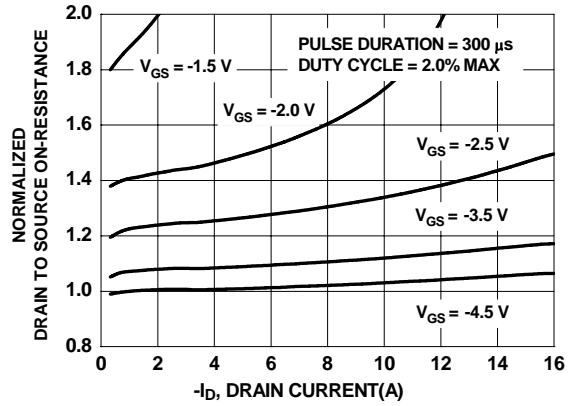


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

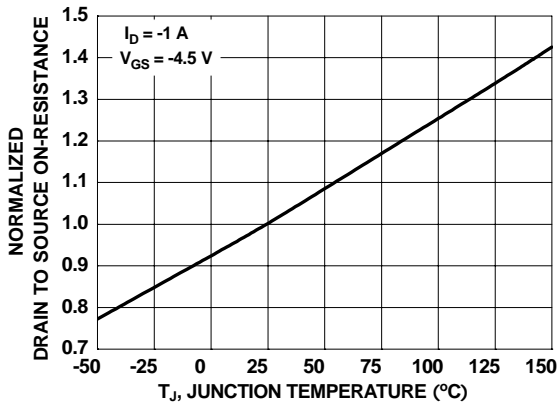


Figure 3. Normalized On Resistance vs Junction Temperature

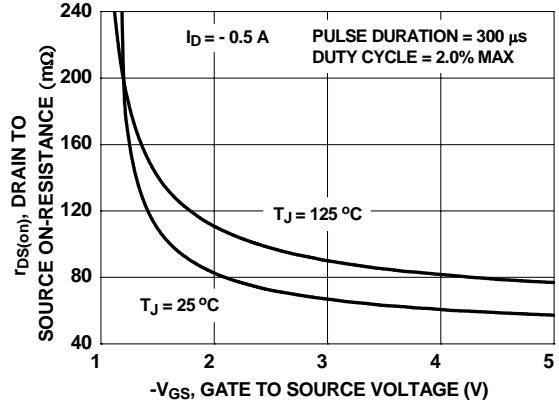


Figure 4. On-Resistance vs Gate to Source Voltage

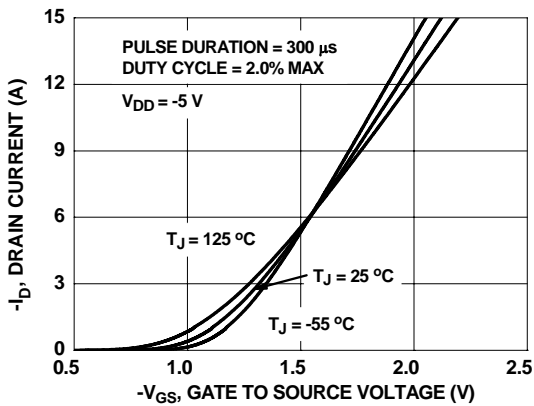


Figure 5. Transfer Characteristics

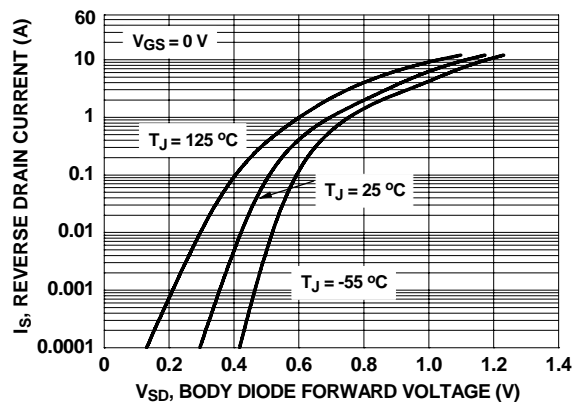


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

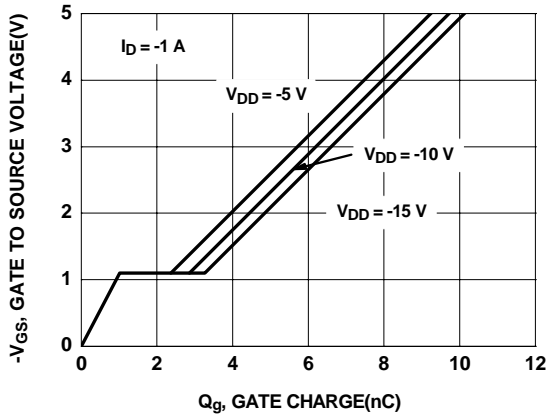


Figure 7. Gate Charge Characteristics

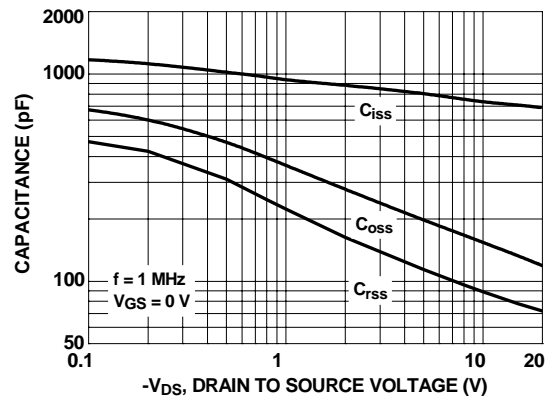


Figure 8. Capacitance vs Drain to Source Voltage

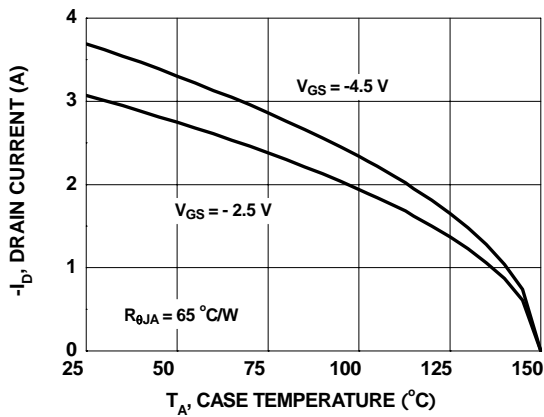


Figure 9. Maximum Continuous Drain Current vs Ambient Temperature

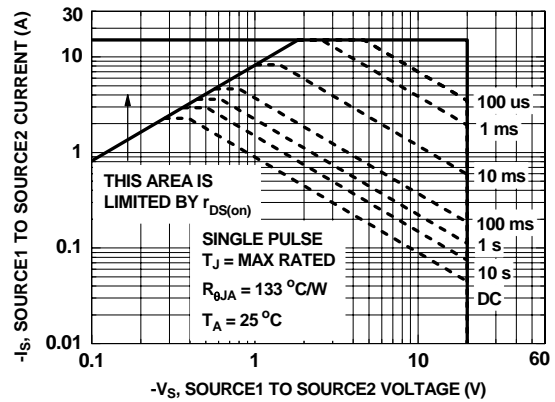


Figure 10. Forward Bias Safe Operating Area

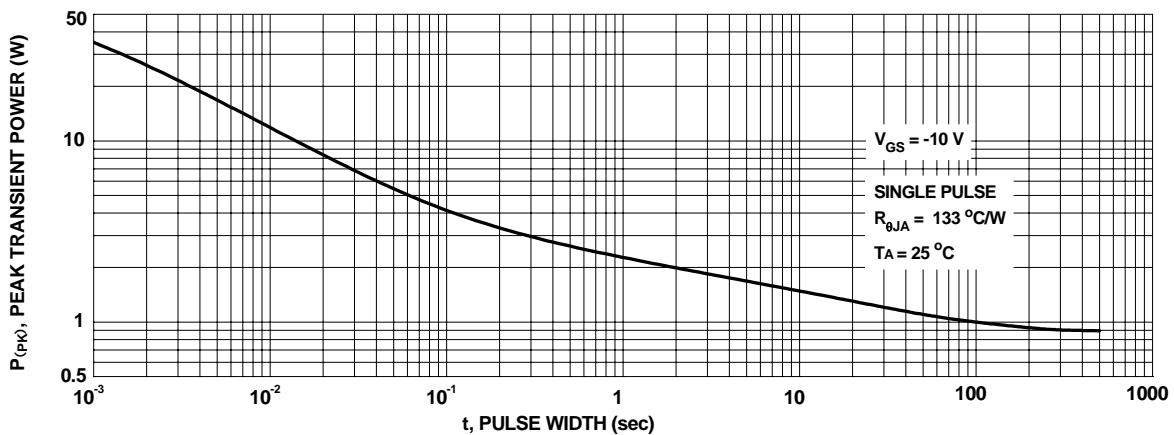


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

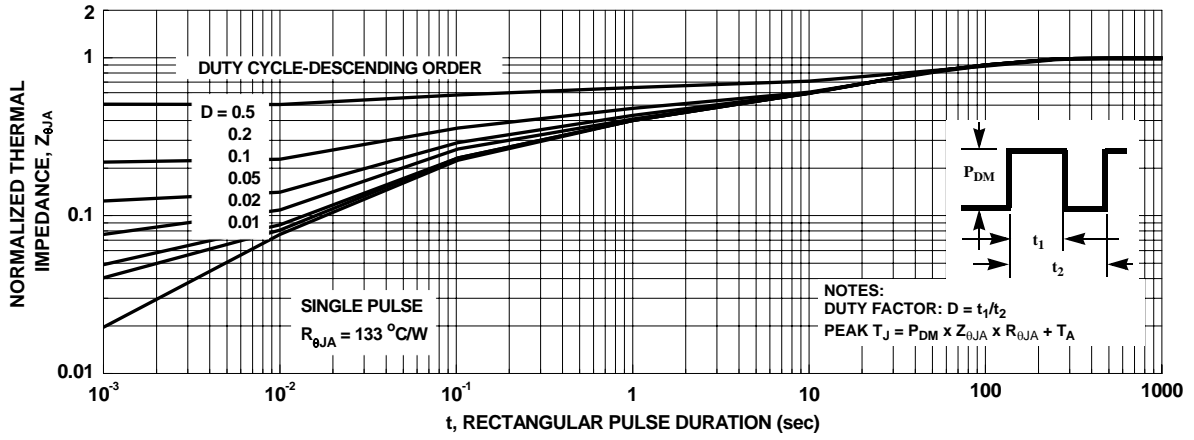
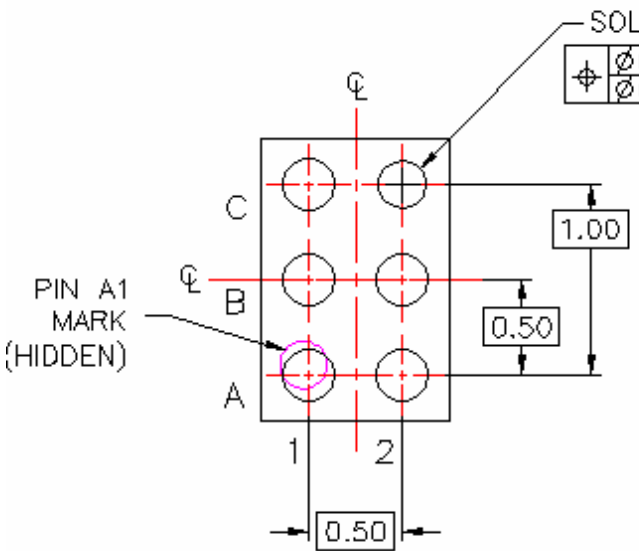
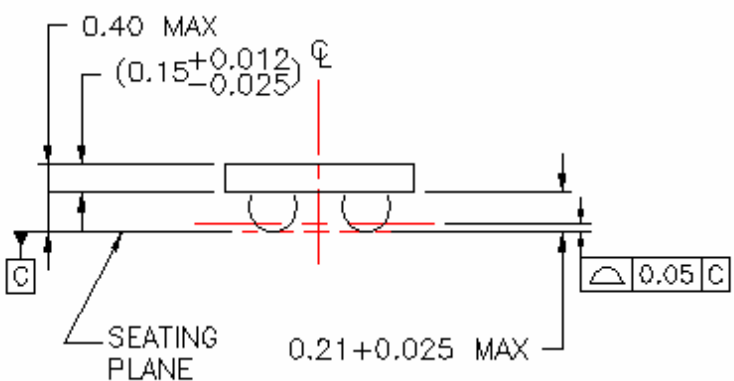
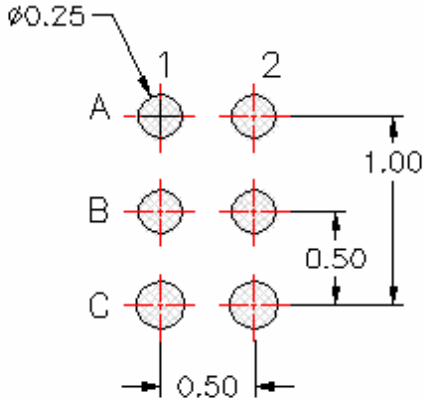
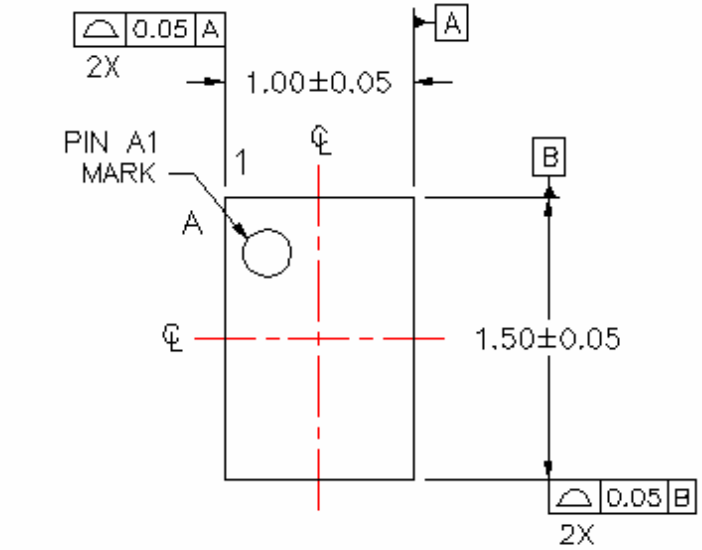


Figure 12. Transient Thermal Response Curve

Dimensional Outline and Pad Layout



| | | | | |
|--------|-------------|---|---|---|
| ϕ | $\phi 0.10$ | C | A | B |
| ϕ | $\phi 0.05$ | C | | |

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- B) DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994
- D) TERMINAL CONFIGURATION TABLE:







| GATE | SOURCE | DRAIN |
|------|------------|--------|
| A1 | A2, B1, B2 | C1, C2 |

E) DRAWING FILENAME: MKT-UC006AEREV2



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Rev. I37