

# FOD0721, FOD0720, FOD0710

## High CMR, 25Mbit/sec Logic Gate Optocoupler

### Features

- 20kV/μs minimum CMR
- 40ns max. propagation delay
- Data Rate, Non-Return Zero Coding
  - 25Mbit/sec (FOD0721 and FOD0720)
  - 12.5Mbit/sec (FOD0710)
- Pulse Width Distortion
  - 6ns (FOD0721)
  - 8ns (FOD0720 and FOD0710)
- +5V CMOS compatibility
- Extended industrial temperature range
  - -40 to 100°C temperature range
- Safety and regulatory approvals
  - UL1577, 3750 VACrms for 1 min. (File #E90700, Volume 2)
  - IEC60747-5-2 pending approval

### Description

The FOD0721/0720/0710 family utilizes Fairchild's patented coplanar packaging technology, Optoplanar®, and optimized IC design to guarantee minimum 20kV/μs Common Mode Noise Rejection (CMR) rating.

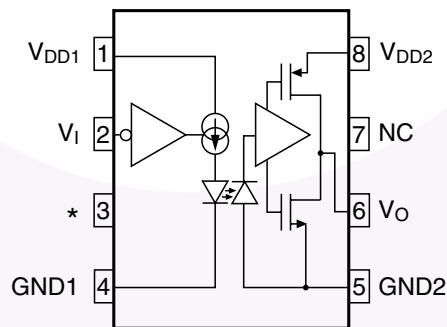
These high-speed logic gate optocouplers consist of a high-speed AlGaAs LED driven by a CMOS IC coupled to a CMOS detector IC, comprising an integrated photodiode, a high-speed transimpedance amplifier and a voltage comparator with an output driver. The CMOS technology coupled to the high efficiency of the LED achieves low power consumption as well as very high speed (40ns propagation delay, 6ns pulse width distortion).

These devices are available in a compact 8-pin small outline package.

### Applications

- Industrial fieldbus communications
  - Profibus, DeviceNet, CAN, RS485
- Programmable logic control
- Isolated data acquisition system

### Functional Schematic



\*: Pin 3 must be left unconnected

Truth Table

V <sub>I</sub>	LED	V <sub>O</sub>
H	OFF	H
L	ON	L

## Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	V <sub>DD1</sub>	Input Supply Voltage
2	V <sub>I</sub>	Input Data
3		LED Anode – must be left unconnected
4	GND1	Input Ground
5	GND2	Output Ground
6	V <sub>O</sub>	Output Data
7	NC	Not Connected
8	V <sub>DD2</sub>	Output Supply Voltage

## Absolute Maximum Ratings (T<sub>A</sub> = 25°C unless otherwise specified.)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
T <sub>OPR</sub>	Operating Temperature	-40 to +100	°C
T <sub>SOL</sub>	Lead Solder Temperature	260 for 10 sec	°C
	Reflow Temperature Profile (Refer to Relow Profile)		
V <sub>DD1</sub>	Input Supply Voltage	0 to 6.0	V
V <sub>I</sub>	Input Voltage	-0.5 to V <sub>DD1</sub> + 0.5	V
I <sub>I</sub>	Input DC Current	-10 to +10	mA
V <sub>DD2</sub>	Output Supply Voltage	0 to 6.0	V
V <sub>D</sub>	Output Voltage	-0.5 to V <sub>DD2</sub> + 0.5	V
I <sub>O</sub>	Average Output Current	10	mA
PD1	Input Power Dissipation	90	mW
PD2	Output Power Dissipation	70	mW

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
T <sub>OPR</sub>	Ambient Operating Temperature	-40	+100	°C
V <sub>DD1</sub> , V <sub>DD2</sub>	Supply Voltages	4.5	5.5	V
V <sub>IH</sub>	Logic High Input Voltage	2.0	V <sub>DD1</sub>	V
V <sub>IL</sub>	Logic Low Input Voltage	0	0.8	V
t <sub>r</sub> , t <sub>f</sub>	Input Signal Rise and Fall Time		1.0	ms

- A 0.1μF bypass capacitor must be connected between pins 1 and 4, and 5 and 8
- Pin 3 must be left unconnected

**Electrical Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $100^{\circ}\text{C}$  and  $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ , all typicals are at  $T_A = 25^{\circ}\text{C}$ ,  $V_{DD} = 5\text{V}$ )

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>INPUT CHARACTERISTICS</b>						
$I_{DD1L}$	Logic Low Input Supply Current	$V_I = 0\text{V}$		6.5	10.0	mA
$I_{DD1H}$	Logic High Input Supply Current	$V_I = V_{DD1}$		0.8	3.0	mA
$I_{DD1}$	Input Supply Current				13.0	mA
$I_I$	Input Current		-10		+10	$\mu\text{A}$
<b>OUTPUT CHARACTERISTICS</b>						
$I_{DD2L}$	Logic Low Output Supply Current	$V_I = 0\text{V}$		5.5	9	mA
$I_{DD2H}$	Logic High Output Supply Current	$V_I = V_{DD1}$		5.3	9	mA
$V_{OH}$	Logic High Output Voltage	$I_O = -20\mu\text{A}$ , $V_I = V_{IH}$	4.4	5.0		V
$V_{OH}$		$I_O = -4\text{mA}$ , $V_I = V_{IH}$	4.0	4.8		V
$V_{OL}$	Logic Low Output Voltage	$I_O = 20\mu\text{A}$ , $V_I = V_{IL}$		0	0.1	V
$V_{OL}$		$I_O = 4\text{mA}$ , $V_I = V_{IL}$		0.5	1.0	V

**Isolation Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$  unless otherwise specified.)

Symbol	Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
$V_{ISO}$	Input-Output Isolation Voltage	$f = 60\text{Hz}$ , $t = 1.0\text{ min}$ , $I_{I-O} \leq 10\mu\text{A}^{(1)(2)}$	3750			$V_{aCRMS}$
$R_{ISO}$	Isolation Resistance	$V_{I-O} = 500\text{V}^{(1)}$	$10^{11}$			$\Omega$
$C_{ISO}$	Isolation Capacitance	$V_{I-O} = 0$ , $f = 1.0\text{MHz}^{(1)}$		0.2		pF

\*All typicals at  $T_A = 25^{\circ}\text{C}$ **Notes:**

- Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
- 3,750 VAC RMS for 1 minute duration is equivalent to 4,500 VAC RMS for 1 second duration.

**Switching Characteristics** ( $T_A = -40^\circ\text{C}$  to  $100^\circ\text{C}$  and  $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ , all typicals are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ )

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{PHL}$	Propagation Delay Time to Logic Low Output	$C_L = 15\text{pF}$		21	40	ns
$t_{PLH}$	Propagation Delay Time to Logic High Output	$C_L = 15\text{pF}$		23	40	ns
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $					
	FOD0710	$PW = 80\text{ns}$ , $C_L = 15\text{pF}$		2	8	ns
	FOD0720	$PW = 40\text{ns}$ , $C_L = 15\text{pF}$		2	8	ns
	FOD0721	$PW = 40\text{ns}$ , $C_L = 15\text{pF}$		2	6	ns
Data Rate	FOD0710				12.5	Mb/s
	FOD0720, FOD0721				25	Mb/s
$t_{PSK}$	Propagation Delay Skew	$C_L = 15\text{pF}^{(3)}$			20	ns
$t_R$	Output Rise Time (10%–90%)			5		ns
$t_F$	Output Fall Time (90%–10%)			4.5		ns
$ CM_H $	Common Mode Transient Immunity at Output High	$V_I = V_{DD1}$ , $V_O > 0.8 V_{DD2}$ $V_{CM} = 1000\text{V}^{(4)}$	20	40		kV/ $\mu\text{s}$
$ CM_L $	Common Mode Transient Immunity at Output Low	$V_I = 0\text{V}$ , $V_O < 0.8$ , $V_{CM} = 1000\text{V}^{(4)}$	20	40		kV/ $\mu\text{s}$

**Notes:**

- $t_{PSK}$  is equal to the magnitude of the worst case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that will be seen between units at any given temperature within the recommended operating conditions.
- Common mode transient immunity at output high is the maximum tolerable (positive)  $dV_{cm}/dt$  on the leading edge of the common mode impulse signal.  $V_{cm}$ , to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable (negative  $dV_{cm}/dt$  on the trailing edge of the common pulse signal,  $V_{cm}$ , to assure that the output will remain low.

## Typical Performance Curves

Figure 1. Typical Output Voltage vs. Input Voltage

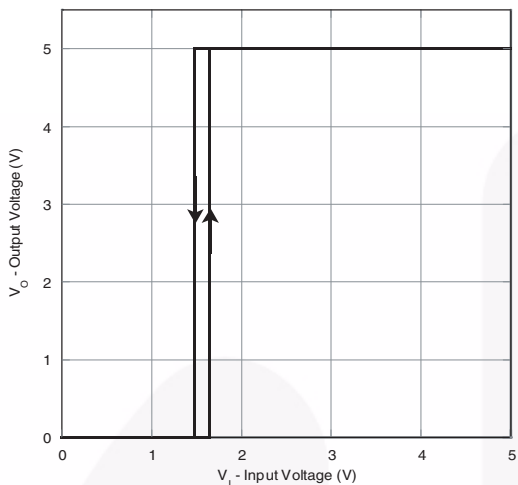


Figure 2. Typical Input Voltage Switching Threshold vs. Input Supply Voltage

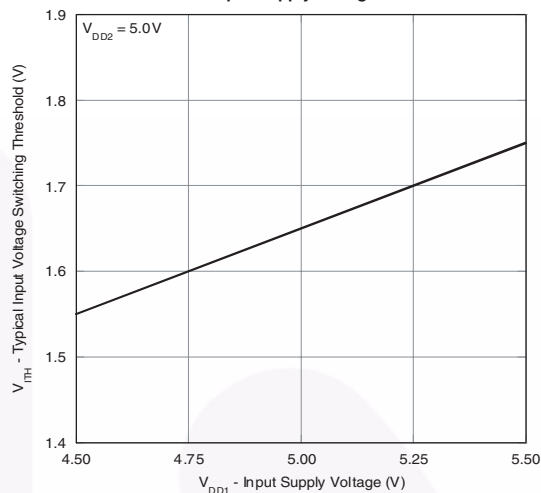


Figure 3. Typical Propagation Delay vs. Ambient Temperature (FOD0710)

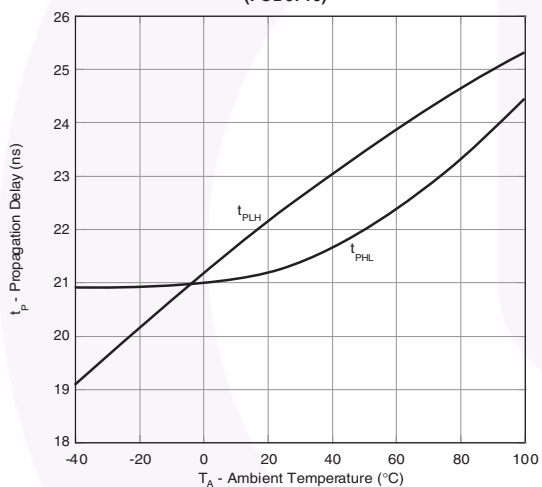


Figure 4. Typical Pulse Width Distortion vs. Ambient Temperature (FOD0710)

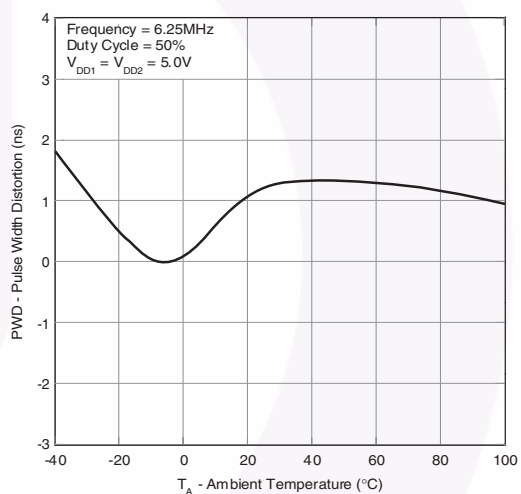


Figure 5. Typical Propagation Delay vs. Ambient Temperature (FOD0721/FOD0720)

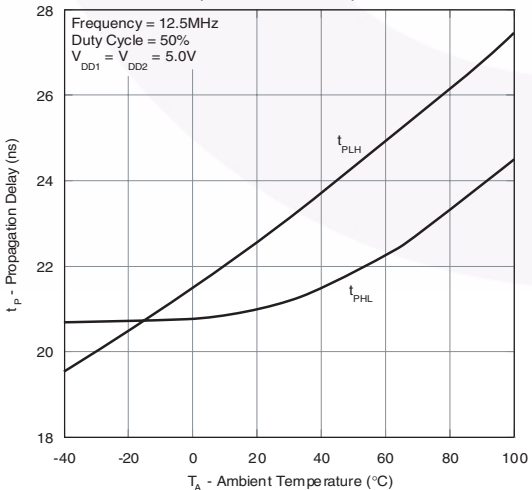
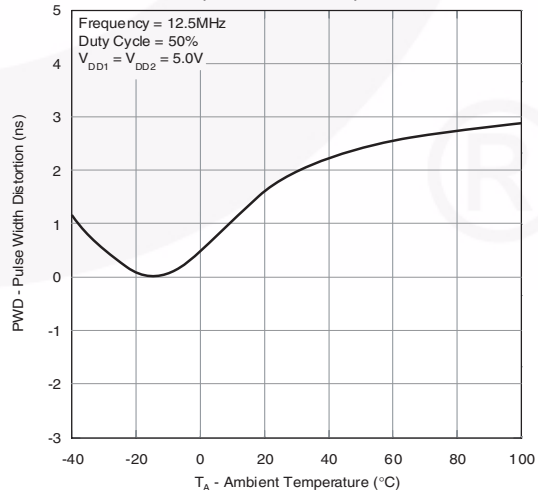
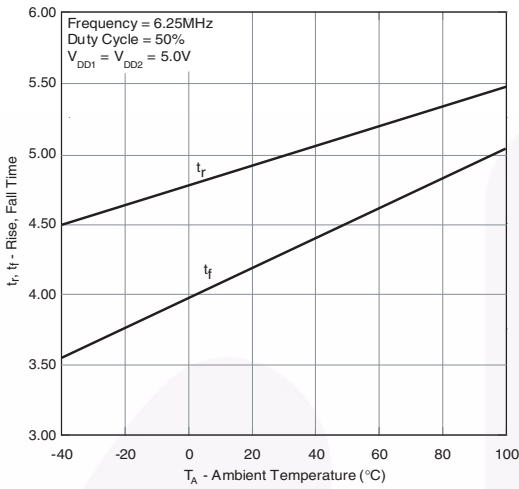


Figure 6. Typical Pulse Width Distortion vs. Ambient Temperature (FOD0721/FOD0720)

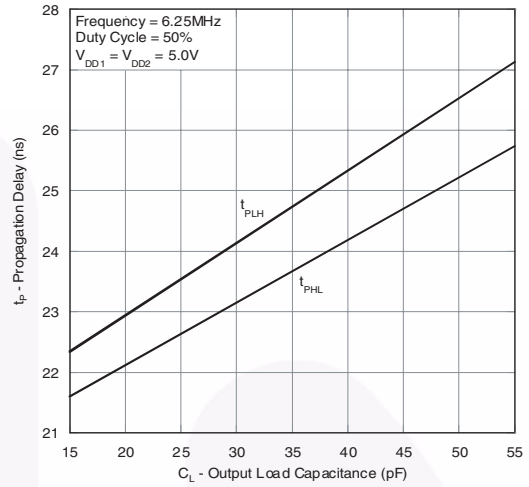


## Typical Performance Curves (Continued)

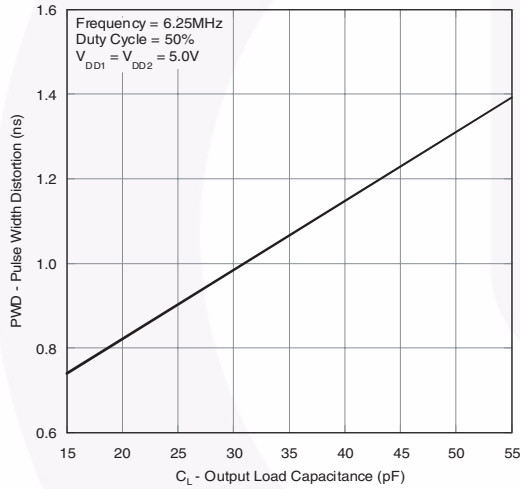
**Figure 7. Typical Rise and Fall Time vs. Ambient Temperature**



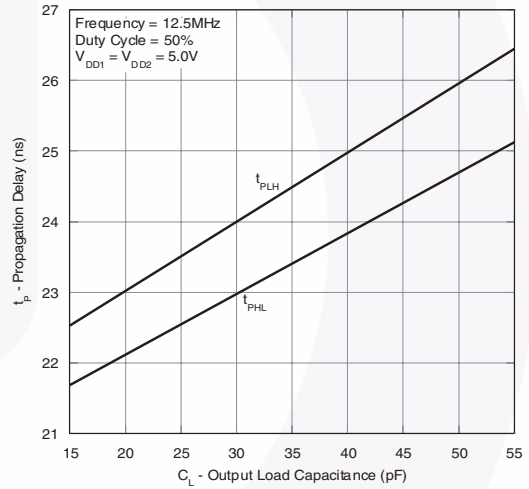
**Figure 8. Typical Propagation Delay vs. Output Load Capacitance (FOD0710)**



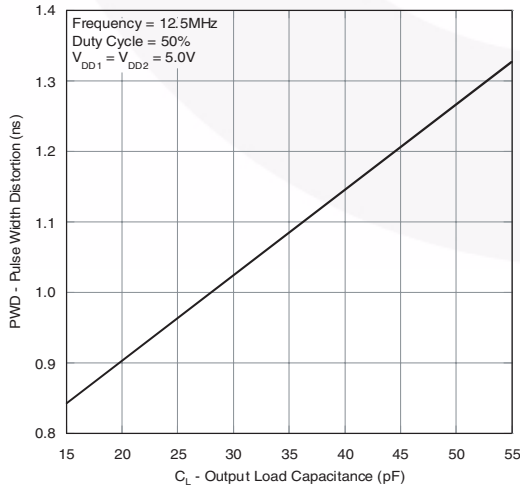
**Figure 9. Typical Pulse Width Distortion vs. Output Load Capacitance (FOD0710)**



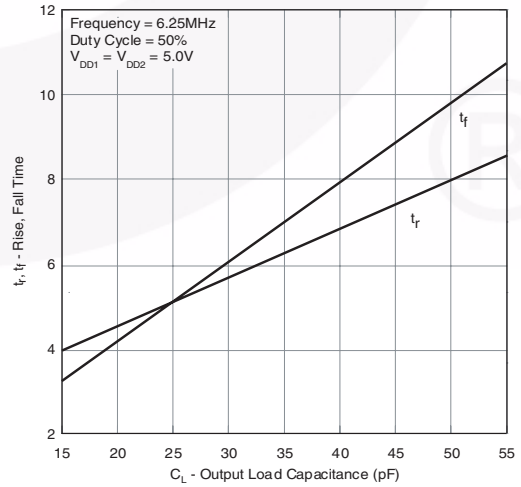
**Figure 10. Typical Propagation Delay vs. Output Load Capacitance (FOD0721/FOD0720)**



**Figure 11. Typical Pulse Width Distortion vs. Output Load Capacitance (FOD0721/FOD0720)**

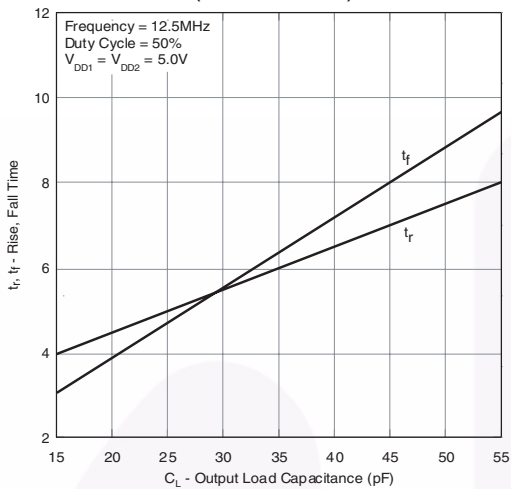


**Figure 12. Typical Rise and Fall Time vs. Output Load Capacitance (FOD0710)**

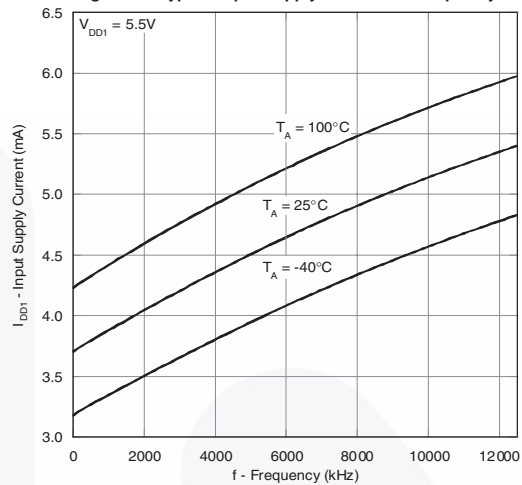


## Typical Performance Curves (Continued)

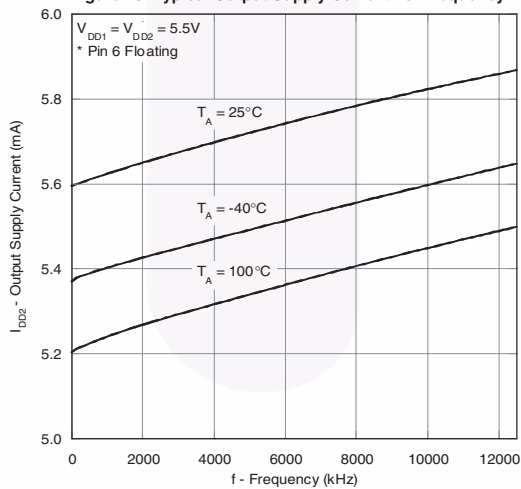
**Figure 13. Typical Rise and Fall Time vs. Output Load Capacitance (FOD0721/FOD0720)**



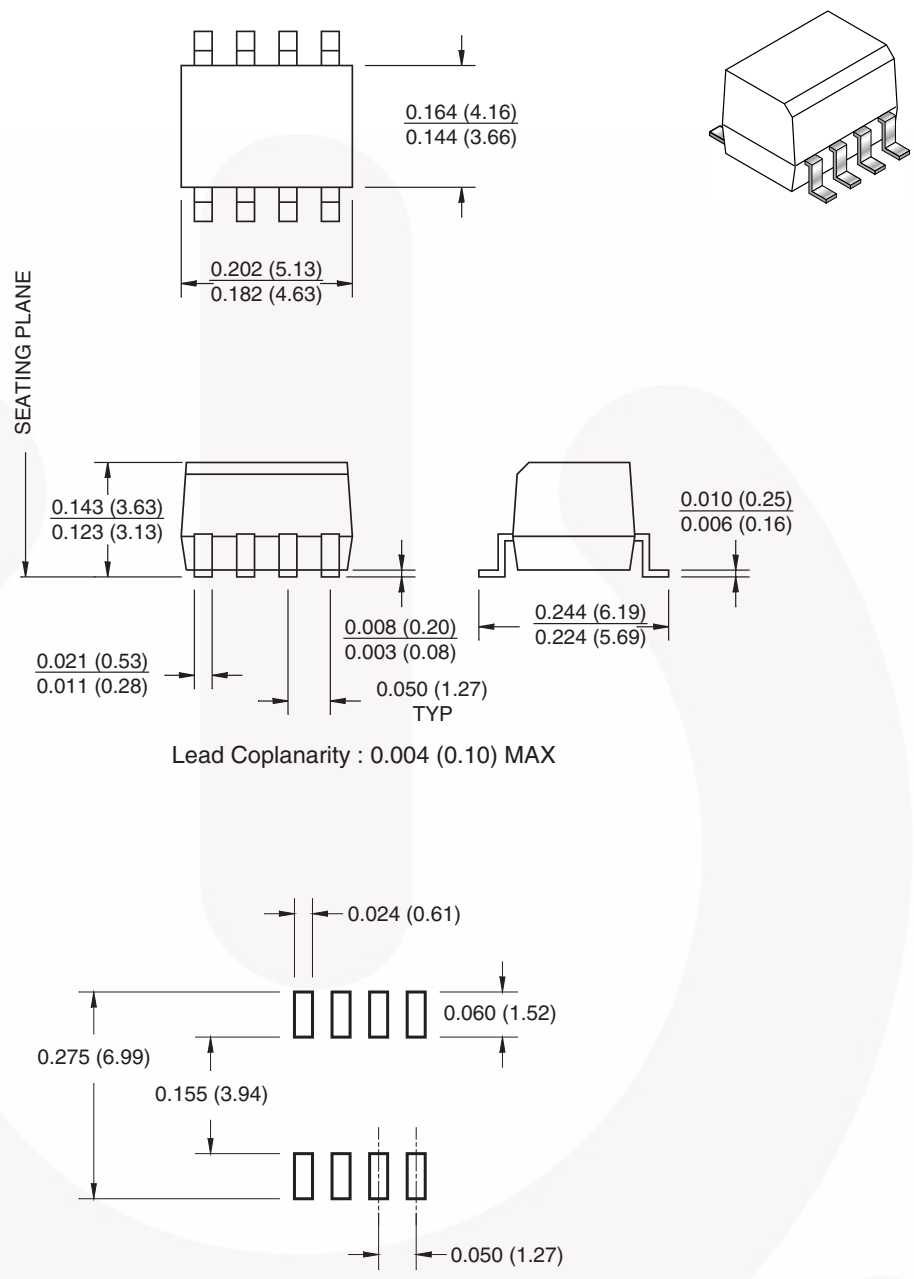
**Figure 14. Typical Input Supply Current vs. Frequency**



**Figure 15. Typical Output Supply Current vs. Frequency**



## Small Outline Package Dimensions



**Note:**

All dimensions are in millimeters.


Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

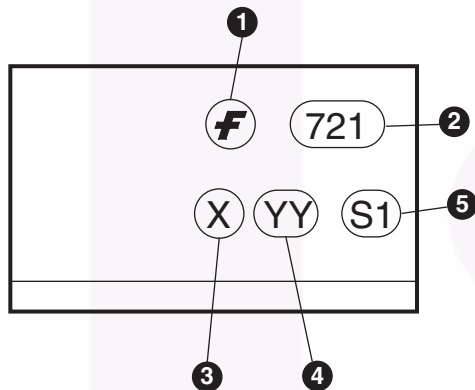
<http://www.fairchildsemi.com/packaging/>

## Ordering Information

Option	Order Entry Identifier	Description
No Suffix	FOD0721	Shipped in Tubes (50 units per tube)
R2	FOD0721R2	Tape and Reel (2500 units per reel)

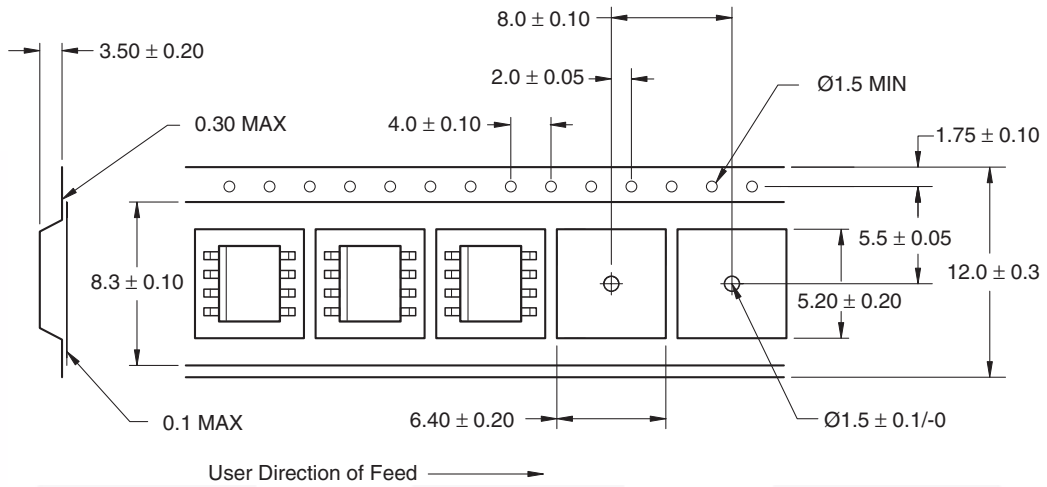
 All packages are lead free per JEDEC: J-STD-020B standard.

## Marking Information



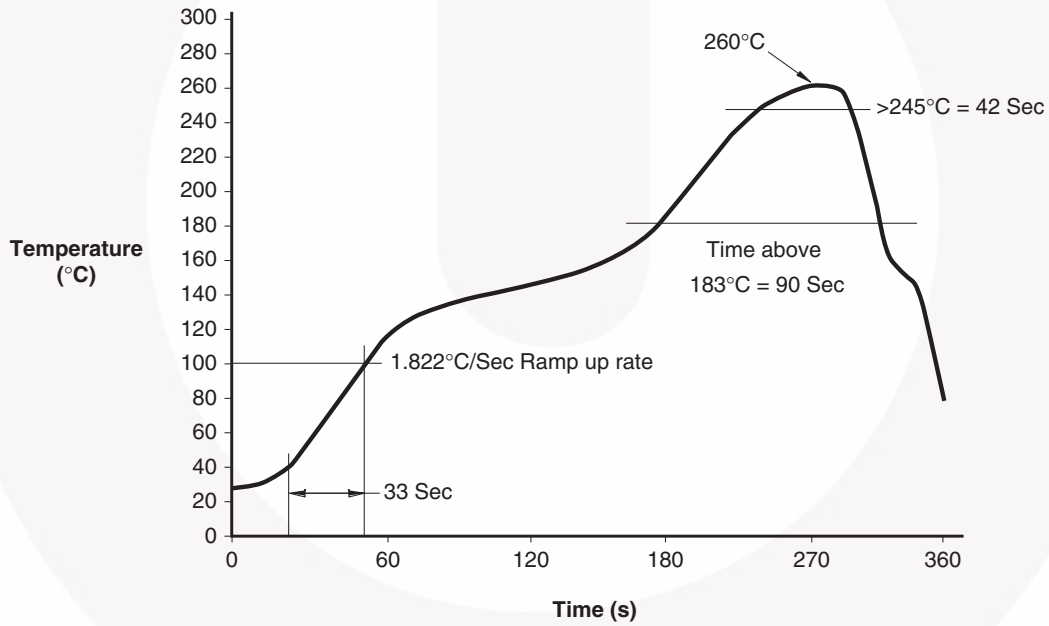
Definitions	
1	Fairchild logo
2	Device number
3	One digit year code, e.g., '8'
4	Two digit work week ranging from '01' to '53'
5	Assembly package code

### Carrier Tape Specification



**Note:**  
All dimensions are in millimeters.

### Reflow Profile



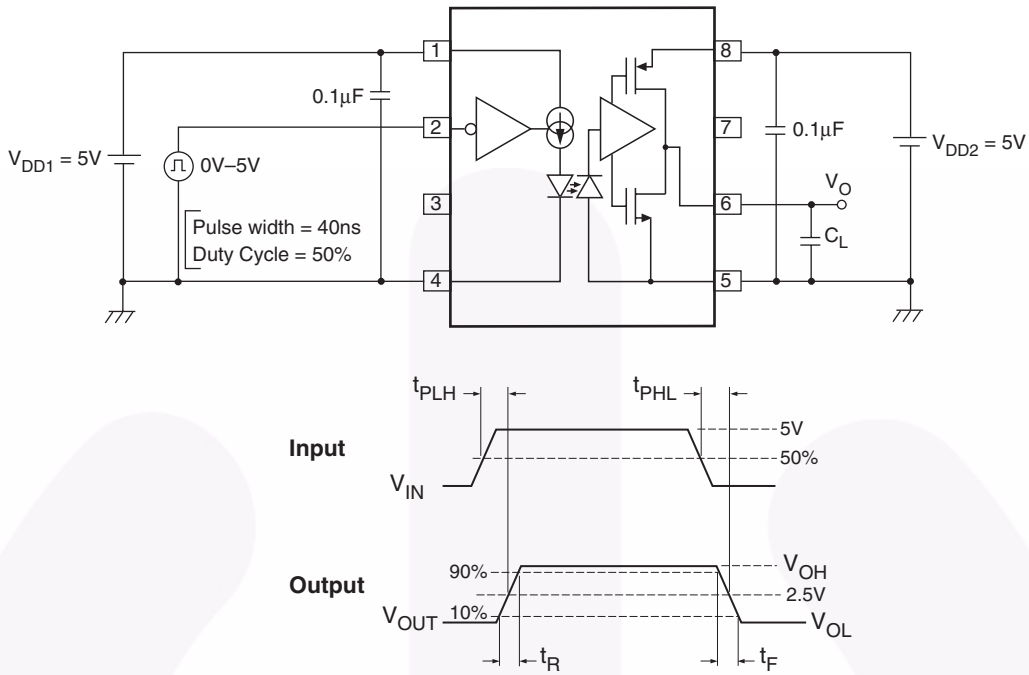


Figure 16. Test Circuit for Propagation Delay Time and Rise Time, Fall Time

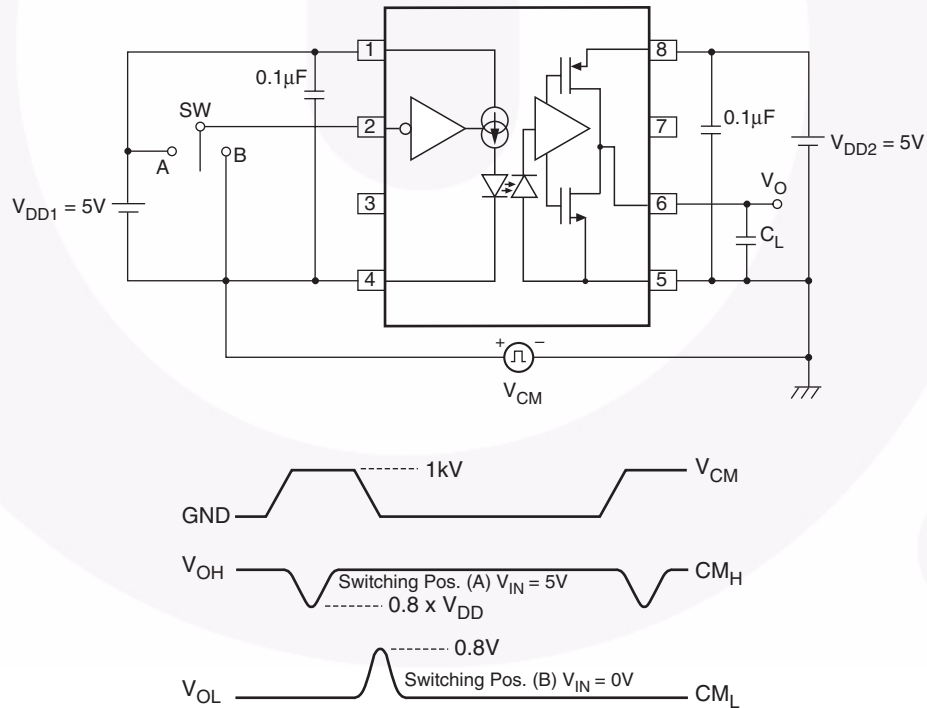








Figure 17. Test Circuit for Instantaneous Common Mode Rejection Voltage



**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |  |   |   |   |
|--|---|---|---|
| Auto-SPM™  | F-PFS™  | PowerTrench®  | The Power Franchise®  |
| Build it Now™  | FRFET®  | PowerXS™  | the power franchise   |
| CorePLUS™  | Global Power Resource™  | Programmable Active Droop™  | TinyBoost™  |
| CorePOWER™   | Green FPS™  | QFET®   | TinyBuck™   |
| CROSSVOLT™   | Green FPS™ e-Series™  | QS™   | TinyLogic®  |
| CTL™   | Gmax™   | Quiet Series™   | TINYOPTO™   |
| Current Transfer Logic™  | GTO™  | RapidConfigure™   | TinyPower™  |
| EcoSPARK®  | IntelliMAX™   |  ™ | TinyPWM™  |
| EfficientMax™  | ISOPLANAR™  | Saving our world, 1mW/W/kW at a time™   | TinyWire™   |
| EZSWITCH™*   | MegaBuck™   | SmartMax™   | TriFault Detect™  |
|  ™* | MICROCOUPLER™   | SMART START™  | TRUECURRENT™*   |
|  ®  | MicroFET™   | SPM®  | µSerDes™  |
| Fairchild®   | MicroPak™   | STEALTH™  |  ™ |
| Fairchild Semiconductor®   | MillerDrive™  | SuperFET™   | UHC®  |
| FACT Quiet Series™   | MotionMax™  | SuperSOT™-3   | Ultra FRFET™  |
| FACT®  | Motion-SPM™   | SuperSOT™-6   | UniFET™   |
| FACT®  | OPTOLOGIC®  | SuperSOT™-8   | VCX™  |
| FAST®  | OPTOPLANAR®   | SupreMOS™   | VisualMax™  |
| FastvCore™   |  ™ | SyncFET™  | XS™   |
| FETBench™  | PDP SPM™  | Sync-Lock™  |   |
| FlashWriter®*  | Power-SPM™  |  ™ |   |
| FPS™   |   |   |   |

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I40