

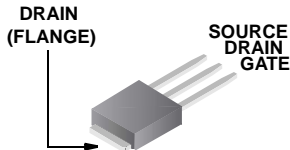
17A, 60V, 0.071 Ohm, N-Channel, Logic Level UltraFET Power MOSFETs



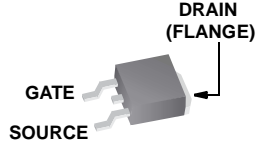
Packaging

JEDEC TO-251AA

JEDEC TO-252AA

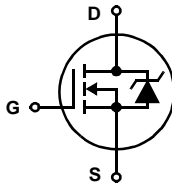


HUFA76409D3



HUFA76409D3ST

Symbol



Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.063\Omega, V_{GS} = 10V$
 - $r_{DS(ON)} = 0.071\Omega, V_{GS} = 5V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Electrical Models
 - Spice and SABER Thermal Impedance Models
 - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs R_{GS} Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUFA76409D3	TO-251AA	76409D
HUFA76409D3ST	TO-252AA	76409D

Absolute Maximum Ratings $T_C = 25^\circ C$, Unless Otherwise Specified

	HUFA76409D3, HUFA76409D3SS	UNITS
Drain to Source Voltage (Note 1)	V_{DSS} 60	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR} 60	V
Gate to Source Voltage	V_{GS} ± 16	V
Drain Current		
Continuous ($T_C = 25^\circ C, V_{GS} = 5V$)	I_D 17	A
Continuous ($T_C = 25^\circ C, V_{GS} = 10V$) (Figure 2)	I_D 18	A
Continuous ($T_C = 135^\circ C, V_{GS} = 5V$)	I_D 8	A
Continuous ($T_C = 135^\circ C, V_{GS} = 4.5V$) (Figure 2)	I_D 8	A
Pulsed Drain Current	I_{DM} Figure 4	
Pulsed Avalanche Rating	UIS Figures 6, 17, 18	
Power Dissipation	P_D 49	W
Derate Above $25^\circ C$	0.327	W/ $^\circ C$
Operating and Storage Temperature	T_J, T_{STG} -55 to 175	$^\circ C$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L 300	$^\circ C$
Package Body for 10s, See Techbrief TB334.	T_{pkg} 260	$^\circ C$

NOTE:

1. $T_J = 25^\circ C$ to $150^\circ C$.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

Reliability data can be found at: <http://www.fairchildsemi.com/products/discrete/reliability/index.html>.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUFA76409D3, HUFA76409D3ST

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ (Figure 12)	60	-	-	V	
		$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, $T_C = -40^\circ\text{C}$ (Figure 12)	55	-	-	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 55\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA	
		$V_{DS} = 50\text{V}$, $V_{GS} = 0\text{V}$, $T_C = 150^\circ\text{C}$	-	-	250	μA	
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 16\text{V}$	-	-	± 100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ (Figure 11)	1	-	3	V	
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 18\text{A}$, $V_{GS} = 10\text{V}$ (Figures 9, 10)	-	0.052	0.063	Ω	
		$I_D = 8\text{A}$, $V_{GS} = 5\text{V}$ (Figure 9)	-	0.060	0.071	Ω	
		$I_D = 8\text{A}$, $V_{GS} = 4.5\text{V}$ (Figure 9)	-	0.064	0.075	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-251AA, TO-252AA	-	-	3.06	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	100	$^\circ\text{C/W}$	
SWITCHING SPECIFICATIONS ($V_{GS} = 4.5\text{V}$)							
Turn-On Time	t_{ON}	$V_{DD} = 30\text{V}$, $I_D = 8\text{A}$ $V_{GS} = 4.5\text{V}$, $R_{GS} = 22\Omega$ (Figures 15, 21, 22)	-	-	153	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	13	-	ns	
Rise Time	t_r		-	89	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	22	-	ns	
Fall Time	t_f		-	37	-	ns	
Turn-Off Time	t_{OFF}		-	-	89	ns	
SWITCHING SPECIFICATIONS ($V_{GS} = 10\text{V}$)							
Turn-On Time	t_{ON}	$V_{DD} = 30\text{V}$, $I_D = 18\text{A}$ $V_{GS} = 10\text{V}$, $R_{GS} = 24\Omega$ (Figures 16, 21, 22)	-	-	59	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	5.3	-	ns	
Rise Time	t_r		-	34	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	41	-	ns	
Fall Time	t_f		-	50	-	ns	
Turn-Off Time	t_{OFF}		-	-	136	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V}$ to 10V	$V_{DD} = 30\text{V}$, $I_D = 8\text{A}$, $I_{g(REF)} = 1.0\text{mA}$ (Figures 14, 19, 20)	-	12	15	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0\text{V}$ to 5V		-	6.8	8.2	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to 1V		-	0.54	0.65	nC
Gate to Source Gate Charge	Q_{gs}			-	1.7	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	3	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 13)	-	485	-	pF	
Output Capacitance	C_{OSS}		-	130	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	28	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 8\text{A}$	-	-	1.25	V
		$I_{SD} = 4\text{A}$	-	-	1.0	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 8\text{A}$, $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	70	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 8\text{A}$, $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	165	nC

Typical Performance Curves

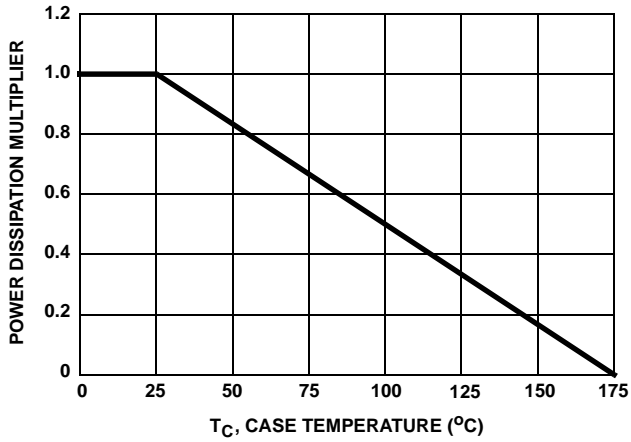


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

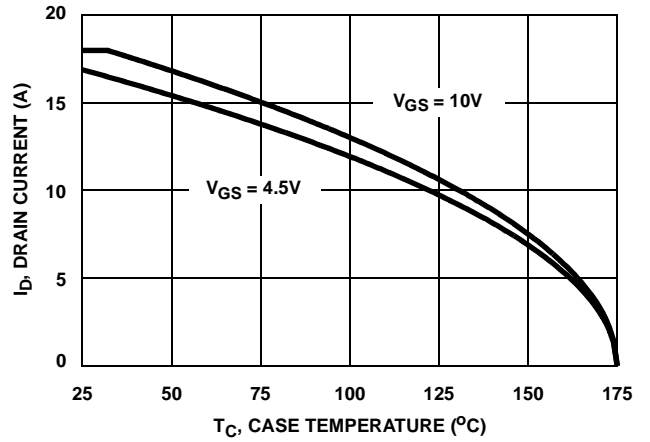


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

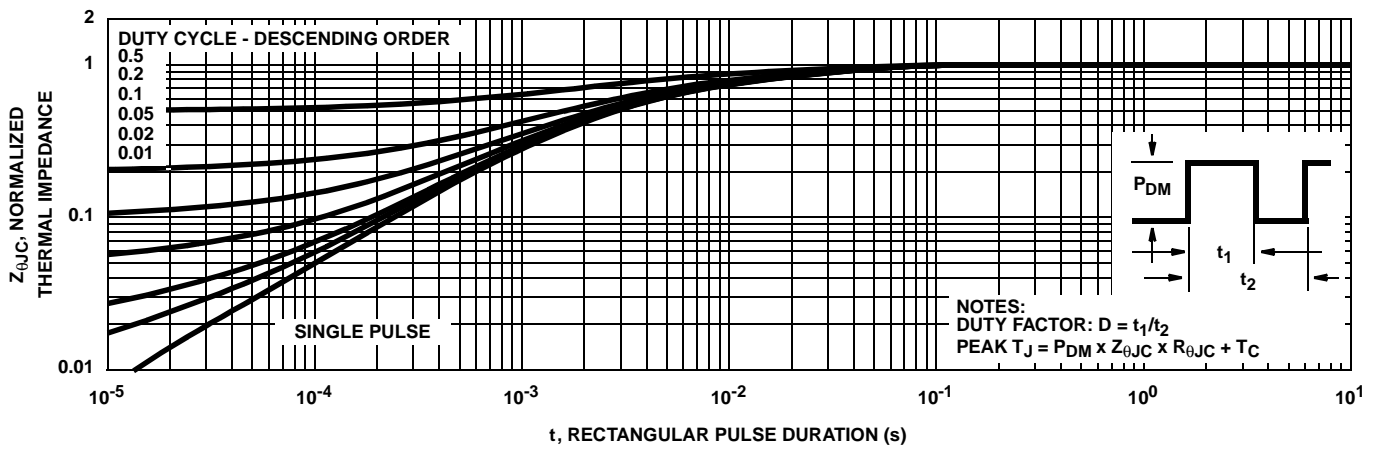


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

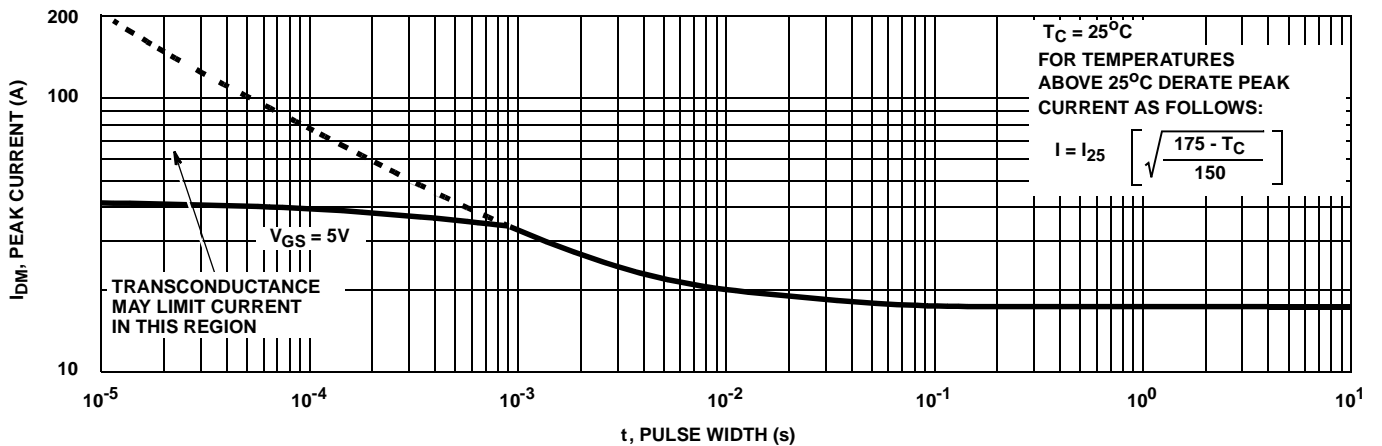


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

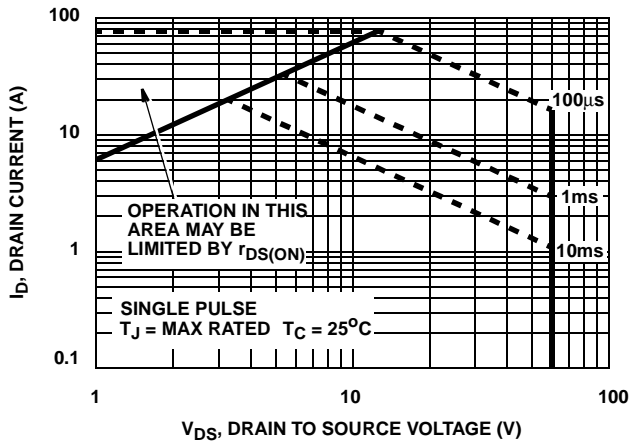
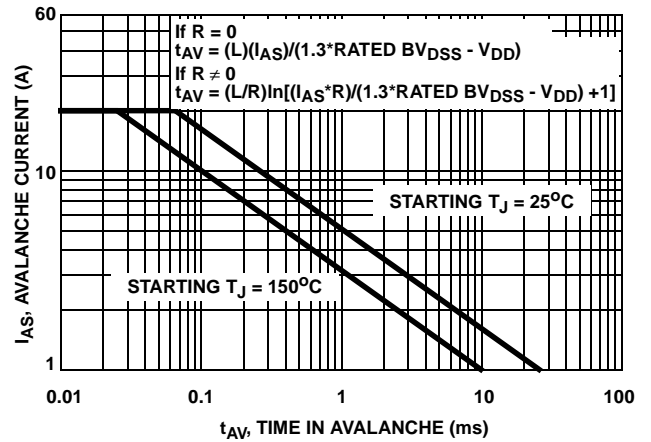


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

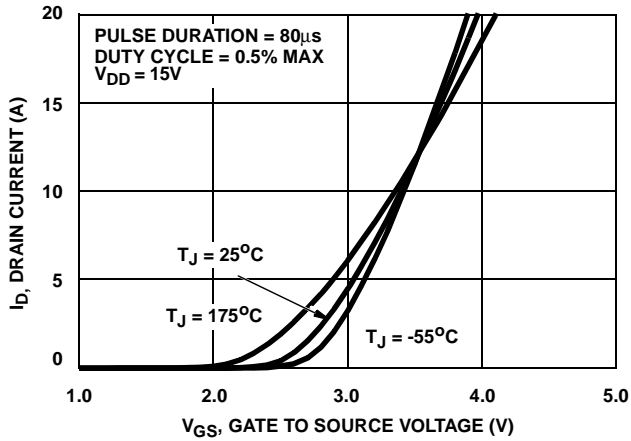


FIGURE 7. TRANSFER CHARACTERISTICS

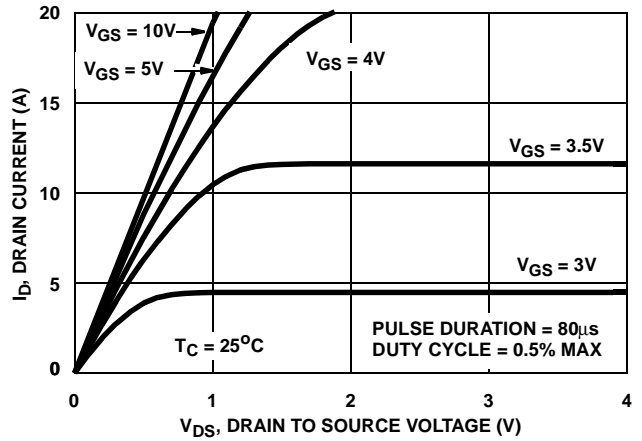


FIGURE 8. SATURATION CHARACTERISTICS

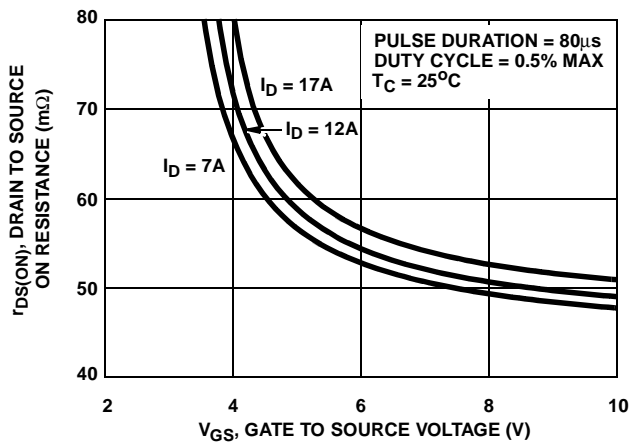


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

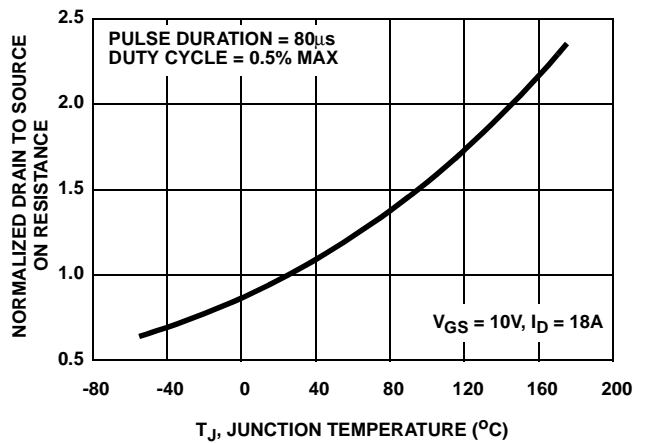


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

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