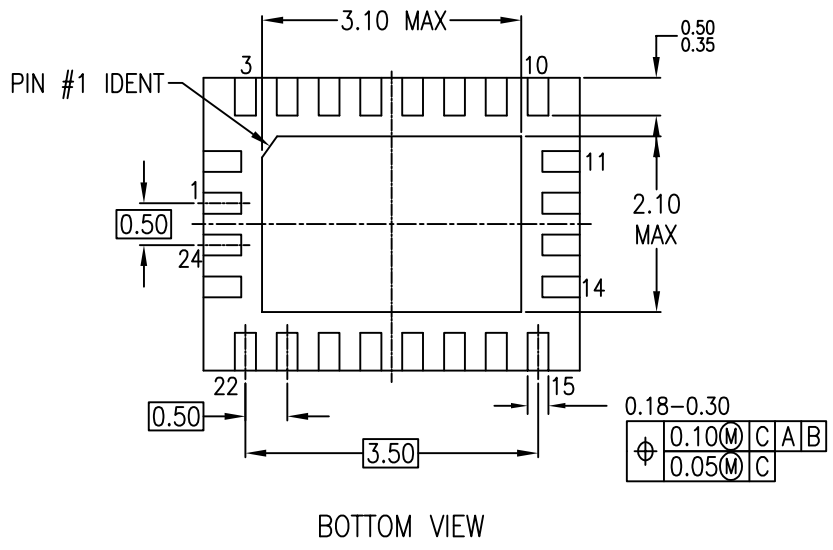
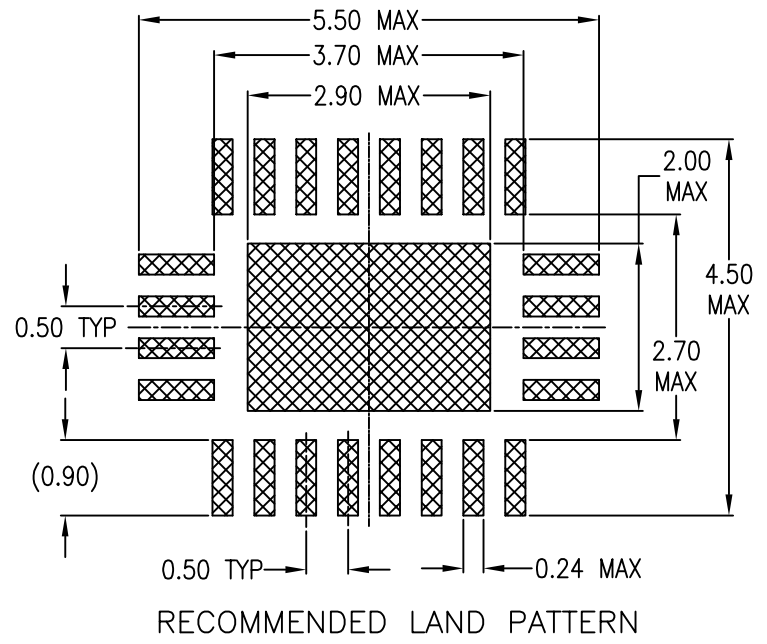
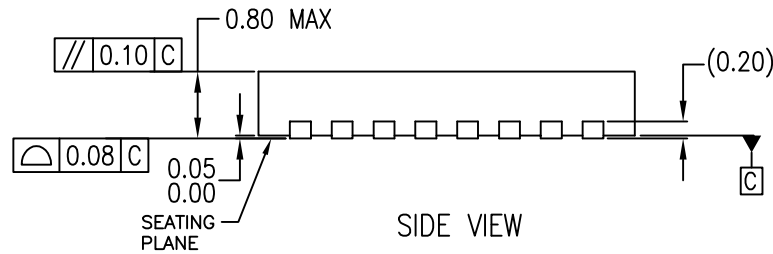
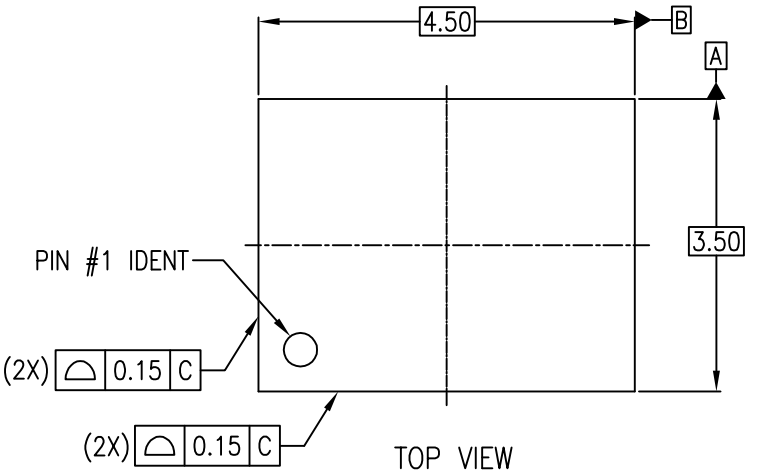


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REVISIONS				
LTR	DESCRIPTION	EDCN	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL		7-4-2003	FEITAN
B	REVISE DWG NAME AND NOTE 1.		12-11-2003	FEITAN
C	CORRECTED PIN NUMBERING AND DAP DIM REMOVED LAND PATTERN NUMBERING. REVISED NOTE 1. TOP VIEW ADDED PIN #1 DOT		17-11-2003	HALLÉN
4	CORRECTED THE LEAD LENGTH FROM 0.35~0.75 TO 0.35~0.50		26 JAN 2007	CHIPKING



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WFS-2 FOR DIMENSIONS ONLY. PIN NUMBERING DOES NOT COMPLY.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP24Brev4

APPROVALS	DATE	FAIRCHILD SEMICONDUCTOR			
DRAWN FEITAN	31-3-2003	Bayan Lepas, FIZ, 11900, Penang, Malaysia.			
DFTG. CHK.		24LD, MLP, QUAD, JEDEC MO-220, 3.5x4.5 MM			
ENGR. CHK.					
PROJECTION		SCALE	SIZE	DRAWING NUMBER	REV
		N/A	N/A	MKT-MLP24B	4
DO NOT SCALE DRAWING				SHEET 1 of 1	