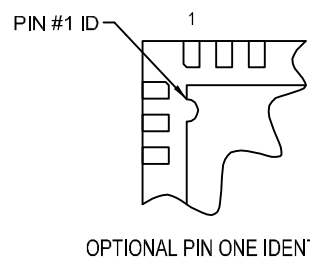
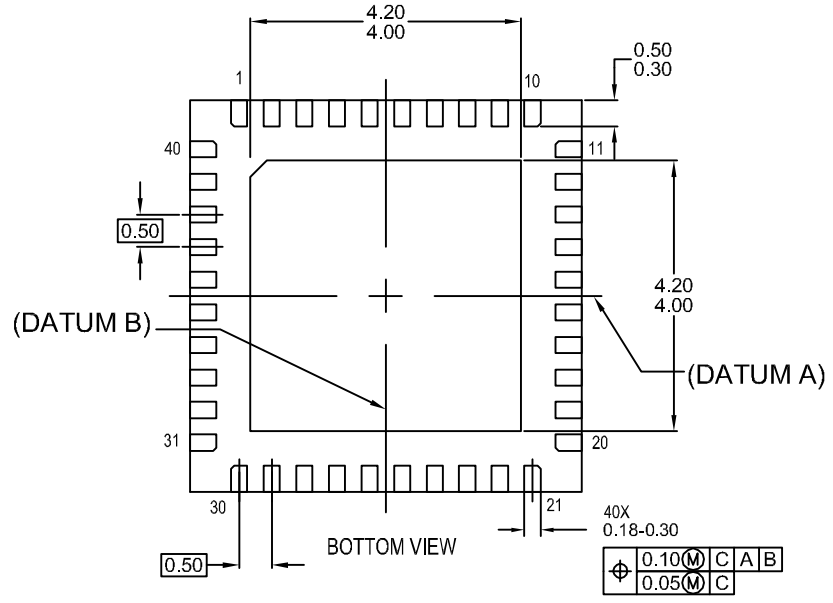
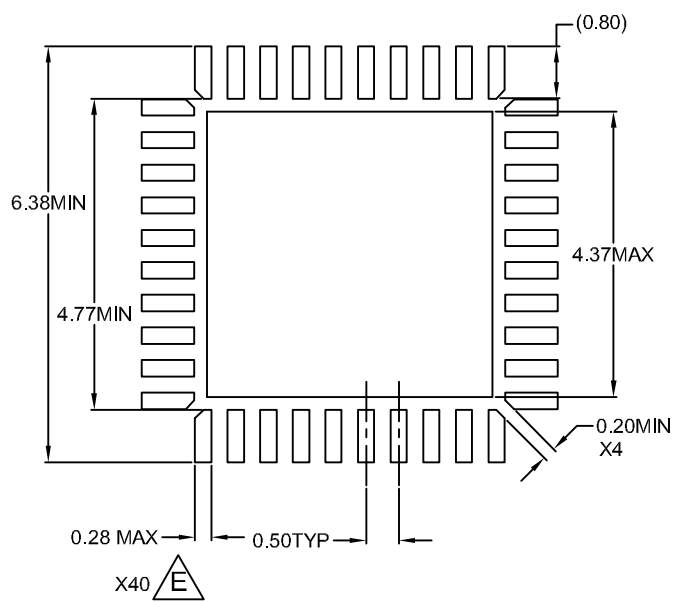
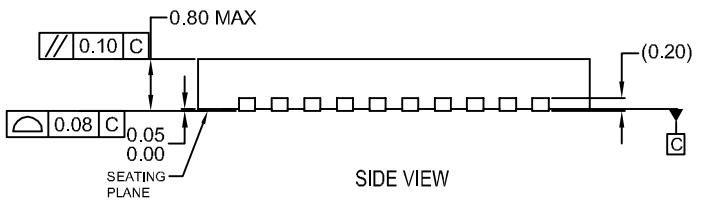
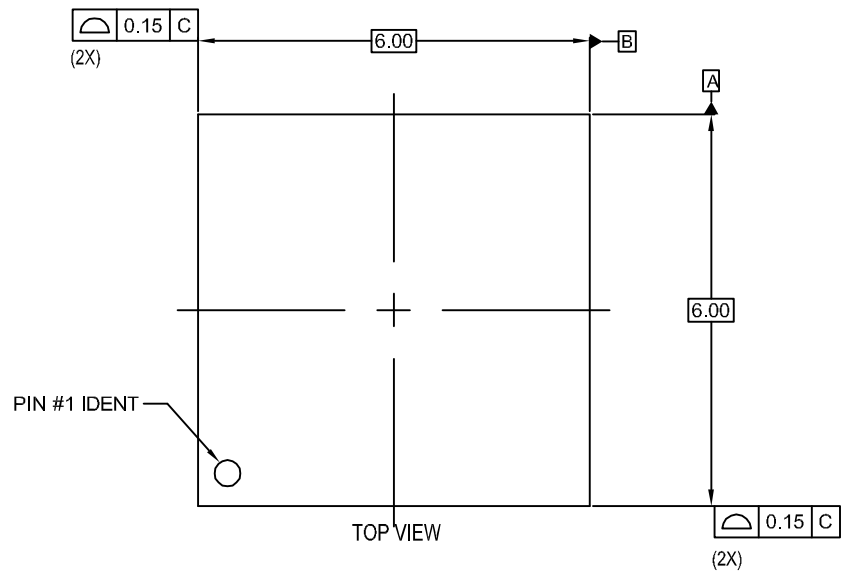


REVISIONS			
REV	DESCRIPTION	DATE	APPO / SITE
A	Released to document control.	11-2004	J. Kingsbury/FSME
B	Added Pin 1 identifier options.	08-2006	H. Allen/FSME
3	Corrected drawing filename, updated notes section, and removed extra positional tolerances on bottom view.	4-23-08	L. England/FSME



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WJJD-2 WITH EXCEPTION THAT THIS IS A SAWN VERSION..
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- D. LAND PATTERN PER IPC SM-782.
- E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.
- F. DIMENSIONS ARE NOT INCLUSIVE OF BURRS, MOLD FLASH, OR TIE BAR PROTRUSIONS.
- G. DRAWING FILENAME: MKT-MLP40Arev3.

APPROVALS		DATE	FAIRCHILD SEMICONDUCTOR		
DRAWN	L. England	4-23-08	40LD MLP, QUAD, JEDEC MO-220 VAR WJJD-2, 6X6MM		
DFTG. CHK.	H. Allen	4-23-08			
ENGR. CHK.					
PROJECTION		SCALE	SIZE	DRAWING NUMBER	REV
		N/A	N/A	MKT-MLP40A	3
DO NOT SCALE DRAWING				SHEET 1 of 1	