

Description and Family Characteristics

ABT Logic for TTL Backplanes

An application's required backplane speed, number of loads (cards), and physical layer are all considerations when selecting the optimal backplane driver IC. Differential and/or reduced swing technologies such as ECL and BTL provide the best noise immunity and are recommended when system performance is at a premium. For most applications, however, TTL-based solutions provide sufficient performance while adding the advantages of lower cost and wider availability. As shown in Figure 1, Fairchild Semiconductor's ABT and LVT BiCMOS technologies are best suited for the most demanding TTL backplane environments, e.g., those with the highest data rates and largest number of loads. ABT and LVT also feature Power-Up 3-STATE capability—a requirement for live insertion.

One difficulty in predicting backplane performance is that most buffer ICs specify propagation delay with a single output switching and a moderate 50 pF load. Conversely, design calculations require the worst case or actual environment which is multiple outputs switching and often a much heavier load. To aid the system designer, most of Fairchild's ABT devices offer extended specifications which include guaranteed AC limits with all outputs switching and driving a 250 pF load.

Fairchild's extended specifications also include guaranteed worst-case noise performance and skew. Noise generation is frequently associated with ground bounce, but also includes V_{CC} droop and dynamic threshold, or shifting of input thresholds due to noise. ABT has the lowest noise generation of any high-speed Logic family. "Skew" refers to the difference in propagation delays between respective paths. Several factors contribute to skew, including the driver IC. Fairchild's ABT logic offers guaranteed skew specifications for three conditions: pin to pin, duty cycle variation, and device to device.

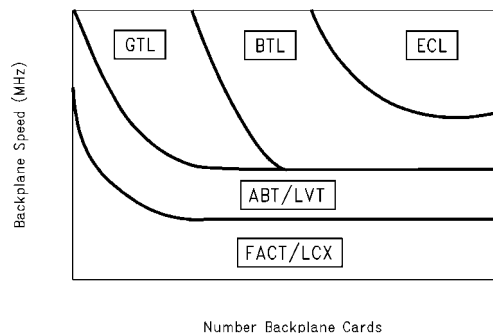
Live insertion is another frequent requirement in any system having high up-time. Input circuitry inherent in Fairchild's ABT and LVT logic devices protects the device

during live insertion while helping to minimize backplane glitch. Please refer to the Applications section of this databook for a detailed discussion of ABT and Live Insertion.

Maximum performance from a backplane is achieved with thorough understanding of the application's environment, including its buffer ICs. Fairchild's extended ABT specifications help provide that knowledge. For details, please refer to the Rating, Specifications and Waveforms section of this databook.

ABT and Computing

Continually higher clock rates combined with tighter noise and EMI constraints have fueled the need for super-fast, yet quiet, Logic. ABT fills this need, coupling the industry's fastest propagation delays with the lowest noise generation of any Advanced Logic family. ABT's BiCMOS process also consumes low power in both static and dynamic conditions. See Sections 2 and 4 of this databook for detailed discussions of power dissipation and ground bounce.



Number Backplane Cards
FIGURE 1. Approximate Backplane Technology Positioning

ABT Circuit and Design Architecture

The basic circuitry for an ABT non-inverting Buffer with 3-STATE control logic is shown in Figure 2. Robust bipolar components form the dual rail ESD protection networks for both input and output structures. The Q6 and D6 ESD circuits provide protection to the V_{CC} rail and have a high enough breakdown voltage rating to remain high impedance ($I_{ZZ} < 100 \mu A$) during powered-down applications. The Schottky transistors Q5, Q7 and Q8 provide protection to the Ground rail and double functionally as highly conductive undershoot clamps.

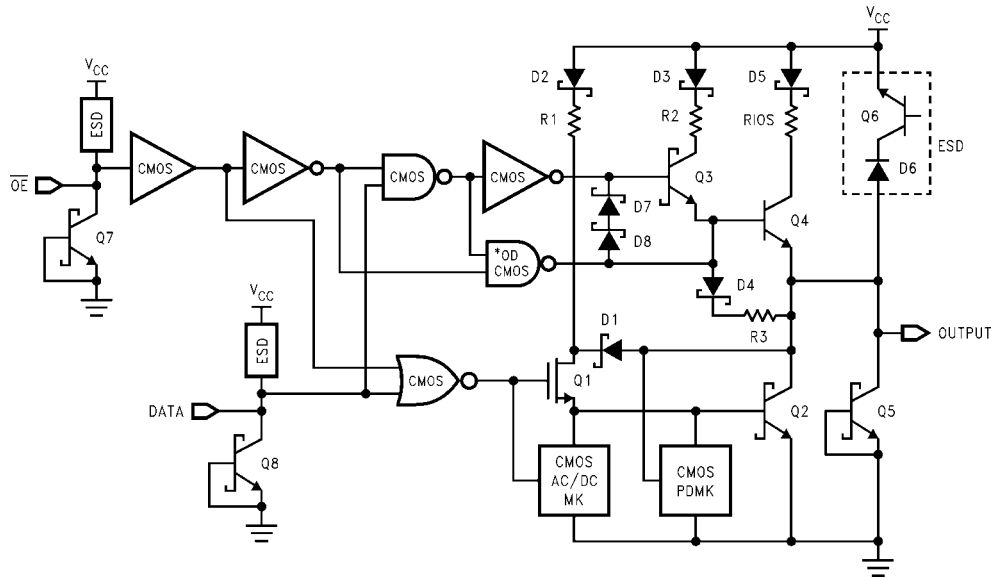
The 3-STATE output structure is formed with Bipolar components to produce high drive ($I_{OL} = 64 \text{ mA}$; $I_{OH} = -32 \text{ mA}$) and high speed TTL compatible logic swings. The pull-up stage utilizes cascaded emitter followers Q3 and Q4 to provide high source current drive for the charging of capacitive loads. The no-load TTL compatible V_{OH} level is one forward-biased V_{BE} (Q3) drop and one forward-biased V_{FD} Schottky diode (D4) drop below the V_{CC} rail yielding typical $3.8V V_{OH}$ at $5V V_{CC}$, $25^\circ C$ and $10 \mu A$ source current. The ON source impedance of this pull-up stage is typically less than 10Ω for source currents between -5 mA to -40 mA at $25^\circ C$. This initial low impedance turn-on characteristic allows the pull-up stage to easily provide a V_{OH} level of $2V$ minimum at I_{OH} source current of -32 mA over the operating V_{CC} and temperature ranges. See Figure 6. At $25^\circ C$ and source currents above -50 mA , the pull-up stage becomes limited by voltage drop across the R_{IOS} resistor and the effective source impedance becomes 25Ω typically. Schottky diodes D3, D4 and D5 also provide blocking

to insure that the pull-up stage remains high impedance during power down applications.

When the output is enabled by a logic low on the \overline{OE} input and a logic high is on the Data input, the base of Q3 is driven to the V_{CC} rail by the CMOS inverter in the data path. The open drain CMOS NAND gate is logic high-open (non-conducting) and allows the base of Q4 to be driven ON by Q3. The CMOS NOR gate goes low turning Q1 OFF and turning ON the CMOS AC/DC Miller Killer circuitry which grounds the base of Q2, quickly turning it OFF. This circuitry provides an active shunt for any charge coupled by the Miller Effect of the Q2 collector-base capacitance during the low to high output transition. Use of this active circuitry improves output rise time and serves to reduce simultaneous conduction of pull-up and pull-down stages during LH transitions. The AC/DC Miller Killer circuit is also active when the output goes to 3-STATE to prevent Q2 base injection by the LH transitions of other outputs on a bus, therefore dynamic bus loading will be capacitive only.

Power Down Miller Killer circuitry at the base of Q2 is inactive when V_{CC} is applied. When V_{CC} is powered down, the Power Down Miller Killer circuitry provides an active shunt to transient energy coupled to the Q2 base by its collector base capacitance. This prevents momentary turn-on of Q2 during LH transitions in partial power down bus applications and maintains the powered off output as only a Hi-Z light capacitive load ($I_{ZZ} < 100 \mu A$) to the bus.

Note that Q1 drives only the Q2 pull-down stage and does not function as the Phase Splitter driver typical of TTL logic. The pull-up stage is controlled by CMOS logic independent of Q1. This feature allows the input threshold voltages for the CMOS logic driving the pull-up stage to be set independent of the logic driving the pull-down stage.

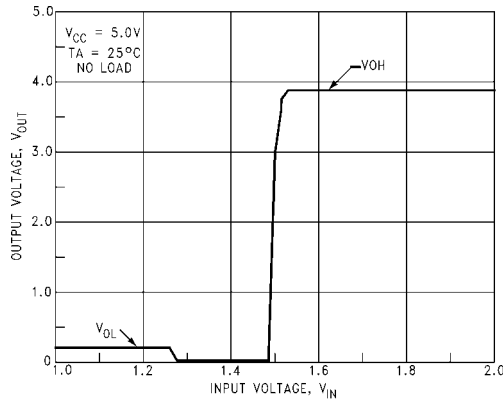


*Open Drain

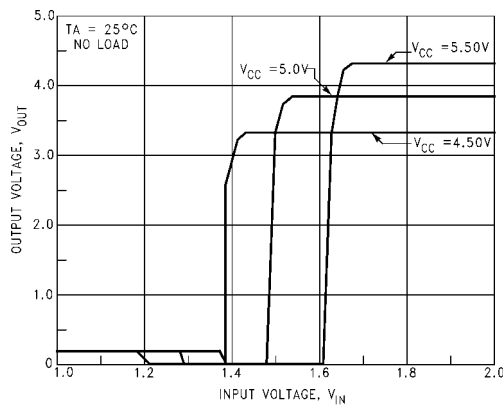
FIGURE 2. Basic ABTC 3-STATE Buffer Schematic

ABT Circuit and Design Architecture (continued)

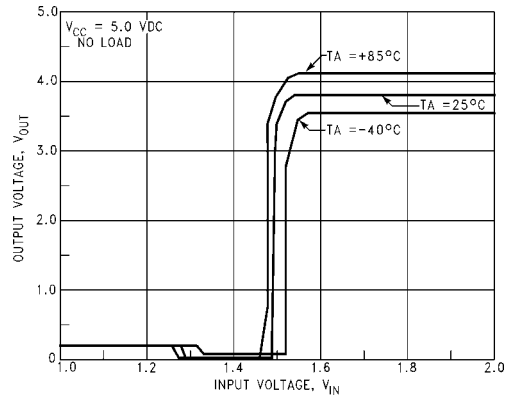
The transfer function for the non-inverting ABT Buffer shown in Figure 3 indicates that the data input switching threshold for the pull-down stage is approximately 200 mV lower than the pull-up stage. As the Data input is swept from logic LOW to logic HIGH, the output switches from active LOW to high impedance at an input threshold of about 1.3V at 25°C and a V_{CC} of 5.0V. When the input reaches about 1.5V, the output switches from high impedance to HIGH. This design feature serves to reduce simultaneous conduction of the stages during switching. Also, the 200 mV offset in Data input switching thresholds acts like hysteresis and causes the buffer to be very tolerant of slow data input edge rates, i.e., edge rates slower than 10 ns/V can easily be tolerated without output oscillation. The switching threshold is proportional to V_{CC} as indicated in Figure 4 and is quite stable as a function of temperature as indicated by Figure 5.



**FIGURE 3. Buffer Transfer Function
@ Room Temperature
 $V_{CC} = 5V$, $T_A = 25^\circ C$, No Load**

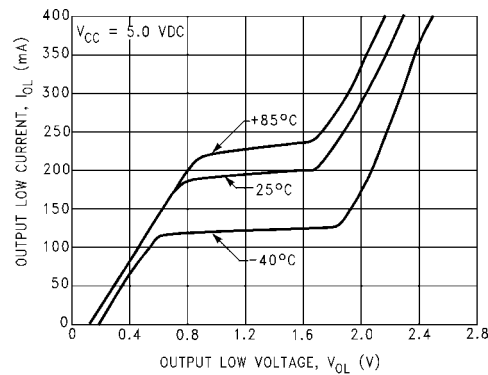


**FIGURE 4. Transfer Function vs. V_{CC}
 $T_A = 25^\circ C$, No Load**



**FIGURE 5. Transfer Function vs. Temperature
 $V_{CC} = 5V$ DC, No Load**

With the output enabled by a LOW on the \overline{OE} input, a LOW on the Data input forces active LOWS on both the CMOS inverter and the open drain CMOS NAND gate outputs, which then simultaneously turn OFF Q3 and Q4. The CMOS NOR gate output goes HIGH, turning the AC/DC Miller Killer circuitry OFF and Q1 ON to drive Q2 ON. Q2 is designed to easily sink 64 mA I_{OL} , at $V_{OL} < 0.55V$. During HL output transitions, Schottky diode D1 assists the pull-down stage in providing a low impedance discharge path for the output load capacitance. As the stage turns on, part of the charge on the output load passes through D1 and Q1 to momentarily increase the base drive to Q2 and increase Q2's current sink capability. See output characteristics in Figure 6, I_{OL} vs. V_{OL} .



**FIGURE 6. Output Low Characteristics
 $V_{CC} = 5V$ DC**

ABT Circuit and Design Architecture (continued)

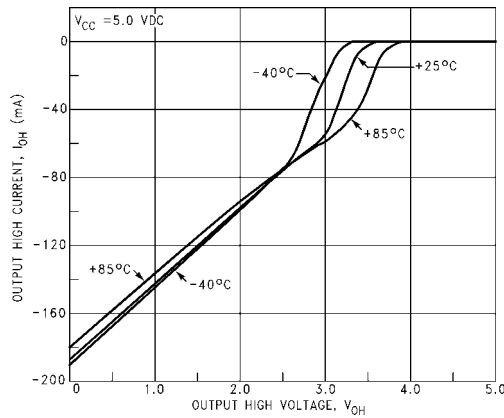


FIGURE 7. Output High Characteristics
 $V_{CC} = 5V$ DC

When the output is disabled by a HIGH on the \overline{OE} input, the enable CMOS logic quickly overrides the Data path logic and cuts off drive to whichever stage is ON. In the case of an LZ transition, the CMOS NOR gate is driven LOW turning OFF Q1 and turning ON the AC/DC Miller Killer circuitry to insure Q2 is quickly turned off. In the case of a HZ transition, the CMOS inverter goes hard LOW to turn off Q3 and quickly discharge the base of Q4 through Schottky diodes D7 and D8. The effect of disable time (t_{PLZ} , t_{PHZ}) being typically faster than enable time (t_{PZL} , t_{PZH}) inherently helps avoid bus contention.

Since the CMOS Enable logic remains active to V_{CC} 's well below 2V, high impedance control can be maintained to V_{CC} voltages below the turn-on V_{CC} thresholds of the Bipolar output stage. This insures the capability for glitch free power ON/OFF high impedance outputs with the provision that the \overline{OE} input is maintained logic HIGH at or greater than the data sheet specified 2.0V minimum V_{IH} during the V_{CC} power ramp. However, since the CMOS logic switching threshold varies proportional to V_{CC} , a practical worst case \overline{OE} logic high of 2.0V or 50% of V_{CC} , will maintain the power ON/OFF 3-STATE condition during the V_{CC} transition.

ABT is designed to be tolerant of controlled live insertion at the PCB level. Controlled means that the insertion or

removal methodology is accomplished in such a way that power to the PCB is applied in a preferred sequence and that control signals are provided to the PCB also in the preferred sequence such that output control is asserted to prevent contention of outputs attached to a bus during the power up or down sequence.

Tolerant means that ABT is designed and guaranteed to behave in a predictable manner during controlled PCB live insertion in systems requiring fault-tolerant or noninterruptible applications. Additionally, ABT has features which facilitate design of systems which must utilize power partitioning for redundant circuitry or for powering saving of inactive circuits.

All ABT input, output, and I/O pins are protected with robust Bipolar components with respect to both V_{CC} and Ground rails. This circuitry is designed to withstand 2000V (Human Body Model) and also to provide clamping action for voltage undershoot while preserving low capacitive loading of the pin. The clamping action by the undershoot clamp begins aggressively at voltages more negative than $-0.5V$ relative to Ground, but this clamp remains non-conductive at voltages up to 7V. Relative to the V_{CC} rail, the ESD circuitry begins clamping only at voltages greater than 5.5V above V_{CC} . These ESD circuits remain high impedance and non-conductive for applied input or output voltages between $-0.4V$ to 5.5V with $V_{CC} = 0V$ to 5.5V.

ABT CMOS input stages are Hi-Z with or without V_{CC} applied. The I_{IL} , I_{IH} , and I_{BVI} data sheet specification guarantees high DC impedance for inputs with V_{CC} applied. The V_{ID} specification guarantees Hi-Z inputs with $V_{CC} = 0V$.

High impedance output and I/O pins are capable of maintaining Hi-Z status with $V_{CC} = 0$ and during the application or removal of V_{CC} . The ABT data sheet parameters I_{OZH} and I_{OZL} guarantee $< 50 \mu A$ output leakage for applied V_{OUT} voltages of 2.7V or 0.5V at any V_{CC} between 5.5V and 0V with the output disabled and with the appropriate logic input voltage maintained on the \overline{OE} input pin. An additional I_{ZZ} bus drainage specification guarantees $< 100 \mu A$ output leakage at $V_{OUT} = 5.5V$ with $V_{CC} = 0V$. Therefore, ABT outputs are guaranteed to remain glitch-free during the power cycle and at power down $V_{CC} = 0V$. Refer to Application Section for a more detailed discussion of live insertion and powerup/down 3-STATE capabilities of ABT.

Threshold and Noise Margin

Figure 8 describes the input signal voltage levels for use with ABT products. The AC testing input levels follow industry convention which require 0.0V for a logic LOW and 3.0V level for a logic HIGH. DC input levels are typically 0.0V to V_{IL} , and high input levels are typically V_{IH} to V_{CC} . DC testing uses a combination of threshold and hard levels to assure datasheet guarantees. Input threshold levels are usually guaranteed through V_{OL} and V_{OH} tests

High level noise immunity is the difference between V_{OH} and V_{IH} and low level noise immunity is the difference between V_{IL} and V_{OL} . Noise-free V_{IH} or V_{IL} levels should not induce a switch on the appropriate output of an ABT device. When testing in an automated environment, extreme caution should be taken to ensure that input levels plus noise do not go into the transition region.

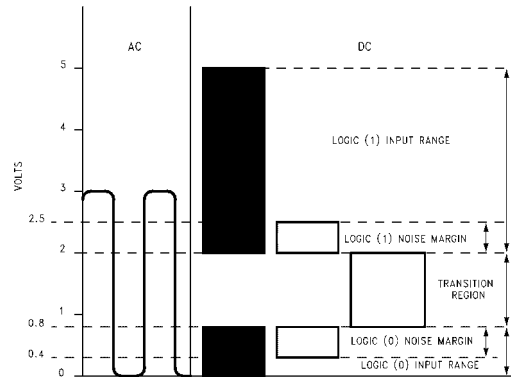


FIGURE 8.

Power Dissipation in BiCMOS Devices

With regards to power dissipation, BiCMOS technology combines the most desirable characteristics from both Bipolar and CMOS. In the quiescent state, BiCMOS power dissipation is reduced relative to Bipolar; the only static power dissipated is due to the small leakage currents I_{CCH} and I_{CCL} . ABT's Dynamic power consumption is reduced relative to CMOS because of ABT's lower output voltage level swings.

In determining a device's contribution to overall system power dissipation, we must consider components of power generated internally to the device as well as that on the external load(s).

Total power dissipation can be described by the equation:

$$P_{Dtotal} = P_{Dquiescent} + P_{Dynamic} \quad (1)$$

$$= P_{Dq} + (P_{Dint} + P_{Dload}) \quad (1a)$$

Where:

P_{Dtotal} = Total Power dissipated into the system due to device operation
 P_{Dq} = Quiescent component of total power dissipated by the device
 P_{Dint} = Power dissipation internal to the device under dynamic conditions
 P_{Dload} = Power dissipated by the device in switching the load

Each component of total power dissipation is determined as follows:

Quiescent power dissipation takes into account the device outputs that are conditioned to TTL high and low levels, as well as those inputs that are being driven with a voltage between Ground and V_{CC} .

$$P_{Dq} = \frac{[(I_{CCL}/N) * N_{OL} * V_{CC}] + [(I_{CCH}/N) * N_{OH} * V_{CC}]}{[I_{CCT} * N_{TTL} * V_{CC}]} \quad (2)$$

As shown by equation 1a, the dynamic power dissipation is a combination of two components. The first, P_{Dint} , is a result of charging and discharging internal parasitic capacitances. The second, P_{Dload} , is a result of charging and discharging the output (system) load on the device.

$$P_{Dint} = [(I_{CCD} * f1 * NS) * V_{CC} * DC] \quad (3)$$

$$P_{Dload} = [C_L * VS * f2 * V_{CC} * NS * DC] \quad (4)$$

Terms used in power dissipation equations:

I_{CCL}	Quiescent power supply current with all outputs in the low state
I_{CCH}	Quiescent power supply current with all outputs in the high state
N	Total number of device outputs
N_{OL}	Number of outputs in the low state
N_{OH}	Number of outputs in the high state
I_{CCT}	Quiescent power supply current resulting from an input conditioned to a TTL level other than ground and V_{CC}
N_{TTL}	Number of inputs conditioned to TTL level other than ground and V_{CC}
I_{CCD}	Power consumption coefficient for one bit toggling; expressed in mA/MHz
f1	Frequency of output switching; expressed in MHz
f2	Frequency of output switching, expressed in Hertz
NS	Total number of outputs switching
VS	Output voltage swing ($V_{OH} - V_{OL}$)
DC	Duty cycle of outputs switching
V_{CC}	Power supply voltage

ABT Process Characteristics

PROCESS CHARACTERISTICS

Fairchild's 1.0 BCT combines bipolar and CMOS transistors in a single process to achieve high speed, high drive characteristics while maintaining low 3-STATE power and the ability to control noise.

Fairchild's 1.0 BCT provides a suitable platform for migration to higher performance levels with minor technology enhancements planned for the near future. In its present form, the technology supports Interface, Digital, Bus and Telecom products from National Semiconductor.

PROCESS FEATURES

- 18 masking layers using stepper lithography
- 100% ion implantation utilized for dopant placement
- Localized retrograde wells tailored for high performance
- Optimized recessed and field isolation sequence for CMOS/bipolar
- NMOS LDD (Lightly Doped Drain), PMOS Halo architecture
- 150Å gate oxide
- Self aligned bipolar contact set utilizing minimum geometries
- Localized retrograde sub-emitter collector
- Advanced planarization on all topographies
- PtSi Schottky diodes, all contacts use platinum for resistance reduction
- Barrier metal of TiW
- Dual layer metal of Al-Cu 0.3% for long term reliability
- Metal pitch of 3.5 microns

PROCESS FLOW

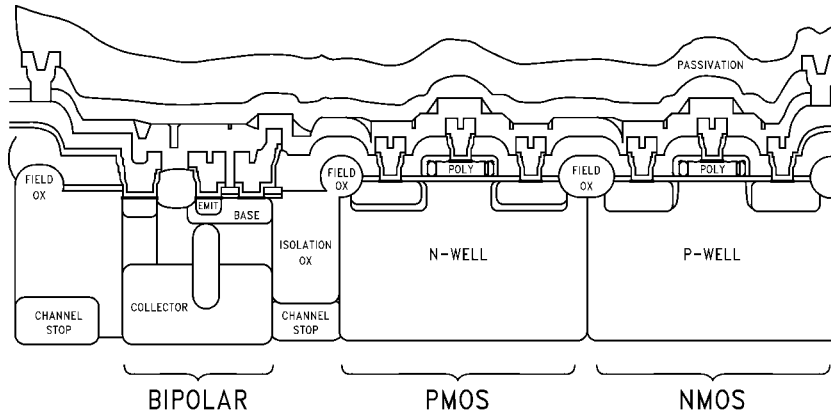
- 1.0 Buried Layer
- 2.0 P-Well
- 3.0 N-Well
- 4.0 Isolation
- 5.0 Sink
- 6.0 Active
- 7.0 Active Strip
- 8.0 Poly
- 9.0 Base
- 10.0 Bipolar Contact
- 11.0 Emitter
- 12.0 P+ Source/Drain
- 13.0 N+ Source/Drain
- 14.0 Contact
- 15.0 Metal 1
- 16.0 Via
- 17.0 Metal 2
- 18.0 Passivation

PROCESS PARAMETERS

- Bipolar Performance: 10 GHz Ft with gains greater than 100
- CMOS Performance: 0.5 μm min Leff
- Platinum Schottky diodes for TTL
- Typical ESD Performance: >2000V, Human Body Method
- Robust latch-up and punch-through protection with retrograde wells
- Advanced interconnect supports superior temperature cycle performance

PROCESS CROSS-SECTION

1.0 BCT Cross Section



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com