

## ABT Applications

### Avoiding Bus Contention

ABT devices typically disable (to high impedance) faster than they enable (to active state) and therefore offer an inherent way to minimize bus contention. System designers must be aware of the effects of bus interface device exposure to contention. Some advice is offered in the following discussion.

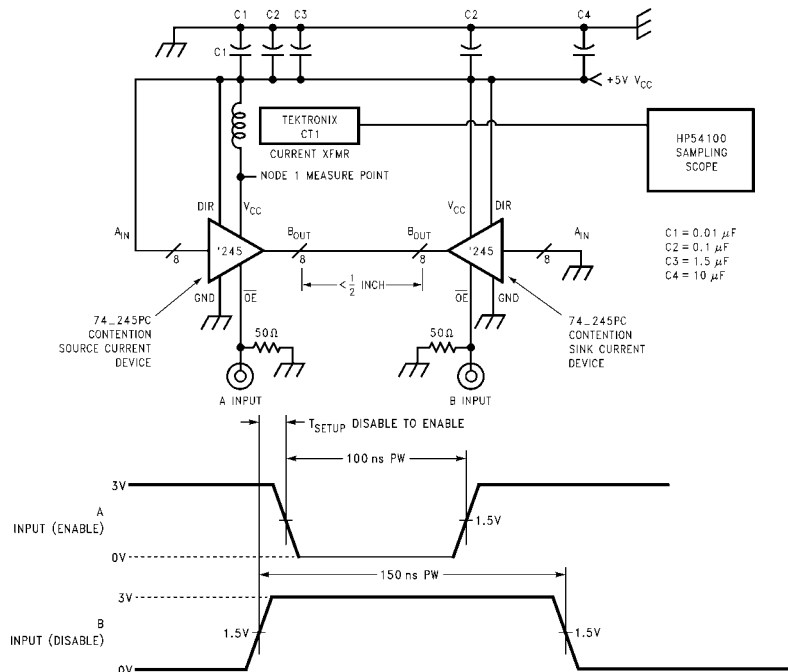
Ideally the system designer should insure that the disabling signal to the active driver always precedes the enabling signal to the next driver to insure minimum contention; i.e.,  $t_{SETUP}$  time disable-to-enable should be a positive number. If the interface devices on the bus (as FSC ABT devices typically do by design) exhibit disable times ( $t_{PHZ}/t_{PLZ}$ ) quicker than enable times ( $t_{PZH}/t_{PZL}$ ), then the  $t_{SETUP}$  time disable-to-enable can be reduced to zero or slightly negative and not cause significant contention.

The typical  $t_{SETUP}$  time is approximated from the typical enable/disable time specs:  $t_{SETUP}$  disable-to-enable =  $t_{PLZ} - t_{PZH}$  or =  $t_{PHZ} - t_{PZL}$ ; whichever yields the most positive number governs. Obviously if disable time is larger than

enable time then  $t_{SETUP}$  is a positive time. Worst case  $t_{SETUP}$  is calculated from the min/max enable times:  $t_{PLZ}(\max) - t_{PZH}(\min)$  or  $t_{PHZ}(\max) - t_{PZL}(\min)$  and will always yield a safer positive number.

Data taken on a 245 function in a bus contention test fixture may be helpful to illustrate the effects of varying the  $t_{SETUP}$  from a value which caused no contention to values which caused significant contention in Figure 1, Figure 2 and Figure 3.

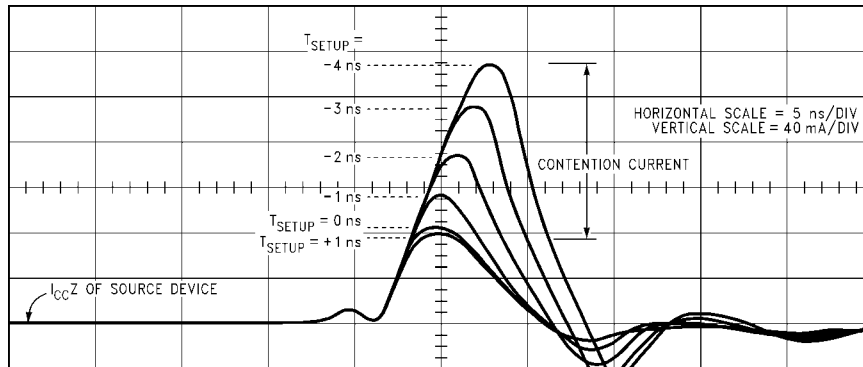
No reliability data to calculate fit rates to support a degree of contention resilience is offered at this time. Deliberate contention is not recommended. For instance a designer should be rightly concerned about the magnitude of current that can flow when a 64 mA (min) bus interface sink ( $I_{OL}$ ) stage contends with a -225 mA (max) source ( $I_{OS}$ ) stage for a large overlap time period with multiple outputs switching. Particularly true for the newer bus interface parts like ABT which have  $I_{OS}$  specifications more negative than the -225 mA max.



**FIGURE 1. 245 Function Bus Contention Test Fixture**

Procedure: Adjust  $t_{SETUP}$  by varying the delay of B pulse. Monitor contention current of OR-tied B outputs at node 1.

## Avoiding Bus Contention (continued)



At  $T_{SETUP} = +1ns$ , there is no contention current, merely normal capacitive charging during LH transition. Bus contention is measured with 8 outputs switching in phase on both devices. This example used the 74F245PC, with the monitor on pin 18,  $B_{OUT}$ .

FIGURE 2. Bus Contention Current

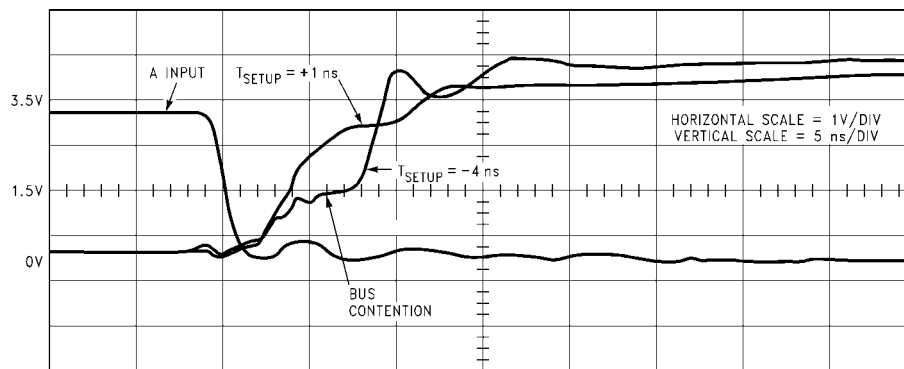


FIGURE 3. Output Response in Bus Contention Test Fixture

## Floating Input Considerations for BiCMOS Design

### ABT INPUT STRUCTURE DESIGN

Although the inputs of a BiCMOS device operate with TTL voltage levels, it is important to understand that the circuitry is built primarily with CMOS structures. Figure 4 shows the basic structure of a typical ABT input. The nature of the ABT input operation is very similar to that of Advanced CMOS devices. There is minimum power dissipated due to  $I_{CC}$  when the input is in either the High or Low logic state; since only one structure will be turned on at a time. Special considerations for power dissipation must be made however, when the inputs of a BiCMOS device are being subjected to an undefined level—such as that on a 3-STATE system bus.

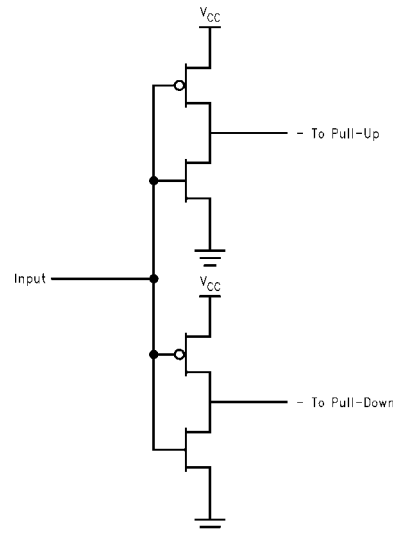


FIGURE 4. Simplified ABT Input Structure Diagram

## Floating Input Considerations for BiCMOS Design (continued)

### EFFECTS OF FLOATING INPUTS

Typically, a number of bi-directional transceivers will be connected in parallel with each other between two system busses; as in Figure 5. Before data can be transferred from one bus to the other, the devices connected to the receiving bus will have their outputs disabled for some period of time prior to the appearance of valid data on the driving bus. This is necessary to prevent data corruption and contention between busses. While the outputs are disabled, there is minimum concern for the effects of  $I_{CC}$  on power dissipation—the output enable circuitry is designed to interact with the input stages to effectively cause them to act as open circuits to  $V_{CC}$  and ground. Floating inputs become a concern when the outputs are enabled and there are a number of inputs that remain connected to a 3-STATE system bus for a period of time.

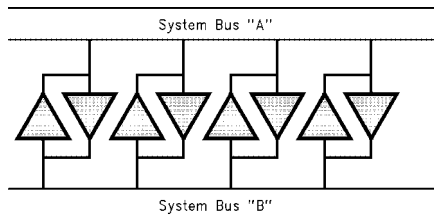


FIGURE 5. Bi-Directional Bus Transceivers

During the time that the bus is inactive, 3-STATE leakage currents will charge the lines to some voltage level within the input threshold region of the device. In the threshold region, and with the outputs enabled, the output pull up and pull down stages may be partially turned on simultaneously. This results in significant flow of  $I_{CC}$  through the input structure to ground. This current is orders of magnitude larger than the typical leakage currents  $I_{IH}$  or  $I_{IL}$ . Given that this is occurring on a number of transceivers located on the same physical device, the problem is compounded. Permanent damage or long term reliability effects on the device may become a concern.

### SYSTEM DESIGN CONSIDERATIONS

In a BiCMOS system design, floating inputs can be dealt with using one of two methods. If the amount of time that the bus is going to be inactive is very short (on the order of microseconds), then the issue can be disregarded. Because this time can be unpredictable due to normal variations in operation the more commonly used approach will be to ensure that the system bus is always going to be at a

valid voltage level. This is accomplished with the use of a pull up resistor to terminate the bus line. It is recommended that a 1k to 10k resistor be connected between the device input and  $V_{CC}$ . Although additional considerations will be made for DC power dissipation by the termination network, pull up resistors will ensure an added level of protection against the effects of floating device inputs.

### FAIRCHILD'S ABT DESIGN CONSIDERATIONS

Fairchild has considered the issue of floating inputs during design of the ABT product family. 8-bit and 16-bit 244 and 245 functions have been designed with additional protection against the effects of floating inputs. In previous discussion, we examined that when a device input is left at some voltage level near the threshold, it is possible for both the input pull up and pull down structures to be partially turned on and conducting  $I_{CC}$  to ground. Depending on the number of inputs at threshold, and the time that they are in the threshold region, the results could be adverse to both the device and the system. Fairchild Semiconductor has designed the input structures of their ABT buffers and transceivers such that the pull up and pull down structures will completely shut off while the input voltage is within the threshold region. This is accomplished by controlling the characteristics of the pull up and pull down structures such that there is an imbalance between their turn on voltages. This prevents simultaneous conduction of the input structures with the presence of a threshold voltage at the input. Figure 6 demonstrates the shutdown of the input structures between the input voltages of 1.2V and 1.4V.

### SUMMARY

Because CMOS structures are incorporated into the ABT input circuitry, considerations must be made for the resulting effects upon device inputs that are connected to a bi-directional 3-STATE system bus. If these lines are not terminated to a valid input level, the result will be  $I_{CC}$  current flow to ground—compounded by the number of inputs that are exposed to threshold levels. The power being dissipated internally to the device may have an effect on long term device and system performance; or may result in a catastrophic failure. Standard system design practice suggests that floating input pins be terminated with a pull up resistor to  $V_{CC}$ . This practice—in conjunction with Fairchild's robust ABT input design—will ensure that the system designed with ABT logic devices will operate efficiently and reliably.

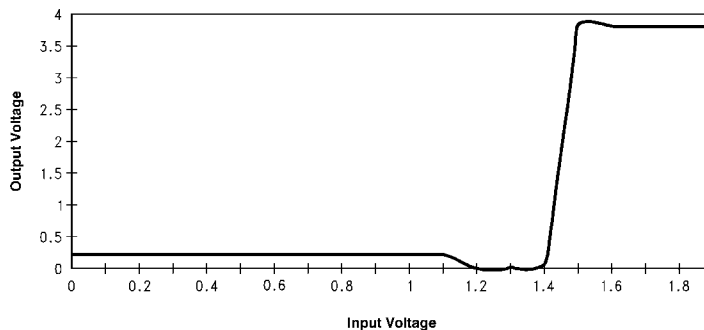


FIGURE 6. Input Characteristics Demonstrating Shutdown at Threshold Levels

## Power Down Characteristics

Power-down characteristics provide the system designer's with an understanding of the loading effects from a device when the device power supply is at 0.0V. The device's powered-down characteristics effect the system bus or backplane in a number of ways and can be characterized by its input and output capacitance and current loading. The measured parameters that provide the designers with loading information include;  $C_{IN}/C_{OUT}$ , input/output capacitance;  $I_{ZZ}$ , tri-stateable output power-down current loading;  $V_{ID}$ , input power-down current loading.

A device's input and output capacitance define the effective bus and backplane loading through the charging and discharging of the interface pins. ABT devices have typical capacitance values of 5 pF for input pins and 9 pF for output pins, while I/O pins have a typical value of 11 pF. Fairchild tests capacitance in accordance with the procedures outlined in the MIL-STD-883, method 3012.

The power-down leakage characteristics of an ABT device provide the effects of current loading on a bus or backplane. Typically, loading leakages in the +200  $\mu$ A range begin to effect the  $V_{OH}/V_{OL}$  levels in a backplane application. The  $V_{ID}$  and  $I_{ZZ}$  curves in Figure 4 and 5 illustrate the loading effects on the backplane over a range of backplane voltages from 0.0V to 5.5V while the power supply is kept at 0.0V.

### VID

$V_{ID}$  is a voltage that is measured on an input pin at a current loading of 1.9  $\mu$ A in a power off condition such as when  $V_{CC}$  and the non-measurement pins are at 0.0V.

The curve of  $V_{ID}$  vs  $I_{ID}$  in Figure 7 shows the current leakage of a typical ABT input pin. ABT inputs typically limit loading leakage to <1.9  $\mu$ A over an input voltage range from 0V to 5.5V at room temperature.

### IZZ

$I_{ZZ}$  is a current that is measured on an output pin at a voltage of 5.5V during a power off condition such as when  $V_{CC}$  and the non-measurement pins are at 0.0V.

The curve of  $V_{ZZ}$  vs  $I_{ZZ}$  in Figure 8 shows the current leakage of a typical ABT input/output (I/O) pin and how it loads a bus or backplane over a range of bus voltages from 0.0V to 5.5V. I/O pin configurations exhibit combined current characteristics from components of the input circuitry and output circuitry. ABT I/O pins specify maximum loading leakage at 100  $\mu$ A with a typical loading leakage  $\pm$  3  $\mu$ A at room temperature.

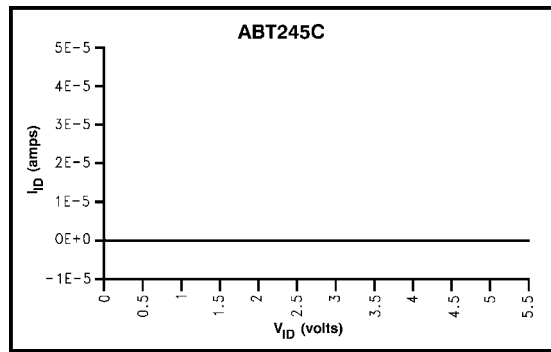


FIGURE 7.

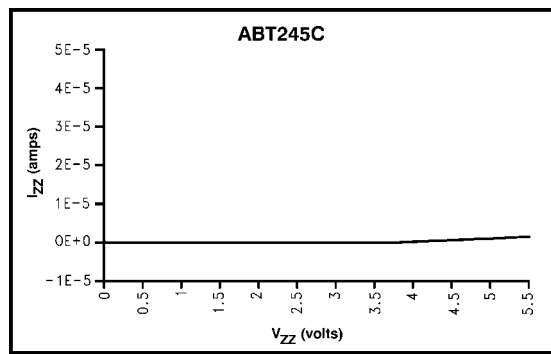


FIGURE 8.

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