

GTLP Product Feature Matrix

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Feature	Device Name													
	GTLP10B320	GTLP16612	GTLP16616	GTLP16617	GTLP16T1655	GTLP17T616	GTLP18T612	GTLP1B151	GTLP1B153	GTLP2T152	GTLP6C816	GTLP6C816A	GTLP6C817	GTLP8T306
A feedback path for control and diagnostics monitoring	X							X						
A Port source/sink -12mA/+12mA													X	
A Port source/sink -24mA/+24mA	X				X	X	X	X	X	X	X	X		X
A Port source/sink -32mA/+32mA		X	X	X										
B Port sink +40mA													X	
B Port sink +50mA	X					X	X	X	X	X	X	X		X
B Port sink +100mA					X									
Bidirectional interface between GTLP and LVTTTL logic levels	X	X	X	X	X	X	X	X		X				X
Bushold data inputs on A port to eliminate the need for external pull-up resistors for unused inputs	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D-type flip-flop, latch and transparent data paths		X	X	X	X	X	X							
Designed using Fairchild advanced BiCMOS technology	X				X	X	X	X	X	X		X		
Designed using Fairchild advanced CMOS technology		X	X	X							X		X	X
Designed with edge rate control circuitry to reduce output noise on the GTLP port		X	X	X		X	X	X	X	X	X	X	X	X
External pin to pre-condition I/O capacitance to high state (V _{CC} BIAS)					X									
Flow through pinout optimizes PCB layout	X	X	X	X	X	X	X	X	X	X				X
GTLP buffered CLKAB signal available (CLKOUT)			X	X		X								
Interface between LVTTTL and GTLP logic levels									X		X	X	X	
Low voltage version of GTLP6C816												X		
Open drain on GTLP to support wired-or connection	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Partitioned as two 8-bit transceivers with individual latch timing and output control but with a common clock					X									
Power up/down and power off high impedance for live insertion	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Special PVT compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Split LVTTTL inputs and outputs	X							X						
TTL compatible driver and control inputs	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Variable edge rate control pin to select desired edge rate on GTLP port (V _{ERC})	X				X									
V _{REF} pin provides external supply reference voltage for receiver threshold adjustability	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1:2 fanout clock driver for GTLP port											X	X	X	
1:6 fanout clock driver for TTL port											X	X	X	
5V over voltage tolerance on LVTTTL ports		X	X	X							X		X	X

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