

Section 7 - Backplane Transceiver Technologies Backplane Designer's Guide

Many integrated circuit manufactures supply transceiver technologies that are designed primarily for backplanes with specific parameters in mind. One device technology might focus on low power consumption and another on high speed. There are also technologies that try to offer a complete solution by addressing each and every backplane issue.

A large part of backplane design is focused on which device technology best suits the design. This section serves as a guide to choosing among the following backplane transceiver technologies:

- Transistor-transistor logic (TTL)-based: Advanced BiCMOS Technology (ABT), Low Voltage Technology (LVT), and Fast CMOS Technology (FCT). These three technologies represent families that are suited for moderately loaded backplanes.
- Differential technologies: Emitter Coupled Logic (ECL) and Low Voltage Differential Signaling (LVDS). These are differential signal alternatives to TTL solutions that can achieve higher backplane frequencies.
- Gunning Transceiver Logic Plus (GTL) standard, derived from the JEDEC GTL standard. When compared to other available technologies, this type is capable of driving heavily loaded backplanes.

Section Reference

This section presents information covering:

- Backplane transceiver technologies
- Performance
- Features
- Drawbacks
- Comparisons

Section	Section Title	Contents
1	Introduction	Application demands, basic backplane considerations, and how to use this guide.
2	Backplane Protocols	Descriptions of different backplane bus protocols, including PCI- and VME-based protocols.
3	Backplane Architecture	Topics relevant to backplane configuration, including parallel versus serial configuration and different configuration topologies and timing architectures
4	Backplane Design Considerations	Issues relevant to backplane layout, including distributed capacitance, transmission line effect, stub length, termination, and throughput.
5	Backplane Signal Driving and Conditioning	Signal driving and conditioning, including power consumption, rise/fall time, propagation delay, flight time, device drive, pin conditioning, live insertion, and incident wave switching.
6	Noise, Cross-talk, Jitter, Skew and EMI	A review of the enemies of signal integrity and high frequency.
7	Transceiver Technologies	Detailed information about the following technologies: TTL-based (ABT, FCT, and LVT); ECL; and GTLP.
8	Mechanical Considerations	Information about mechanical considerations such as backplane chassis/cages and connectors.
9	Layout Considerations	Physical layout of the receiver and driver cards plugged into the backplane, primarily focusing on construction of the physical layer and the configuration of the devices that comprise the cards.

Feature Comparison

This section presents an overview of the devices covered in this section. It compares the offerings of each design family in relation to backplane design issues. Often a large part of the selection process involves comparing features: choosing which are most important to a particular design while not compromising too much in another area. The values in the table below are typical for the technologies listed.

	ABT	LVT	FCT	ECL	LVDS	GTLP
Noise Margin (H/L) (mV)	500 / 250	400 / 400	500 / 300	N/A	N/A	450 / 400
Freq (Typ Max) (MHz)	80	80	80	1000	200	125
Transmission Mode	Single-ended	Single-ended	Single-ended	Single-ended or Differential	Differential	Single-ended
Supply Voltage (V)	5	3.3	5	3.3 / 5	3.3 / 5	3.3 / 5
Supply Current (mA)	30	9.5	10	50 to 65	3.5 to 7	40
Input Current (μA)	-5 / 5	-5 / 1	-1 / 1	0.5 / 240	-20 / 20	-10 / 10
Drive (I_{OL}/I_{OH}) (mA)	-32 / 64	-32 / 64	-32 / 64	-50 / 50	-8 / 8	50 - 100
Speed t_{PD} (typ) (ns)	3	3.5	4.5	0.5	1.7	4
Edge Rate Control	No	No	No	No	No	Yes

TTL-based Technologies

A TTL backplane is a system bus that uses transistor-to-transistor logic levels to transmit data through the system. This section discusses three device technologies based on the TTL I/O standard: ABT, LVT, and FCT. These technologies are considered together because they are high-drive devices designed for TTL backplane applications and because they offer similar performance.

A backplane device must be capable of dealing with the required frequency (or speed) and number of loads. As the demand for backplane speed grows, ABT, LVT, and FCT become more limited in their performance because they were designed to drive a certain number of loads in a defined frequency range. As the demand grows for higher frequencies and number of loads, the demand for higher performance drivers also increases.

Comparison of ABT, LVT, and FCT Technologies

Once the designer determines the frequency at which the backplane will operate and the number of loads the driver will see, these performance demands can be compared to the capabilities of ABT, LVT, and FCT to see if these technologies meet design needs. Here is a comparison of the overall features of these three technologies:

- ABT and LVT are based on BiCMOS technology; FCT is based on CMOS.
- ABT has the lowest I/O capacitance. This is a concern if the design is sensitive to capacitance.
- LVT maximum propagation delay is 3.5ns; ABT maximum propagation delay is 3.9ns, depending on the manufacturer of the device.

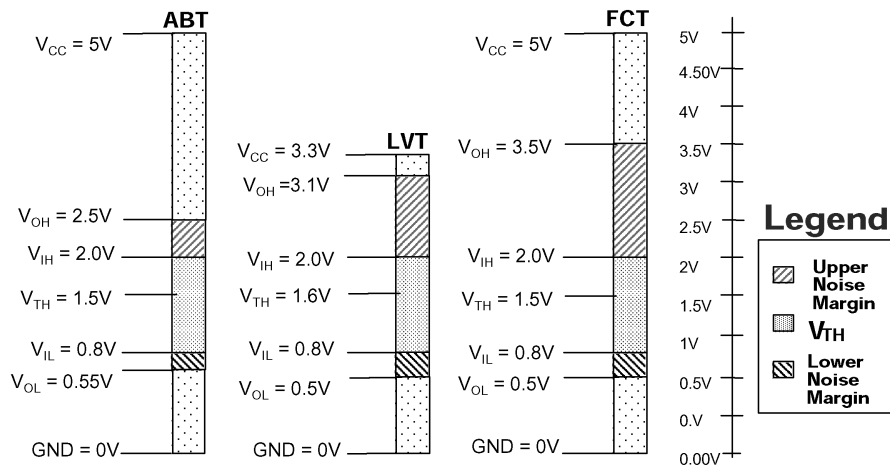


FIGURE 1. Signal levels for ABT, LVT, and FCT

TTL-based Technologies (Continued)

Noise Margins

Noise margin is the amount of input noise a device can tolerate and still maintain the integrity of its logic levels. It is important to consider the noise margins of the three choices. Figure 1 shows a comparison of the voltage levels of ABT, LVT, and FCT. The noise margin is measured between V_{OH} and V_{IH} for the upper noise margin, and between V_{IL} and V_{OL} for the lower noise margin.

As an example, V_{TH} for LVT is $V_{CC}/2$. Below this level the device input should be in low state. However, the LVT guaranteed V_{IL} specification is 0.80 V. With a V_{IL} of 0.80V and input V_{OL} of 0.50V the noise margin is 0.30V. Within the specification guarantee, voltage LOW-to-HIGH noise transient would need to rise above 0.80V to place the input in jeopardy of switching states.

The following table represents the numerical value of the noise margins for these devices.

	ABT	LVT	FCT
Upper Noise Margin	500mV	1.1V	1.5V
Lower Noise Margin	250mV	300mV	300mV

ABT

ABT (Advanced BiCMOS Technology) is a 5V V_{CC} TTL device suitable for use in a backplane based on TTL architecture. In many situations TTL solutions provide sufficient performance while including other benefits such as low cost and a wide selection of functions and packages. This section presents the main features and performance characteristics of ABT.

ABT Features

The following list is an example of many important features offered on a standard 74ABT16245 device:

- 10pF input/output capacitance

- Low static and dynamic power consumption
- High output drive (-32 mA I_{OH} / $+64$ mA I_{OL})
- 5V supply voltage
- Guaranteed low ground bounce
- Live insertion capability – with power-up/power-down 3-STATE
- 3.9ns maximum propagation delay
- Cost efficiency

ABT Performance

Devices in the ABT family are well suited for backplane designs because they can handle high data rates and a significant number of loads. At one time, ABT was considered a high-performance driver IC technology for use in backplanes, but, with the constant migration to higher data rates and number of loads, ABT's performance has been surpassed by other technologies, such as GTLP, that offer even higher speeds. ABT is limited to the 10 to 33 MHz range with up to 20 loads, but, if a backplane operates in ABT's window of functionality, the features of this device make it worth consideration.

ABT Power Consumption

The ABT device family offers low-static, dynamic power consumption. As the name suggests, Advanced BiCMOS Technology controls power consumption by relying heavily on BiCMOS technology that combines the most desirable parameters from both Bipolar and CMOS. When the system is in quiescent state, BiCMOS power dissipation is reduced relative to bipolar devices. The only static power dissipated is due to the small leakage currents I_{CCH} and I_{CCL} . ABT's dynamic power consumption is reduced relative to other technologies because of its low output voltage swing. Figure 2 shows a comparison of dynamic power consumption between ABT, LVT, and FCT (based on the 244 function).

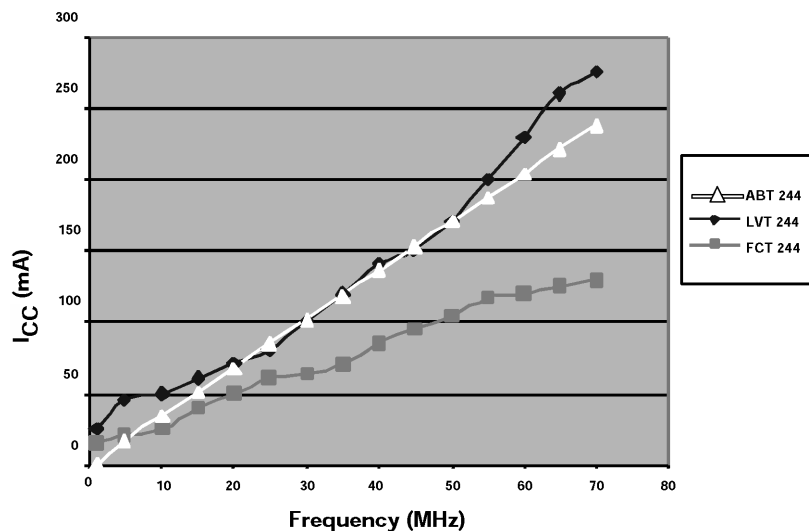


FIGURE 2. Dynamic Power Consumption Comparison

ABT (Continued)

ABT Disadvantages

There are drawbacks to the ABT technology. The device is unable to produce incident wave switching in heavily loaded backplanes that operate at high frequencies. As new system designs demand increased performance, the ability of ABT to produce incident wave switching decreases significantly.

Any device driver technology can produce incident wave switching under perfect backplane conditions, but backplane conditions are rarely ideal. In many situations, where the number of loads is significant, an ABT device must rely on a reflected wave to signal the receivers in the backplane. Since the receivers have to wait for the reflected wave to be signaled, valuable time is lost switching the backplane. Because of this, ABT device technology is limited in speed and number of loads.

LVT

Low Voltage Technology (LVT) is optimized for off-board driving applications and offers mixed 3V - 5V capability by providing 5V over voltage tolerance at both the inputs and the outputs. LVT is fabricated on an advanced BiCMOS process and has many of the same features as ABT but is optimized for the 3V operating range.

LVT Features

LVT offers the following features, based on a standard LVT16245 device:

- 8pF input/output capacitance
- Low power consumption
- 3.3V supply voltage
- High output drive (-32mA I_{OH} / +64mA I_{OL})
- Live insertion capability – with power-up/power-down 3-STATE
- High speed (3.5ns max propagation delay)

Like ABT, LVT supports live insertion because the LVT family has the feature of power-up/power-down 3-STATE. The LVT device family also incorporates the option of bushold on the input and output pins. This means it will hold the last known valid state of the input when the input signal is removed. This feature eliminates the need for external pull-up or pull-down resistors. Devices with bushold can lower component count, save printed circuit board area, and reduce cost.

More information on bushold is in Backplane Designer's Guide Section 5, "Backplane Signal Driving and Conditioning."

LVT Performance

Another feature that the LVT device family has in common with ABT is performance in relation to frequency and number of loads. This means LVT can be placed in the 10 to 33 MHz operation range. LVT is based on a 3.3V power supply and offers the designer a low-voltage, low-power-consuming technology for backplane.

LVT Power Consumption

The LVT device family offers low static and dynamic power consumption. As with ABT, LVT is a BiCMOS technology that combines the most desirable parameters from both Bipolar and CMOS. BiCMOS power dissipation is reduced relative to Bipolar devices, and the only static power dissipation

is due to the small leakage currents I_{CCH} and I_{CCL} . LVT also has a 3V V_{CC} operating range. The lower V_{CC} range reduces power static power consumption. Additionally, the reduced output swing lowers dynamic power consumption.

LVT Disadvantages

LVT technology suffers from the same load and speed limitations as ABT. This limits LVT to backplanes that are not heavily loaded or to backplanes that use reflected wave switching for system timing operation.

FCT

Fast CMOS Technology (FCT) is as a low-power alternative to traditional 5V bipolar technology. The need to process large amounts of data in a relatively short amount of time is driving the demand for higher performing systems. As performance and system size increase, power usage becomes a concern.

FCT Features

The following FCT device characteristics are based on a standard FCT16245 device:

- 8pF input/output capacitance
- 4.6ns to 7ns propagation delay, depending on speed grade
- Low power consumption
- High output drive (-32 mA I_{OH} / +64 mA I_{OL})
- 5V supply voltage
- Live insertion, depending on type of FCT device – power-off disable. (Power-off disable is the ability of the device output to maintain a high-impedance state during power supply ramping, provided the output enable control pins are conditioned to place the outputs in a high-impedance state.)

In addition, some manufacturers offer a derivative of the FCT device family that is based on a 3.3V supply voltage.

FCT Performance

The FCT family has been designed to maintain the same high output drive capabilities as bipolar products (+64 mA I_{OL}), while decreasing static power dissipation and maximum propagation delay.

As a family, FCT devices usually have a propagation delay on the order of 7ns. However, FCT devices usually have three different speed grades: A, B, and C. The typical propagation delays for the speed grades can range from 7ns to 4ns. The speed grade is designated on the device number. Check manufacturer's specifications to see what propagation delay time is offered.

FCT Power Consumption

FCT is an all CMOS technology and offers low power consumption and high speed. Figure 2 shows the power consumption of FCT compared with other device technologies.

FCT Disadvantages

One drawback to FCT devices is the amount of noise they can generate. Because of the characteristics of the CMOS technology and the 5V output swing, FCT devices are more susceptible than BiCMOS devices to noise such as ground bounce. Noise can cause several problems: decreased

FCT (Continued)

throughput, poor signal integrity, and, if the problem is severe enough, false triggering.

Additional potential drawbacks to FCT are the technology's load and speed limitations. FCT is designed for the same type of performance as ABT and LVT. Because of this, FCT is limited to 10 MHz to 33 MHz operation for most backplane environments.

ECL

Emitter Coupled Logic (ECL) technology has some significant advantages over other technologies. The most obvious advantage is speed. Some ECL device families have buffer propagation delays as low as 300ps and specified maximum frequencies (f_{MAX}) above 1 GHz. These speeds, combined with a high level of noise immunity and low noise generation, make this family the obvious choice when very high speed is required. ECL offers an additional feature that adds flexibility: the choice of single-ended or differential transmission architecture.

ECL is designed primarily for point-to-point architectures. However, it can be designed into a multidrop environment. ECL uses devices such as generic registers and buffers to perform the function of a transceiver.

Due to the combination of differential signaling, high speeds, and specific ECL device technology, the transmission line and components used for ECL have very specific requirements. Before using ECL in a backplane design, it is important to consider transmission line media (microstrip, strip-line, coaxial twisted pair), terminations, connectors, power planes, and loading effects.

ECL Technology

ECL technology is designed around a very low swing (800mV is typical) differential amplifier, as illustrated in Figure 3. This amplifier is supplied by a current source (Q_5), and current is switched from between the sides of the differential amplifier by the voltages on the device inputs. The device differential inputs are connected to the transistor bases of the differential amplifier (Q_1 and Q_2). The differential amplifier collectors are connected to the base of the output drive transistors (Q_3 and Q_4). These output transistors have the collector connected to V_{CCA} and the emitter coupled to the load.

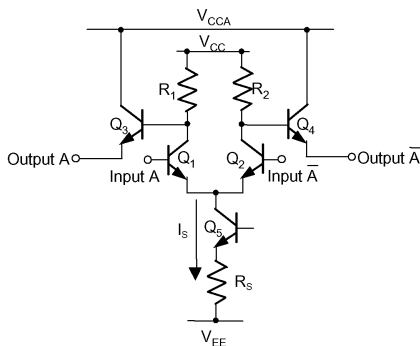


FIGURE 3. Simplified Schematic of an ECL Device

The emitter follower output configuration provides isolation of the differential amplifier from the output load, as well as current driving capability (50 mA typical).

ECL devices are current driving devices and require very specific circuit layout and loading conditions including an output connection to a Termination Voltage (V_{TT}) for proper operation. ECL is particularly immune to noise when used in a differential configuration. Noise coupled concurrently onto both signal lines will be ignored by the input. This common mode rejection gives differential technologies much better noise immunity than most single-ended technologies.

Another advantage of ECL is low noise generation. Although ECL has extremely fast propagation speeds, the edge rates are not fast. These soft edges coupled with 800 mV swings generate very little ground bounce or EMI.

ECL families are designed using bipolar transistors to take advantage of their high switching speeds and current driving capability. However, bipolar devices use much higher levels of quiescent power than equivalent CMOS devices. Some new ECL families are designed using BiCMOS technology to reduce I_{CC} power usage.

ECL Features

ECL devices offer the following features:

- Backplane frequencies over 200 MHz possible
- Single-ended or differential transmission setups
- High noise immunity
- Low noise generation

ECL also has the ability to drive transmission lines, with impedances as low as 25Ω . As a transmission line's impedance decreases, the speed of the transmitted signal increases providing a significant increase in overall system performance.

Single-ended Setup

In a single-ended ECL backplane, signals are transmitted as a voltage on a single line that is referenced to AC ground. Figure 4 shows an example of a backplane using ECL in a single-ended setup.

ECL (Continued)

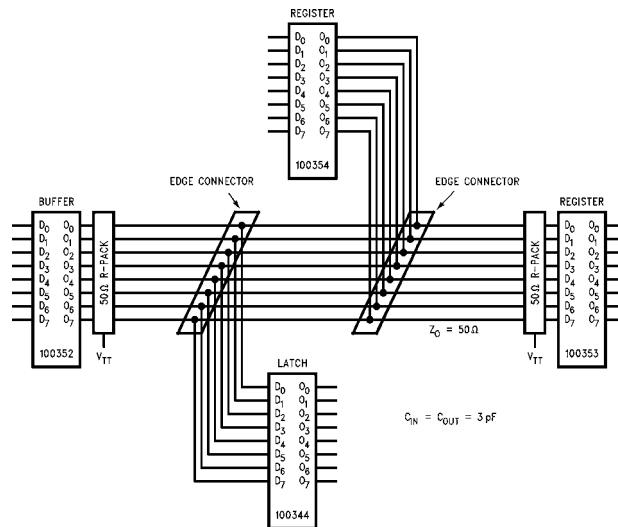


FIGURE 4. Single-ended ECL backplane

In this configuration there are several drivers and receivers tied into one common backplane. The 50Ω transmission line is terminated at both ends of the line into its characteristic impedance, also 50Ω. With this type of a setup a driver that is capable of driving 25Ω driver is required. Figure 4 shows a Fairchild Semiconductor register and octal latch in this backplane setup using ECL devices.

One characteristic of a single-ended backplane environment is susceptibility to ground potential differences at the ends of the lines. This can create a distorted signal that transmits throughout the backplane. For this reason, imple-

menting a single-ended setup in a noisy backplane environment is not recommended.

Differential Setup

The differential setup offers an alternative to a single-ended setup and has improved noise immunity. Figure 5 shows how ECL can be implemented into a backplane using a differential setup. The two major benefits of using ECL with a differential setup are higher data rates and higher noise rejection.

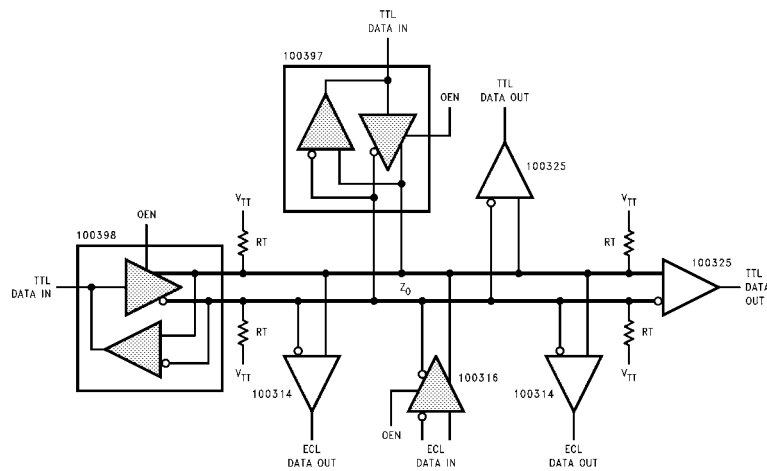


FIGURE 5. Differential ECL Backplane

More information on backplane architecture setups is in Backplane Designer's Guide Section 3, "Backplane Architecture."

ECL (Continued)

Advantages Over TTL Devices

ECL devices have many advantages over standard TTL devices, including:

- Non-saturating logic that results in much faster switching speeds for drivers tied into the backplane than the speeds equivalent TTL technologies offer.
- Reduced capacitance created by this device gives a lighter equivalent capacitive load. This also allows ECL devices to achieve faster switching speeds as compared to TTL.

The following table shows a comparison between ECL devices and TTL devices.

Capacitance	ECL (Typical)	TTL (Typical)
Input	3.0pF	5.0pF
Output	3.0pF	5.0pF

Note that the total I/O capacitance of ECL is 6pF, compared to ABT at 10pF, LVT at 12pF, and FCT at 14pF.

ECL Disadvantages

ECL has some very important drawbacks, including:

- Power consumption: ECL consumes a large amount of power compared to other device technologies. This is due to the architecture of the devices.
- Complexity: Implementing an ECL design is more complex than single-ended technologies.
- Cost: The cost of implementing an ECL solution is very high compared to other technologies.

GTLP

Gunning Transceiver Logic Plus (GTLP) is a high-speed, low-power-consumption, cost-effective solution for high-performance backplane applications. GTLP technology's reduced voltage swing, tight threshold differential receivers, and controlled edge rates enable designers to optimize backplane design and achieve incident wave switching. GTLP allows existing parallel architectures to be upgraded to higher switching speeds without the radical change to a serial-based system.

Gunning Transceiver Logic (GTL), invented by William Gunning, was standardized by JEDEC as a low-swing input/output driver. From GTL, Fairchild Semiconductor developed GTLP to improve GTL's noise margins.

The GTLP device family is designed primarily for backplane driving applications. It has distinct advantages over other device families and addresses specific backplane design issues. GTLP incorporates a unique feature set with high-performance backplane driving in mind. These features including a reduced output swing, tight receiver threshold, edge rate control, low voltage, low power consumption, and high-speed. GTLP can operate in excess of 125 MHz (f_{MAX}) because it is specifically designed with a slower edge rate for optimum performance in a distributed load configuration. Figure 6 shows a performance comparison of GTLP to some TTL device families often used in backplane applications.

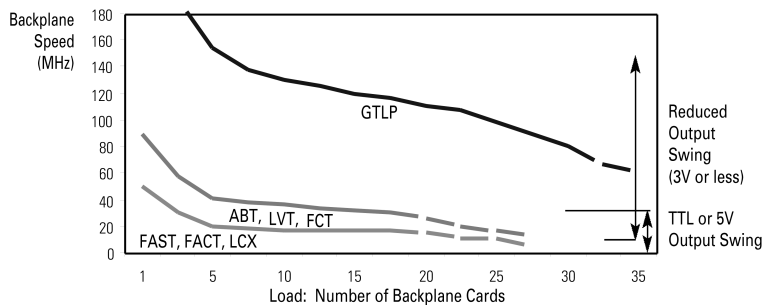


FIGURE 6. GTLP Performance Compared to Other Technologies

GTLP Technology

The GTLP device family incorporates an open drain output design on the backplane driving side of the device. This requires the bus to be actively terminated for proper signaling. For GTL and GTLP this termination should be pull-up resistors to a termination voltage (V_T) and should match backplane impedance to minimize reflections.

GTLP backplane signal levels are reduced swing of 1.0V or less. This output voltage level is typically $0.55 V_{OL}$ to $1.5 V_{OH}$. V_{OH} can be as low as 200 mV above the V_{OL} level. GTLP V_{OL} level is 0.15V above GTL V_{OL} of 0.4V. This increases GTLP V_{OL} low level noise immunity.

GTLP also contains a user-defined V_{REF} level that can be adjusted from 0.95V to 1.05V for best performance in a backplane design.

The non-backplane side of GTLP devices is a TTL-compatible, low voltage (3.3V range) CMOS transceiver design. This is comparable in performance to the LCX CMOS family.

GTLP Features

The GTLP device family offers many desirable characteristics, including:

- Incident wave switching that enables higher throughput
- Reduced swing, tight threshold, and controlled edge rates for low noise and EMI
- Adjustable variables (R_{TERM} , V_{TT} , and V_{REF}) to optimize backplane characteristics
- Live insertion capability
- Interface with TTL to GTLP

GTLP (Continued)

TTL Performance Comparison

Figure 7 shows the superior performance of a typical GTLP backplane compared to a similar TTL backplane. Two comparisons are shown in the figure:

- The GTLP backplane achieves incident wave switching while the standard TTL backplane does not. This results in a shorter propagation delay time for the GTLP backplane.

- Note the number of resistors used in the GTLP backplane compared to the number used in the TTL backplane. GTLP uses a lower value of resistance and half the number of resistors because GTLP can successfully be terminated with the setup shown above. The TTL backplane uses a Thevenin termination for backplane termination.

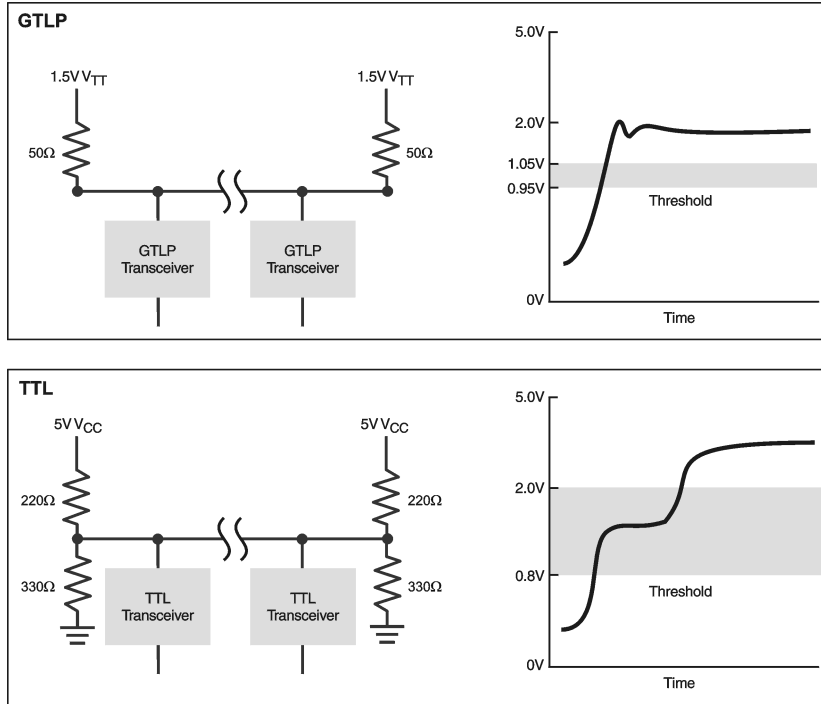


FIGURE 7. Typical GTLP Backplane vs. Typical TTL Backplane

General GTLP Characteristics

GTLP technology features include high noise margin, reduced swing, low power consumption, high speed, and adjustability to the backplane environment.

GTLP Noise Margin

The designer must account for the amount of noise seen by the receiver and must select a device that corresponds to the amount of noise generated on the backplane. The noise the receiver usually contends with is from the effects of ground bounce, EMI, and cross-talk. GTLP receivers are able to reject much of this noise due to the input noise margin and adjustable V_{REF} .

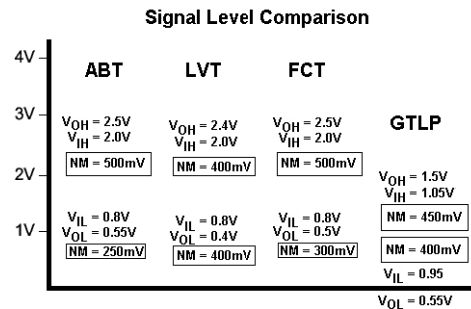


FIGURE 8. Signal Levels

GTLP (Continued)

Reduced Swing

With a reduced output swing of one volt or less, GTLP has many benefits. The most obvious is much faster transitions that allow for a higher backplane speed than with TTL technologies. Also, since the device does not have to transition as far, the transition can be much less steep than a 0V to 3V transition. This significantly lowers $\Delta V/\Delta t$ and results in much lower noise levels from ground bounce, ringing, cross-talk, and EMI. Compared to TTL technology, GTLP offers much lower swing, resulting in:

- Lower EMI seen by the GTLP device
- Better incident wave switching
- Higher throughput

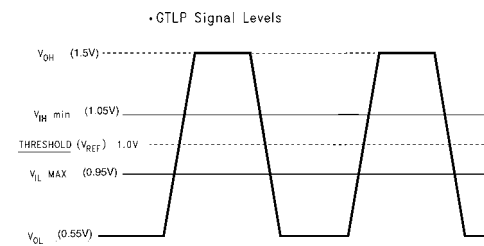


FIGURE 9. GTLP Signal Levels

Figure 9 shows the reduced signal levels of a GTLP device. Note the reference voltage is set at 1V.

Adjustability to backplane environment

GTLP devices offer characteristics that allow the device to be adjusted to perform optimally in specific backplane environments. These characteristics include higher throughput, incident wave switching, lower EMI, and reduced noise effects in the backplane.

Fairchild Semiconductor's GTLP devices allow the adjustment of three key variables: termination resistance (R_T), termination voltage (V_T), and reference voltage (V_{REF}). V_T and R_T fine-tune a termination scheme, which contributes to factors like power consumption and noise margin. V_{REF} allows the voltage output signal to swing above and below a fixed point, typically 1V.

Termination Voltage / Resistance

The method of termination can affect signal integrity and power consumption. With GTLP technology, there are two termination methods: parallel and Thevenin. These two schemes allow the termination voltage and termination resistance to be set to specific values. For GTLP devices the termination voltage used in the backplane is usually 1.5V. Termination resistance values depend on the method of termination. For GTLP:

- Parallel termination configuration uses a termination resistance equal to backplane Z_0 . At higher frequencies, parallel termination will consume less power because of lower AC power consumption.
- The Thevenin termination resistance is usually set to twice backplane Z_0 .

V_{REF}

The GTLP device has a voltage reference pin that allows the designer to set a voltage around which the output signal "swings." In many backplane applications that use GTLP, the voltage reference pin is set at 1V, allowing the output signal to swing above and below 1V. For GTLP, the output voltage signal swings at 0.5V above and 0.5V below V_{REF} , which allows the GTLP device to be set according to the voltage levels required in the backplane. V_{REF} sets the receiver threshold level (not the range). The receiver threshold is ± 50 mV of V_{REF} .

GTLP Incident Wave Switching

Incident Wave Switching (IWS) is important to the designer who wants to extract the greatest possible amount of performance from a backplane design. GTLP is specifically designed to achieve incident wave switching in a heavily loaded backplane environment. GTLP's controlled edge rate, tight threshold, and high drive are all features that contribute to achieving IWS. The output control circuitry of GTLP allows the output signal to be optimized, depending on the backplane environment.

By adjusting the value of R_T , the designer can match the termination impedance to the backplane environment and enable the backplane to achieve incident wave switching.

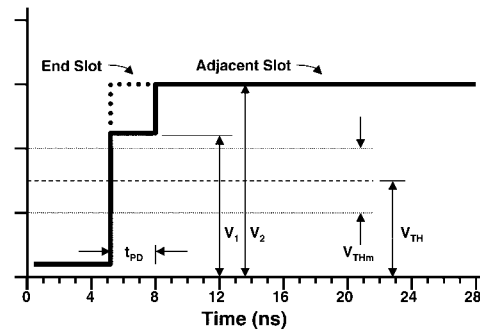


FIGURE 10. Desired Shape for Incident Wave Switching

Figure 10 shows an ideal waveform shape that produces IWS, where:

- V_1 = the desired voltage level across the backplane necessary for IWS
- V_2 = the typical V_{OH} level of a driver output
- V_{THm} = input threshold margin voltage
- V_{TH} = input threshold voltage
- t_{PD} = propagation delay of the backplane

Figure 11 compares a device with a clean incident wave, such as GTLP, to a device with a reflected signal, such as ABT, LVT, or FCT.

GTLP (Continued)

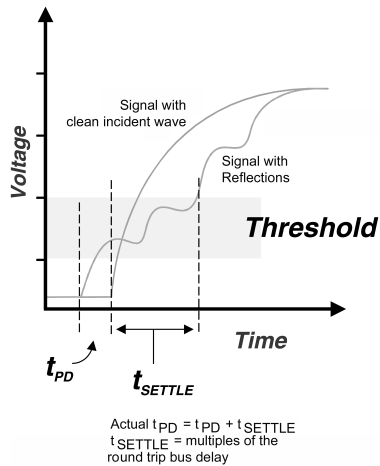


FIGURE 11. Clean incident wave enhances performance.

GTLP Throughput

The ideal backplane architecture for promoting increased throughput and incident wave switching is one that has low-capacitive loading through low-driver/receiver capacitance, short stub lengths, and efficient connectors. Under these conditions, the GTLP family of devices can demonstrate incident wave switching and very high throughput. The throughput rates for GTLP devices are in the order of

200 Mbits/s – 3.6 Gbits/s, depending on the device (1 bit - 36 bit).

Live Insertion Capability

GTLP allows insertion or extraction of a board in a backplane without powering down the host system or suspending an active backplane. All GTLP devices incorporate power-up/power-down 3-STATE circuitry.

Some devices provide output pins with precharge circuitry. Precharge places the voltage on the output pins at mid-swing levels during insertion or extraction. Setting the voltage at midswing during insertion minimizes the capacitive loading effects on the signals of an active backplane.

More information on live insertion and precharge is in Backplane Designer's Guide Section 5, "Backplane Signal Driving and Conditioning."

Controlled Edge Rates

Fairchild Semiconductor's GTLP devices incorporate output control circuitry to address one of the most prevalent problems with high-speed devices: output switching noise. Overshoot, undershoot, and ground bounce all fall under the category of output switching noise. The output design incorporates wave-shaping techniques that optimize GTLP devices for driving backplanes. The main focus is to control the output level transition. This minimizes switching noise and electromagnetic interference, and reduces signal-settling time.

Figure 12 illustrates the areas of the output transition (LOW-to-HIGH and HIGH-to-LOW) that are addressed by the GTLP output control circuitry.

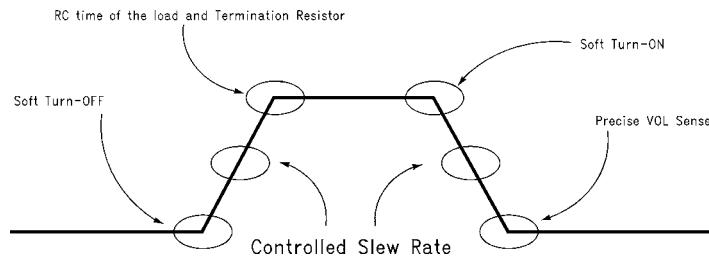


FIGURE 12. GTLP Transition Waveform

Figure 13 shows the reduced noise generated by a GTLP device as compared to that of a TTL-based device. The noise of a GTLP device is much lower than that of a standard TTL device because the GTLP device creates a clean output signal.

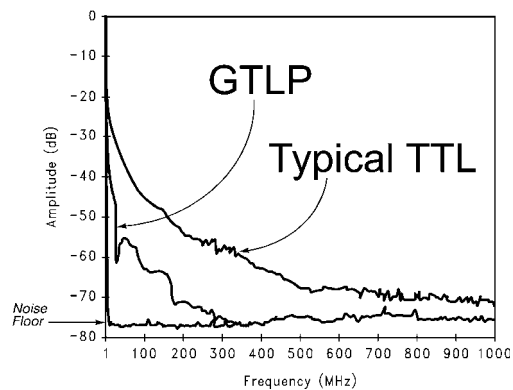


FIGURE 13. Controlled edge rates reduce noise and EMI

LVDS

LVDS is a low-voltage, low-power, differential technology used primarily for point-to-point and multidrop cable-driving applications. It is also used in serial backplane applications, and higher drive LVDS families have also been developed for multidrop backplane use.

LVDS is defined in the ANSI/TIA/EIA-644 standard and was developed under the Data Transmission Interface committee TR30.2. The standard specifies a maximum data rate of 655 Mbit/s, although some of today's applications are advancing well above this specification for a serial data stream.

Compared to other differential cable driving standards like RS422 and RS485, LVDS has the lowest differential swing with a typical voltage swing of 350mV with a typical offset voltage of 1.25V above ground.

LVDS Technology

LVDS features a low-swing, differential, constant-current-source configuration that supports fast switching speeds and low power consumption. Figure 14 illustrates this configuration, which allows for other features not found in single-ended technologies, such as common mode rejection and fail-safe operation.

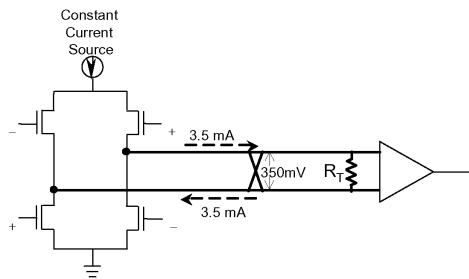


FIGURE 14. Figure 7-14. LVDS Driver / Receiver Schematic

LVDS Features

The LVDS device family offers many desirable characteristics, including:

- High-speed operation (≈ 200 MHz)
- Low power usage compared to other differential technologies
- Fail-safe operation

- Less complex implementation than ECL
- High noise immunity
- Low noise generation

General Characteristics of LVDS

This section describes the features of LVDS technology: high speed, high noise rejection, low power consumption, and fail-safe operation.

LVDS Differential Signal Operation

Differential signaling offers many advantages over single-ended technologies. LVDS signals center at 1.25V with a 350 mV swing. The signal position and value are not dependent on power supply voltage. Not only does this result in a faster, more stable signal, it also makes migration to lower power supply voltages much easier.

Another advantage of differential technology is that the balanced differential lines have tightly coupled equal but polar opposite signals to reduce EMI. The magnetic fields radiated by each of the conductors are drawn toward each other and cancel each other out.

LVDS Common Mode Rejection

Differential signals offer common mode rejection. The receiver ignores any noise that is coupled equally on to the differential signals and only considers the difference between the two signals. The LVDS receivers have the ability to reject common mode noise ranging from 0.5V to 2.35V. LVDS receivers will operate with as much as a ± 1 V ground shift between the driver and receiver. This is shown graphically in Figure 15.

Due to common mode rejection, differential signals also reduce signal integrity concerns at higher speeds. As throughput demands increase throughout the information industry, higher frequencies and wider bit widths cause transmission line reflections and cross-talk. As system loading increases, the characteristic impedance of a system can change and cause impedance mismatches. These mismatches generate reflective signals on the transmission line and these reflections, in turn, can cause bit errors or increase settling times. Reflections can also cause difficulty in achieving timing budgets as system speeds increase.

Differential signaling technologies like LVDS overcome these noise issues by ignoring common mode noise on the differential signal lines. Additionally, lower swing differential technologies reduce reflections by having small voltage swings that limit the energy supplied to the transmission line.

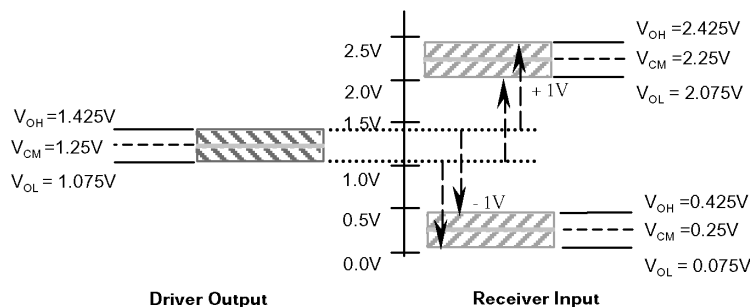


FIGURE 15. Common Mode Operation Range

LVDS (Continued)

Fail-safe Operation

Fail-safe operation is an LVDS feature that helps ensure system reliability by preventing errors. Fail-safe guarantees that the outputs are in a known state (HIGH) when the receiver inputs are under certain fault conditions. Without the fail-safe feature, any external noise above receiver thresholds could trigger the output to an unknown state.

According to the TIA/EIA-644 standard, when the receiver inputs are open, not connected to the driver, or if the driver is powered off, the fail-safe feature will drive the outputs high. Also, if the receiver inputs are shorted, the outputs will be in fail-safe mode.

The standard also states that the receiver outputs will also go into fail-safe if the differential inputs remain within the threshold region for an abnormal period of time. The standard does not specify a time; however, most vendor LVDS receivers will go into fail-safe mode in 1ns or less with open inputs.

The fail-safe protection feature has many benefits for a system designer. For example, some applications may dictate that not all of the LVDS receiver inputs are used. With LVDS, these inputs can be left floating without causing oscillations on the receiver output. With the fail-safe feature, the receiver outputs will always be in a known state anytime that the inputs are not receiving a valid signal.

Termination

Termination of LVDS is necessary at the receiver input to generate the output differential voltage (V_{OD}). This termination resistor is connected between the two differential signal lines. A single resistor is the only termination required for LVDS.

In a point-to-point system configuration, the LVDS termination resistor should be placed within 2 centimeters of the receiver. For a multidrop configuration, the LVDS termination resistor should be located within 2 centimeters of the last receiver.

The TIA/EIA-644 specification stipulates a termination resistor value between 90Ω and 132Ω . Fairchild recommends a termination resistor value between 90Ω and 110Ω , depending on the characteristic impedance of the line.

Termination of LVDS is much simpler than most other technologies. ECL and PECL both use a 220Ω pull-down resistor on each driver output as well as a 100Ω resistor across the driver outputs. GTLP, due to the open-drain configuration, must have a termination resistor matched to the line impedance (usually 50Ω) to a 1.5V pull-up voltage to generate a GTLP signal.

High Data Transfer Rates

LVDS fast propagation speeds and low voltage transitions combine to allow very high data transfer speeds. Typical propagation delays through an LVDS device are 1.4ns. Typical edge rates for LVDS transitions are under 1ns when measured from 10% to 90% of the edge. These fast propagation speeds and low swings provide typical data transfer rate of 400 Mbits/s.

In addition to high speed, the extremely low output swing of 350mV generates minimal noise in the forms of ground bounce, cross-talk, and EMI.

The offset voltage of 1.25V above ground gives LVDS another noise immunity benefit. This voltage offset helps keep the LVDS signal above ground plane noise.

LVDS Point-to-Point Configuration

LVDS drivers and receivers perform optimally when used in systems designed as point-to-point configured systems. The transmission line must be terminated at the receiver with a termination resistor between 90Ω and 132Ω (110Ω is the recommended typical resistor value).

The termination resistor should be placed as close to the receiver inputs as possible. Most twisted-pair cables are designed to 100Ω impedance, to avoid transmission line mismatches a 100Ω termination resistor is recommended. Figure 16 illustrates an LVDS point-to-point configuration.

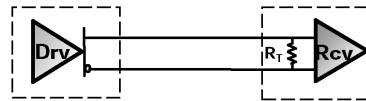


FIGURE 16. LVDS Point-to-Point Configuration

LVDS Multidrop Configuration

LVDS can also be used in a multidrop application. Typically found in backplanes, multidrop configurations are also used in box-to-box applications, provided the media transmission distance is short. In a multidrop system, the termination resistor must be located at the receiver at the far end of the bus. This is illustrated in Figure 17.

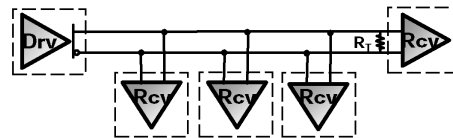


FIGURE 17. LVDS Multidrop Configuration

When flight time from the driver to the receivers is crucial, the system can be designed to drive from the center of the bus. Termination resistors are needed at each end of the bus to prevent reflections. This arrangement is preferred when high frequencies dictate short signal propagation across the transmission line. The termination resistors are seen by the driver as two parallel resistors; therefore, the driver must provide twice the current to drive the bus. Figure 18 illustrates a multidrop configuration with the driver both at the end of the bus and the center of the bus.

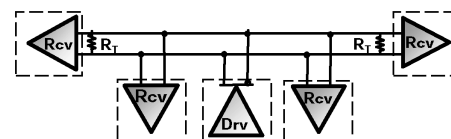


FIGURE 18. LVDS Center-driven Multidrop Configuration

LVDS (Continued)**Multipoint Configuration**

With 3.5mA of dynamic drive standard, LVDS does not have the dynamic current drive to support a multipoint bus application. However, there is also a drive higher than the standard 3.5mA available: high drive LVDS, or MLVDS (multipoint low voltage differential signalling), is specified with 10mA of output drive for operation in multipoint environments.

In a multipoint system, the driver can be located at any point along the bus. For this reason, much like the multi-drop center driven bus previously discussed, a termination resistor is required at each end of the bus. This means that the driver sees the two resistors in parallel and must supply twice the current to the bus. The 10mA dynamic drive is provided on the high drive version of LVDS to address multipoint configurations. Figure 19 illustrates LVDS in a multipoint system.

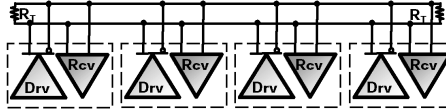


FIGURE 19. LVDS Multipoint Configuration

Summary

Backplane transceiver technologies are designed with specific design parameters in mind. These parameters feature low power consumption or high speed. Some technologies attempt to address each and every backplane issue to offer a complete solution. However, no technology is perfect for

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