

## Section 9- Layout Considerations Backplane Designer's Guide

The best backplane designs allow the components to operate at peak efficiency. Minimizing compromises and enhancing all design parameters enable backplanes to do more with less. To increase efficiency, for example, the I/O technology chosen should allow the backplane to run at maximum frequency. This is achieved by minimizing impedance discontinuities and noise and by carefully matching termination design. The alternative to optimizing I/O technology is selection of higher drive and speed technology and operation at slower than optimum speeds. The first method – choice of the correct I/O technology – reduces overall cost and delivers better signal integrity than the second “brute force” method.

An optimized backplane will use less power, generate little noise, have better signal integrity, and be less costly. For this reason, it is key for the designer to understand how the components interact with each other when laying out a backplane.

### Section Reference

This section addresses layout considerations for a backplane design with primary focus on optimizing the overall design. It discusses:

- Performance
- Trace Layout and Vias
- Clock and Signal Routing
- Skin Effect
- Shielding
- Board Layout
- Board Materials

Section	Section Title	Contents
1	Introduction	Application demands, basic backplane considerations, and how to use this guide.
2	Backplane Protocols	Descriptions of different backplane bus protocols, including PCI- and VME-based protocols.
3	Backplane Architecture	Topics relevant to backplane configuration, including parallel versus serial configuration and different configuration topologies and timing architectures
4	Backplane Design Considerations	Issues relevant to backplane layout, including distributed capacitance, transmission line effect, stub length, termination, and throughput.
5	Backplane Signal Driving and Conditioning	Signal driving and conditioning, including power consumption, rise/fall time, propagation delay, flight time, device drive, pin conditioning, live insertion, and incident wave switching.
6	Noise, Cross-talk, Jitter, Skew and EMI	A review of the enemies of signal integrity and high frequency.
7	Transceiver Technologies	Detailed information about the following technologies: TTL-based (ABT, FCT, and LVT); ECL; and GTLP.
8	Mechanical Considerations	Information about mechanical considerations such as backplane chassis/cages and connectors.
9	Layout Considerations	<b>Physical layout of the receiver and driver cards plugged into the backplane, primarily focusing on construction of the physical layer and the configuration of the devices that comprise the cards.</b>

## Performance Considerations

For best possible backplane performance, designers should consider every characteristic of the backplane. Optimizing key layout parameters, such as the dimensions of the signal traces, placement of the devices, physical layer characteristics, and the amount of noise associated with the driver and receiver cards, will result in a higher level of system performance.

### Design Recommendations

Good layout design includes use of the following basic techniques:

- Use of solid ground and power planes, coupled with multilayer boards
- Minimizing the distance between the layers
- Surrounding PCB with chassis ground trace
- Centrally locating high-frequency clock circuits
- Locating line drivers and receivers close to associated connectors
- Decoupling high-frequency currents locally
- Use of shielded components when applicable
- Use of a line of ferrites for input/output lines
- Use of narrow and buried traces if possible
- Keeping input and output leads away from electromagnetic noise generators
- Making trace impedances uniform
- Matching the impedance of all interfaces on a transmission

## Bandwidth

The bandwidth of a circuit can be thought of as the frequency range in which it will operate properly. The characteristics of circuit layout and components combine to set the bandwidth. If system frequency is increased or its components are changed, circuit operation and bandwidth should be evaluated.

An example would be a new I/O technology with faster edge rates replacing another technology in an existing design. In this case, the circuit could begin to generate excessive noise from reflections if the termination is no longer adequate. Lines that did not exhibit transmission line behavior with slower edge rates, may exhibit transmission line behavior with faster edge rates.

Another potential noise source is cross-talk. Trace spacing that was adequate to prevent signal coupling at slower edges may not be enough with faster edge rates.

As system frequencies and device edge rates increase, the board layout also must be addressed. This concern can be attributed to the limited bandwidth at which traces can operate. To extend the performance of a trace, it is important to understand how the dimensions of the trace affect bandwidth. The bandwidth of almost all transmission lines can be easily calculated.

For PC board applications, the bandwidth is proportional to the square of the trace width (W). For the length, the bandwidth is inversely proportional to the square of the trace length (L).

$$\text{Bandwidth} = W^2$$

$$\text{Bandwidth} = 1/L^2$$

Where:

W = Trace Width

L = Trace Length

## Basic Board Design

Early circuit boards were one layer designs with power and ground traces mixed with signal traces. As system operating frequencies increased, the amount of noise created from signal traces mixing with the power and ground traces started to become a problem. Narrow power and ground traces resulted in a  $V_{CC}$  impedance on the order of 100Ω.

Newer board designs placed ground and power traces on separate layers. The ground traces were placed on the bottom of the board, which became the ground plane; and the power traces were placed on top, which became the power plane. This reduced the impedance of the  $V_{CC}$  plane to about 2Ω or less.

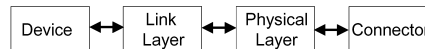
### Board Layout

The layout of a board is critical to design optimization, and this is especially true as system frequencies increase. The number of board layers and the relation of the ground, power, and signal layers to each other all play a role in design optimization. These layout spacing relationships will affect the maximum edge rates and, therefore, maximum frequency as well as the amount of cross-talk in a design.

### Connection Distances

The distance of the I/O device to the backplane connector should be kept to an absolute minimum. The shorter this line length, the better the signal integrity.

Reducing the drive-to-connector line shortens the signal stub length and has several benefits: minimization of transmission line effects, reduction of the impedance of the backplane line by minimizing capacitance and inductance of the stub, and reduction of signal flight time on the stub. The results are better backplane signal integrity from cleaner signals running on the backplane, and higher performance due to less flight time delay on backplane stubs.



**FIGURE 1. Typical device-to-connector connection node, showing the device, link layer (usually solder), physical layer (board traces), and connector**

Figure 1 shows a typical connection node, where distances are kept as short as possible. As system frequencies increase, the adverse effects of discontinuities on signal integrity become more of a problem.

An additional critical layout issue is the connection between the various layers. Every layer interface is a source of potential impedance discontinuity and added capacitance. Therefore, all interface connections must be carefully designed and manufactured for best impedance match and minimum additional capacitance.

## Basic Board Design (Continued)

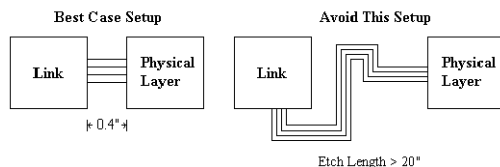
### Trace Length

Signal trace lengths have a direct effect on maximum frequency of a system. Longer trace lengths increase flight time of the signals, limiting the maximum frequency. This is because longer trace lengths will exhibit transmission line characteristics. All transmission lines must be properly terminated to control reflections. If the driver and termination are not matched, receivers that are not at the trace end may require a full signal round trip to recognize a state change. To minimize transmission line effects, trace lengths should be kept to a minimum where possible.

As noted in the section on connection distances, every connection and stub has the potential to introduce discontinuities that disrupt signal integrity. To minimize signal integrity problems, traces, connectors, stubs, and cables should all be impedance-matched. Having a different impedance characteristic can cause reflections that result in signal distortion and reduced throughput. For system trace layout consider the following rules:

- The trace lengths should be kept as short as possible. After a signal has been transmitted, it travels the length of the trace. A reflection travels the equal length back. All this must take place well under the rise time of the signal. If not, the trace can act as a transmission line.
- To minimize the effects of cross-talk, each trace should be spaced as far apart as possible.
- Avoid making 90° trace turns on trace runs. 90° turns increase the effective width of the trace in the turn contributing parasitic capacitance. At very fast edge rates (~100 ps) these discontinuities can cause significant signal integrity problems. 45° corners are recommended instead. If 90° turns are used, round the corners of the turn to reduce the width change through the corner.

Figure 2 illustrates these rules. The best-case setup may be difficult to implement with today's multicomponent designs. The important point is that whenever possible, given design restraints, the designer should try to minimize trace lengths and avoid 90° turns.



**FIGURE 2. Trace Run Comparison, Theoretical “Best-case” and “Worst-case” Layouts**

### Signal Trace Layout

The position of a signal trace relative to the ground or power plane and other traces directly affects maximum frequency and cross-talk. All signal lines have a current return path or paths. The proximity of ground and power planes, as well as other signal traces, will determine where this path is.

A high-speed driver current return path is through the lowest inductance and closest path this current can find. Ideally, this is on an uninterrupted ground plane directly beneath the device and trace. The return current will follow the signal trace and its density will fall off quickly away from this trace.

This return current loop to distance relationship can be approximated with the formula:

$$i(D) = \frac{I_0}{\pi H} \cdot \frac{1}{1 + (D/H)^2}$$

Where:

$I_0$  = Total Current (amperes)

$H$  = Height of Trace above return plane (inches)

$D$  = Perpendicular Distance from return plane (inches)

$i(D)$  = Signal Current Density (ampere/inch)

The low-inductance current return path that is provided by a ground plane, which is close to the device provides several benefits over other return paths. This path minimizes noise disruptions to other circuits caused by widely dispersed currents on ground and power planes, cross-talk, and the effects of the radiated electromagnetic field.

The distance between the traces on a board layer should be greater than the distance between the traces and the ground, or the current return path plane. The minimum distance between signal traces will increase with frequency and edge rate. Keeping this ground-to-signal tracing is critical for minimizing cross-talk.

If it is not possible to keep minimum spacing between signal traces, a grounded guard trace will help minimize cross-talk. The guard trace will minimize coupling between the traces, and it should be connected to the ground plane at both ends. Better shielding performance will be achieved if additional ground vias are connected to the guard trace at intervals along the trace. The longer the guard trace, the more critical this becomes.

Power planes can also be used as a current return path if a ground plane is not available nearby. However, the ground and power planes must be well connected with many bypass capacitors for this to become a low-inductance return path. In this case, the return current will couple onto the power plane and, through the bypass capacitors, be coupled to the ground and back to the driver ground.

For very high-speed board layouts this is not recommended. Voltages induced across the bypass capacitors will generate EMI radiation. At higher frequencies, this EMI radiation can be significant.

### Ground Plane Breaks

Ground planes are sometimes interrupted to insert signal traces, a matrix of vias or other routing that will not fit on other board layers. It is imperative that no signal traces run over a ground plane break.

If a trace is routed over a break in the ground plane, the return current will be forced to flow around the ends of this break. This will significantly raise return path inductance, which will slow the edge rate on the signal path. This will limit maximum frequency and have adverse effects on timing. Additionally, the current flowing around the ground plane break may pass under other traces and induce cross-talk.

## Basic Board Design (Continued)

### Clock Signal Layout

In systems that use clock signals for timing, noise-free clock signals arriving at the correct time are critical for proper system operation. Noisy or mistimed clock signals can corrupt system operation. To protect clock signals from corruption due to noise, particular care should be taken in their layout and shielding.

All techniques used to minimize noise caused by cross-talk, reflections, or ground bounce should be implemented with extra care on clock lines.

Many layout techniques can be implemented to ensure clock integrity in sensitive and high-speed designs. Additional spacing between clock lines and signal traces can prevent cross-talk coupling. If board density does not permit additional spacing, or if additional protection is required, guard traces to shield and isolate clock lines can be used.

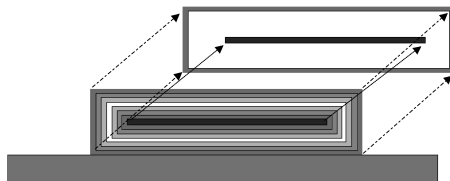
Differential I/O technologies that offer superior noise immunity to single-ended technologies are commonly used to drive clock signals in high-speed applications. Additionally, the low voltage swings, slower edge rates, and termination designs used by differential technologies minimize ground bounce and reflections.

### Skin Effect

As frequency rises, current propagating down a trace or cable will tend to travel more on the outside of the trace, and less down the center. The higher the frequency, the more pronounced the effect. This phenomenon is referred to as "skin effect".

As the current flow pulls away from the center of the conductor, the effective resistance of the conductor increases proportionally. This increase in resistance with an increase in frequency results in attenuation of the signal.

Skin effects are caused by inductive reactance of the trace. As frequency increases, the inductance of the trace also increases. This increase in inductance is seen more at the center of the trace or cable and less toward the outside. This is illustrated by the trace cross section in Figure 3. The center cross-section of a trace has much less area than the outer cross-section, resulting in a higher inductance.



**FIGURE 3. A Cross Section of a Signal Trace**  
The inner sections have less area than the trace surface outer section. The result is a much higher inductance inside the trace than at the surface.

At frequency, currents follow the path of least inductance. As frequency increases, the skin effects become more pronounced, and eventually all current will flow at, or just below, the edges of the trace or cable. This can be shown with the formula:

$$\text{Skin Depth} = \left( \frac{2p}{w\mu} \right)^{1/2}$$

Where:

Skin Depth = Depth of Current Flow

p = Conductor Volume of Resistivity

w = Frequency (in radians/sec.)

μ = Magnetic Permeability of the Conductor

Or:

$$\text{Skin Depth} = \left( \frac{2 \cdot \left( p \frac{\text{volt} \cdot \text{inch}}{\text{amp}} \right)}{\left( \frac{2 \cdot \pi \cdot f}{\text{sec}} \right) \cdot \mu \left( \frac{\text{volt} \cdot \text{sec}}{\text{amp} \cdot \text{inch}} \right)} \right)^{1/2}$$

Skin depth effects are a function of material conductivity. Conductor shape does not have an effect on skin depth effects; however, cross-sectional size does. The critical dimension is the conductor cross-section. For a rectangular conductor, this is one half the thickness. For a round conductor, this is the radius.

Increase in resistance due to skin effect is seen at the frequency where current flow begins to pull away from the center of the conductor. At the frequency where skin depth is less than the thickness of the conductor, the resistance per square inch rises in proportion to the square root of the frequency.

The formula for calculating resistance at skin effect frequencies is:

Where:

$$R_{AC}(f) = \frac{(2.61 \times 10^{-7})(fp_r)^{1/2}}{2(w+d)}$$

Where:

R<sub>AC</sub> = AC Resistance per inch

f = Frequency, Hz

p<sub>R</sub> = Relative Resistivity, compared to copper = 1.00

w = Trace Width, inches

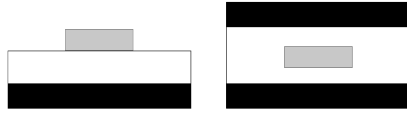
d = Trace Height, inches

Note: for round cross-section conductors, substitute (π x D)

D = Diameter of the wire in place of 2(w+d)

## Microstrip and Stripline Traces

Board layouts typically include two types of signal traces, microstrip and stripline. These trace types are illustrated in Figure 4.



**FIGURE 4. Microstrip trace etched on a board surface layer (left). Stripline ribbon trace embedded into a board dielectric layer (right).**

Microstrip traces are implemented on board surface layers by etching away the unwanted conductive material and leaving the trace run. By ensuring consistent line width, thickness, and distance from the ground plane, line characteristic impedance will also be consistent. The formula for microstrip characteristic impedance ( $Z_0$ ) is:

$$Z_0 = \frac{87}{\sqrt{\epsilon_R + 1.41}} \ln \left( \frac{5.98h}{0.8w + T} \right)$$

Where:

- $\epsilon_R$  = Relative Dielectric Constant of the Board Material
- h = Height of Trace Above the Ground Plane
- w = Trace Width
- T = Trace Thickness

Stripline traces are copper ribbon traces embedded into board dielectric layers during board assembly. Controlling trace width, thickness, distance from the ground plane, and dielectric constant of the board material will ensure consistent trace impedance. The formula for stripline characteristic impedance ( $Z_0$ ) is:

$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \ln \left( \frac{1.9b}{0.8w + T} \right)$$

Where:

- $\epsilon_R$  = Relative Dielectric Constant of the Board Material
- w = Trace Width
- T = Trace Thickness
- b = Separation between Ground Planes

## Coaxial and Twisted-pair Cables

Cables are used if a signal connection must be made between boards. Some systems use cables to route signals on boards. In high-speed system design, coaxial cables and twisted-pair cables are the two types commonly used.

For predictable behavior in high-speed systems, high-quality cabling with consistent impedance values should be selected.

Coaxial cables are constructed of a center conductor surrounded by a dielectric material, then a ground shield covered by an insulating sleeve. Coaxial cable comes in many impedance values and is usually used for routing signals between system racks or between systems.

Twisted-pair cables are two equal-impedance cables twisted around each other with a specific number of turns

per foot or meter. This cable construction, including the conductive material and turns combine to give twisted-pair cables a specific impedance characteristic. This cabling is often used for differential signals because of the close coupling between the two cables.

## Vias

Vias are electrical connections between board layers. The usual construction of a via is a drilled hole between two conductive pads, the walls of the via hole are plated with a conductive material. Vias are used for connecting two signal traces, for access to ground or power planes, or for mounting a through-hole device.

### Via Construction

The most common via construction is from one side of the board to the other side. This through hole via is the least expensive design to manufacture because drilling for through-board vias is done after the board stack is assembled. However, because these types of vias run through all board layers, they take up board space on all layers and can disrupt smooth interior layer trace and bus runs.

Two other via types are used more frequently in order to locate more components in less space. These are the blind via and the buried via, alternatives that take up less board space than the more conventional surface-to-surface designs.

The blind via runs from a surface layer to one or more interior layers. These are more costly than standard vias due to the precision depth drilling required.

Buried vias connect two or more interior board layers but do not connect to a surface layer. These vias must be drilled prior to board assembly, a process that requires extremely tight layout specifications.

### Via Electrical Behavior

Vias have capacitive, inductive, and impedance properties that affect signals routed through or past them. The size of a via and its associated connection pads have a direct effect on these properties.

Vias have a parasitic capacitance that is in direct proportion to via size. This parasitic capacitance can be calculated for via size:

$$C = \frac{1.41 \epsilon_r T D_1}{D_2 - D_1}$$

Where:

- $D_2$  = Diameter of clearance hole in ground plane(s), inches
- $D_1$  = Diameter of pad surrounding via, inches
- T = Thickness of printed circuit board, inches
- $\epsilon_r$  = Relative electric permeability of circuit board material
- C = Parasitic via capacitance, pF

Via capacitance slows rising and falling edges by introducing voltage dips and peaks due to the charging or discharging of this parasitic capacitance. For this reason, capacitance, and, therefore, via size should be as small as available manufacturing technology and costs permit. This is especially important as frequencies increase.

A via has inductance that is in approximate proportion to its length (or height), and, to a lesser degree, the via's

## Vias (Continued)

diameter. This inductance can be approximated using the equation:

$$L = 5.08h \left[ \ln \left( \frac{4h}{d} \right) + 1 \right]$$

Where:

- L = Inductance of the via, nH
- h = Length of via, inches
- d = Diameter of via, inches

By inhibiting current flow, via inductance adversely affects a bypass capacitor's ability to filter noise from power and ground planes. Vias used with bypass and decoupling capacitors should be kept as short as possible to minimize inductance.

Via impedance should match the impedance of the traces it connects as closely as possible to minimize signal reflections and discontinuities.

If a via is not impedance-matched to the signal line, the mismatch will slow the signal edge. Trace vias not used to pass signals will still cause disruptions to the signal edges if an impedance mismatch is present.

As rise time gets faster, especially rise times faster than 1ns, vias will slow the edge rate. This is primarily due to the capacitive component of the via. This edge rate degradation will affect the signals that pass through or go past a via on a signal trace.

As with trace-to-trace spacing, via pad spacing is critical to ensure minimization of cross-talk disruptions. Minimum via pad spacing will vary with the specifications for board material design, frequency, and edge rate.

## Board Layer Stacking

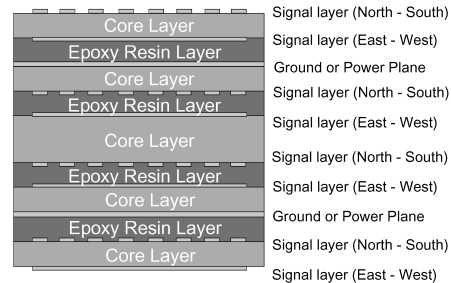
The number of board layers and the positions of the ground, power, and signal layers in relation to each other all have a direct effect on maximum frequency and noise levels.

Multilayer board construction is an assembly process in which a nonconductive core material with a specific dielectric property is bonded with conductive layers that are usually copper. These copper layers are etched to create signal trace layers or are left intact to create ground or power planes.

These core layers are bonded to other layers as necessary, using an epoxy resin of the same dielectric properties as the core material. The process continues until all required layers are bonded to complete the board. In theory, this could be an infinite process; however, cost and, to some degree, mechanical considerations such as board warping limit layer stacking.

### Reducing Noise Coupling and EMI

To reduce unwanted coupling, adjacent trace layers are run at right angles, i.e., east to west on one layer and north to south on the next layer. Minimizing the length that signals run next to each other on adjoining layers limits cross-talk coupling. Ground and power planes can also be used between signal layers to increase signal shielding. Figure 5 illustrates a multilayer board stack up.



**FIGURE 5. Board stack up showing alternating right-angle signal layers and core and epoxy resin layers.**

As system frequencies increase, the layout of the board layers becomes more critical. The faster edge rates of higher frequencies couple more energy onto adjacent traces and power planes and radiate more EMI.

To further reduce noise from cross-talk coupling and EMI, additional ground plane layers are used to provide isolation and shielding. Very high-frequency designs separate each signal layer with a ground plane. These ground plane layers should be connected using multiple vias.

For high-frequency applications, the power plane or planes should be placed next to a ground plane. Use multiple vias and bypass capacitors to connect the two planes. This layout will minimize power plane noise.

## Termination Resistor Parametrics

The purpose of a terminating resistor in a backplane is to minimize unwanted reflections on a transmission line and thereby assure maximum signal integrity. The effectiveness of the termination will depend on how closely the resistance value matches the impedance of the backplane. Additionally, I/O technologies such as GTLP are open drain and require a pull up resistor to operate correctly.

### Determining Resistor Value

To achieve the maximum throughput and signal integrity, the backplane, connector and termination impedance values must all be selected as a system. Termination resistor values typically range from 30Ω to 100Ω as a result of the 50Ω to 65Ω backplane impedance. The resistor value selection should also take into account backplane I/O drive. Simulations should be run to ensure effectiveness.

Small backplanes can utilize a resistor termination at one end, while larger, high-performance systems use terminations at both ends. It is important that doubly terminated systems use a resistor value twice the normal value at each end in order to arrive at the correct overall impedance. (Example: A 100Ω resistor at each end is 50Ω total for  $R_T$ ).

Experience has shown that the impedance of the backplane can vary by a significant amount; therefore, terminating resistors with 1% tolerance should be used to minimize overall error.

## Termination Resistor Parametrics (Continued)

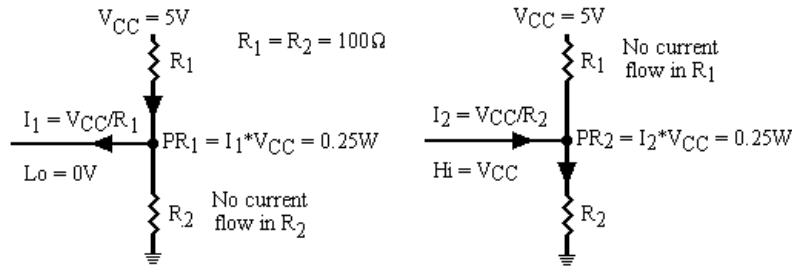
### Power Dissipation in Termination Resistors

Regardless of the application speed, it is essential to determine the worst-case power dissipation for a termination resistor and select that wattage value as minimum.

Although an application may allow for a 50% duty cycle, experience has shown that it is simply not a good idea to select a design with minimal margin. As an example, a power consumption calculation is illustrated below. Each of

the terminating resistors will dissipate a worst-case power of:

Resistors with 1/8 W power ratings will overheat in this particular application at room temperature. Larger 1/4 W resistors may overheat at higher temperatures. Again, it is best to specify an over-sized rather than marginal power rating to ensure stability over worst-case operating conditions and a long stable life.

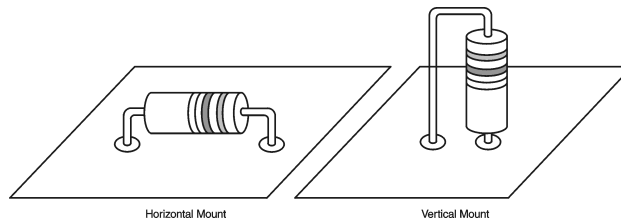


**FIGURE 6. Power Calculation - Worst Case LO or HI Signal**  
 $P_{\text{WORST}} = (5V^2)/100\Omega = 0.25 \text{ W}$

### Mounting

There are two configurations used in mounting single-terminating resistors, the vertical mount and the horizontal mount. As the names imply, the resistor is mounted either

vertically or horizontally to the plane of the circuit board as illustrated in Figure 7.



**FIGURE 7. Mounting Configurations for Single Termination Resistors**

The vertical mount has a lower thermal resistance in still air than the horizontal mount. The horizontal mount has lower inductance characteristics because the leads of the resistor are shorter, and stay low and close to the plane of the circuit board. Choose the resistor mounting that best meets your application requirements.

In addition to discrete resistors, resistor arrays can be found in SIP and DIP type packages. These packages are usually selected to allow for the maximum possible use of circuit board space. Different electrical configurations may be obtained from the manufacturers.

The various resistor pack designs have unique properties that make each better suited to some applications than to others. Resistor arrays that have independent resistor connections on one end and a common connection on the other can be purchased. This may be fine for low-speed applications, but for high-speed environments each resistor should be independent of the others. The mutual inductance between resistors in an array can cause cross-channel disruption. Experience has shown it is best in challenging environments to utilize independent resistors within SIP or DIP package types.

### Parasitic Inductance

Every resistor has some level of series parasitic inductance. Resistor inductance is dependent upon its internal construction, external lead type, and the mounting configuration used.

## Termination Resistor Parametrics (Continued)

The effect of inductance on a digital circuit is a direct function of frequency. Inductance in the wrong place can result in unanticipated adverse effects to circuit behavior and performance. For digital signals it is useful to analyze the inductive nature of the frequency below which most energy in digital pulses concentrate (This is also called the knee frequency). Using the following equation, the inductive reactance magnitude seen by a rising edge can be calculated.

$$|X(t_R)| = (\pi L) / (t_R)$$

Where:

- $t_R$  = Rise Time of Digital Signal, s
- $|X(t_R)|$  = Magnitude of Inductive Reactance as seen by Rising Edge  $t_R$ , s
- $L$  = Inductance, H

Parasitic series inductance can cause mismatches in a termination equivalent to an error in the terminating resistance value. Expressing the magnitude of inductive reactance as a percentage of the terminating resistance value, every 1% of reactance causes 0.5% of reflection. Following this method, if the quantity  $|X(t_R)|$  equals 10% of the terminating resistance value, then the reflection is 5%.

### Typical Series Inductance of Resistors

Resistor Type	Series Inductance (nH)
1/4 - W axial	2.5
1/8 - W axial	1.0
1/8 - W 1206, Surface Mount	0.9

### Sample Calculation

An example of the calculation for the equation above is included. If a 1/4-W axial resistor is used to terminate a signal that has a rise time of 1 ns, then the following will hold.

Signal Rise or Fall Time	1 ns
Transmission Line Impedance	50 W
Inductance of 1/4-W axial	2.5 nH

The inductance magnitude is:

$$|X(t_R)| = \pi(2.5 \text{ nH})/1 \text{ ns} = 7.85$$

If the system is using a split termination of 100W going into 5V  $V_{CC}$  and 100W into ground then the ratio of  $|X(t_R)|/R$  is the following:

$$|X(t_R)|/100 = 7.85\%$$

### RF Termination Resistors

In very high-speed applications, almost 1nH can exist with standard surface mount resistors. Due to this, it may be advantageous to select resistors especially designed for very high-frequency applications. These RF resistors have a minimal inductance, and, in many cases, they can be successfully utilized up to 4GHz and are available through vendors who specialize in this technology.

### Noise Characteristics

System noise is minimized by a layout that limits coupling between signal lines and between the power planes and signal lines. This coupling is seen as cross-talk between signal lines and noise coupling between the supply planes and system signal lines.

Radiated and received EMI is minimized by layout. An EMI-minimized layout includes avoiding antenna loops in circuits, slow signal edge rates when possible, and shielding. These techniques prevent coupling between internal system signals as well as other coupling signals between separate systems.

Careful layout and design can significantly reduce noise levels and, in the process, improve performance. This section discusses layout issues related to noise, including EMI, device placement, and shielding.

### EMI

The importance of the electromagnetic compatibility (EMC) for electronic circuits and systems has led to more stringent requirements for the electrical properties of electronic devices. The EMC of an electronic circuit is primarily determined by how components are laid out with respect to each other and how devices are connected to one another.

In an electronic system, the current flowing in a line generates a current flowing in the return path of the same magnitude. This function creates a circuit that behaves like a loop antenna. The loop antenna will radiate electromagnetic energy with a magnitude determined by the current amplitude, the frequency of the signal, and the configuration of the primary and return lines carrying the current. To reduce loop antenna effects, the length of the lines should be made as short as possible.

Circuit layouts that create loop antennas are also very susceptible to EMI reception. Received EMI radiation can corrupt signals and disrupt system operation. EMI can cause disruption in the system that generates the radiated EMI, or any nearby systems.

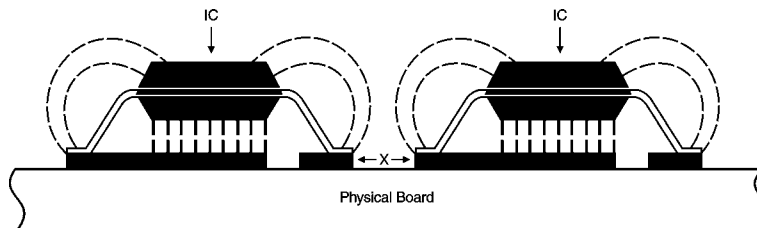
### Device Placement

The amount of EMI generated can also be affected by where devices are placed on a circuit board. Figure 8 shows the area of EMI generated by a device.

Any grounded sections under the IC should be directly connected to the ground pin of the IC if possible. Grounding ensures that the majority of the field lines originating from the IC are concentrated between the IC and the ground level.

In general, driving and receiving devices should be kept close to one another to minimize signal line lengths between devices. However, as shown in Figure 7, if the devices are too close together then the electromagnetic waves of the devices can affect the performance of one another especially with devices that exchange information at high frequencies. Depending on the device, some distance "X" should be maintained to avoid device-to-device generated noise. This distance is dependent upon device technology and system frequency.

## Termination Resistor Parametrics (Continued)



**FIGURE 8. Electromagnetic waves of surface mount IC devices.**  
A minimum distance (X) between high-speed devices is required to prevent interference.

### Shielding

Design layout can greatly reduce EMI. For very high-speed applications where careful layout may not be enough additional internal circuit EMI protection can be achieved with shielding. Shielding is an effective way of reducing EMI. Additional ground plane layers between signal layers on the circuit board will reduce EMI coupling.

Additional shielding can be gained by using the chassis for EMI shielding. Typically, the high-speed circuitry is enclosed in a metal chassis with good earth and system ground connections. In the ideal situation, the chassis completely seals the internal circuitry. Because many shields are not designed to handle significant ground return currents, for safety construct a filter network between the chassis and ground.

### Circuit Board Materials

The circuit board material chosen for the backplane and system has a subtle but significant effect on system operation. This is because the frequency response of the system and overall signal behavior will be affected by the board material. The impact of chosen board material on system behavior increases dramatically above 1GHz.

### Dielectric Constant

The most significant impact board material has on system performance is due to the dielectric constant. A dielectric is thought of as an insulating material, and in high-speed system applications, the dielectric constant,

$$\epsilon_r$$

is a measure of impedance to signal energy propagating through the medium. This impedance-to-signal propagation is often specified as permittivity.

Air has a dielectric constant of 1. The dielectric constant value for other materials increases from 1, depending on the density of the material. Other materials are equated to air by the percent that the material impedes signal velocity. As an example, a material with an  $\epsilon_r$  of 3 has a signal velocity of 58% compared to air.

To calculate this velocity percentage, use reciprocal of the square root of the  $\epsilon_r$ .

$$\begin{aligned} \epsilon_r &= 3 \\ \% \text{ signal velocity compared to air} &= 1/[\text{SQRT}(3)] \\ &= 0.577 = \%58 \end{aligned}$$

The dielectric constant becomes a significant concern above 1 GHz. As system frequency requirements increase, board material with lower dielectric constants should be used. As the dielectric constant value is decreased, signal attenuation decreases and results in narrower traces for the same impedance value and shorter transmission line lengths.

### Dielectric Loss

As the board material absorbs energy from the signals passing over and through it, the material begins to generate heat. This heat is dissipated from the board to the surrounding atmosphere. The generation and dissipation of heat is a transfer of signal energy to heat in the board and then heat to the atmosphere and represents a loss to the system in the form of signal attenuation. This attenuation is referred to as dielectric loss or dissipation factor ( $\text{Tan}\delta$ ), and is a ratio of energy dissipated to energy stored.

$$\begin{aligned} \text{Tan}\delta &= \text{Energy Dissipated/Energy Stored} \\ &= \text{Loss(resistance)/Conductivity} \end{aligned}$$

The dissipation factor varies with material type. Dissipation factor also changes across frequency and is not linear across frequency. For a  $\text{Tan}\delta$  number to be meaningful, it should include a corresponding frequency or be graphed across frequency.

As with dielectric constant effects, dielectric loss effects only become significant above 1GHz for board material. However, dielectric loss can also be a problem over long cable lines at significantly lower frequencies. In either case, careful choice of materials with low dielectric loss is critical to avoid signal attenuation.

## Simulations

There are two methods used to design a high-speed backplane: Designers can build the board based on component specifications and their own design expertise and hope it works, or they can simulate the design before assembling a prototype, and, if it is performed correctly, eliminate all, or at least many, of the bugs before the creation of a physical prototype.

The simulation path is critical when time and money restrictions are present. Although there are many derivatives and some proprietary modeling software platforms available, two types are most widely used: SPICE and IBIS.

### SPICE

The Simulation Program with Integrated Circuit Emphasis (SPICE) tool was developed at the University of California Berkeley. It was the first and still is the most widely used circuit-modeling software available, especially in semiconductor design because it generates a substantial amount of device and circuit information.

Many software companies have made additions and improvements to the original software, namely, SPICE2, SPICE3, HSPICE, and PSPICE. Of the available versions, HSPICE is the most widely used, incorporates more features than the other versions, and has become the version of choice for most semiconductor manufactures.

### Creating SPICE Models

SPICE device models are normally created by semiconductor manufactures during the design of a product. Vendors use SPICE models to verify the design prior to manufacture.

With the increase in model use by semiconductor customers, many vendors have generated models of older, popular products. This is an involved task that requires converting or encoding design data into HSPICE format, but SPICE can accurately simulate nearly any complex system circuit.

### SPICE Model Types

SPICE device models can be obtained from most semiconductor vendors. However, these models contain proprietary device information. For this reason, most vendors require a Non-Disclosure Agreement for newer designs, or they supply models with all internal device nodes encrypted.

Vendor-supplied device SPICE models come in three types: full device models, device slice, and I/O structure. As the names imply, these models contain different amounts of device data.

The full model contains all circuit information in the device. This is the model used by the device designer to verify a design. This model, combined with others in a full circuit, can require a significant amount of system and time overhead because all internal nodes on every device model will be simulated during a run. Device slice and SPICE I/O give the customer most of the functionality of the full model, but minimize simulation overhead.

A device slice is one section of a device from input to output. For example, a slice of a 16-bit driver with one output enable control would contain just one driver circuit from input to output with the output enable. The slice will accurately model driver behavior; however, some internal circuits may be abbreviated to make the slice function.

A SPICE I/O model contains just the input and output stages of a device. This model will accurately simulate device behavior, but not internal propagation delays.

Often a SPICE I/O and slice are combined to give the customer an easy-to-use model with minimum simulation overhead.

### Advantages of SPICE

SPICE model simulations provide the system designer a large amount of circuit analysis data, including DC and AC circuit parameters and behavior. Simulation results can also include timing information.

SPICE is a powerful and accurate simulation tool that is readily available. Many platforms run SPICE, and, in most cases, models are easily convertible between platforms. SPICE is widely used as the starting point for IBIS models, known as SPICE-to-IBIS conversion.

### SPICE Limitations

The same features that make SPICE simulations such a powerful and accurate tool can also be a hindrance. The features of SPICE, and the way the software runs, can result in longer run times and create a significant amount of system and time overhead. It is not uncommon for a SPICE simulation to run for over 12 hours, and, for very complex circuits, over 24 hours is not out of the question. And, if the circuit is large and complex and measurement steps selected are small, the simulation may not run at all because of the many complex computations taking place.

### IBIS

The Input/Output Buffer Information Specification (IBIS) is a device-modeling standard developed in 1993 by a group of companies in the electronic design industry. IBIS allows the development of device models that preserve the proprietary nature of IC chip designs, while at the same time providing information-rich models for signal integrity and EMC analysis. Currently, IBIS is organized and maintained by the IBIS Open Forum, which includes several semiconductor manufacturers, computer companies, and universities.

### Creating IBIS Models

IBIS models are created using two different methods. The first method employs a SPICE conversion. A SPICE-to-IBIS translator uses simulation data to create IBIS current/voltage or voltage/time data. This particular method is primarily done for new I/O device designs and is intended to give the customer a pre-silicon model of a device. The second method uses bench measurement techniques. An automated DC bench is used to collect current and voltage characteristics. This particular technique can be very time consuming.

### Golden Parser

The Golden Parser is a program that checks to see if a file meets the guidelines that have been set for IBIS models. The program checks the structure and syntax of the IBIS model as well as the validity of the data contained therein.

Once the model has passed the Golden Parser program, any simulator supporting the IBIS specification can read the voltage/current data in the file and convert the data to internal simulator modeling format. The Golden Parser can be downloaded from the IBIS Web site and supports many different types of operating systems.

## Simulations (Continued)

IBIS simulations generate data for a specified output loading. This loading is defined by the IBIS model input data. IBIS simulations run 10 to 100 times faster than equivalent SPICE simulations and allow the following key areas to be analyzed by simulation:

- Cross-talk, overshoot/undershoot, ringing
- Impedance mismatches, reflections
- Line terminations
- Layout configurations
- Board level simulation

### Advantages of IBIS

Semiconductor manufacturers create IBIS models to provide modeling support to their customers without disclosing important process/design parameters of a device. With the IBIS model a device's input/output buffer characteristics can be provided accurately to the customer without the manufacturer giving up its intellectual property. For this reason, several semiconductor manufacturers have increased the number of IBIS models available.

Another advantage obtained by using IBIS is that the user can perform signal integrity analysis on design issues such as reflection, cross-talk, and impedance mismatches. The analysis is performed in significantly less time using IBIS models rather than SPICE software. With board designs increasing in complexity, the behavioral modeling of IBIS becomes superior to the structural modeling of HSPICE.

### Summary of Features

IBIS models can perform the following:

- Represent the DC voltage and current characteristics of a device input and output structures and provide multiple pin models
- Allow the user to do transmission line and signal integrity analysis
- Include package information on all signal, control, power, and ground pins
- Create models from empirical bench data or SPICE simulation results

IBIS models cannot provide the following:

- Details about the device design, layout, or process information
- The logic functionality of a device
- AC characteristics such as propagation delays

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## Summary

Backplane design optimization saves costs and complexity and results in a system that performs better, is quieter, and uses less power.

To achieve system optimization, all components must work in harmony and be designed as part of the entire system. Furthermore, all system and layout parameters as well as the interaction of each component with all others must be well understood.

This is a large and complex undertaking, but, fortunately, information and tools are available. Simulation tools can significantly reduce development cycle time. Simulation tools allow experimentation and fine-tuning in relatively short time periods and at much lower cost than trial-and-error assembly methods.