



Date Created: 2/24/2004
Date Issued: 3/3/2004
PCN # 20040803

DESIGN/PROCESS CHANGE NOTIFICATION -- FINAL

Notification of this change was initially distributed via Forecast Change Notice #20031701, issued 5/20/2003. This PCN covers US8 products identified in 20031701. Additional PCNs have been or will be issued for the other products listed in the FCN.

This is to inform you that a design and/or process change will be made to the following product(s). This notification is for your information and concurrence.

If you require data or samples to qualify this change, please contact **Fairchild Semiconductor within 30 days of receipt of this notification.**

If you have any questions concerning this change, please contact:

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PCN Type: Alternate Fab Location

Effectivity

Expected 1st Device Shipment Date: 4/5/2004
Earliest Year/Work Week of Changed Product: 0415
(Note: Package marking may differ from this format)

Product ID (Description):

This notification affects Fairchild's TinyLogic, US8 packaged, ULP and ULP-A products, assembled at Hana Semiconductor, Thailand. Please see the attached product list for specific products.

Description of Change:

Fairchild is announcing the qualification of its South Portland, Maine, FS35 Fab Process to produce 0.35 um products. Prior to this qualification, Fairchild's 0.35 um products were fabricated exclusively at TSMC, Taiwan.

Fairchild's 0.35 um fabrication process is equivalent to the TSMC's 0.35 um process. Material produced in South Portland is interchangeable with material produced at TSMC. Fairchild product will now be fabricated at both sites. There will be no package top mark or other distinguishing feature denoting which fabrication facility the material came from.

Effect of Change:

All package dimensions, product performance, and production test specifications will remain unchanged. Material fabricated in the South Portland facility meets the same quality and reliability standards as TSMC fabricated material.

Qualification:

Full Rel Qualification stresses testing for Fairchild's FS35 fab process has been completed. All reliability stresses outlined in the reliability qualification plan were successfully met.

Qual/REL Plan Numbers

Additional Qualification Data

Results/Discussion:

Environmental Results:

Test: MSL (1), PKG(Small), Peak-Temp (260c), Cycles(3) (Precondition)				
Lot	Device	Precon Results		Failure Code
Q20030059AAPCNL1A	NC7WV125K8X	0/320		-
Q20030059ABPCNL1A	NC7WV125K8X	0/320		-
Q20030059ACPCNL1A	NC7WV125K8X	0/320		-

Test: (Autoclave)				
Lot	Device	96-HOURS Results		Failure Code
Q20030059AAACL	NC7WV125K8X	0 / 77		
Q20030059ABACL	NC7WV125K8X	0 / 77		
Q20030059ACACL	NC7WV125K8X	0 / 77		

Test: (High Temperature Storage Life)				
Lot	Device	168-HOURS Results	1000-HOURS Results	Failure Code
Q20030059AAHTSL	NC7WV125K8X	0 / 77	0 / 77	-
Q20030059ABHTSL	NC7WV125K8X	0 / 77	0 / 77	-
Q20030059ACHTSL	NC7WV125K8X	0 / 77	0 / 77	-

Test: (Highly Accelerated Stress Test)				
Lot	Device	96-HOURS Results		Failure Code
Q20030059AAHAST1	NC7WV125K8X	0 / 45		-
Q20030059ABHAST1	NC7WV125K8X	0 / 45		-
Q20030059ACHAST1	NC7WV125K8X	0 / 45		-

Test: (Static Op Life)				
Lot	Device	168-HOURS Results	1000-HOURS Results	Failure Code
Q20030059AASOPL1	NC7WV125K8X	0 / 77	0 / 77	-
Q20030059ABSOP1	NC7WV125K8X	0 / 77	0 / 77	-
Q20030059ACSOPL1	NC7WV125K8X	0 / 77	0 / 77	-

Test: (Temperature Cycle)				
Lot	Device	500-CYCLES Results		Failure Code
Q20030059AATMCL1	NC7WV125K8X	0 / 77		-
Q20030059ABTMCL1	NC7WV125K8X	0 / 77		-
Q20030059ACTMCL1	NC7WV125K8X	0 / 77		-

Test: (Gate Leakage): + 400 Volts				
Lot	Device	+ 400 V		Failure Code

Q20030059AAGATE	NC7WV125K8X	0/3		-
Q20030059ABGATE	NC7WV125K8X	0/3		-
Q20030059ACGATE	NC7WV125K8X	0/3		-

Test: (Gate Leakage): - 400 volts				
Lot	Device	- 400 V		Failure Code
Q20030059AAGATE	NC7WV125K8X	0/3		-
Q20030059ABGATE	NC7WV125K8X	0/3		-
Q20030059ACGATE	NC7WV125K8X	0/3		-

Mechanical Results:

Test: (Bond Pull)			
Lot	Device		Failure Code
Q20030059AABPULL	NC7WV125K8X	0 / 45	-
Q20030059ABBPULL	NC7WV125K8X	0 / 45	-
Q20030059ACBPULL	NC7WV125K8X	0 / 45	-
Test: (Bond Shear)			
Lot	Device		Failure Code
Q20030059AABSHR	NC7WV125K8X	0 / 45	-
Q20030059ABBSHR	NC7WV125K8X	0 / 45	-
Q20030059ACBSHR	NC7WV125K8X	0 / 45	-
Test: (Die Shear)			
Lot	Device		Failure Code
Q20030059AADSHR	NC7WV125K8X	0 / 5	-
Q20030059ABDSHR	NC7WV125K8X	0 / 5	-
Q20030059ACDSHR	NC7WV125K8X	0 / 5	-
Test: As Received; Die Surface, Die Attach, Lead-Frame Front, Lead-frame Back (C Scanning Acoustical Microscope)			
Lot	Device		Failure Code
Q20030059AACSAM1	NC7WV125K8X	0 / 10	
Q20030059ABCSAM1	NC7WV125K8X	0 / 10	
Q20030059ACCSAM1	NC7WV125K8X	0 / 10	
Test: Post Precondition; Die surface, Die Attach, Lead-frame Front, Lead-frame Back (C Scanning Acoustical Microscope)			
Lot	Device		Failure Code
Q20030059AACSAM2	NC7WV125K8X	0 / 10	
Q20030059ABCSAM2	NC7WV125K8X	0 / 10	
Q20030059ACCSAM2	NC7WV125K8X	0 / 10	
In accordance with JEDEC Standard J-STD-20B the impact of de-lamination was evaluated with passing results based on the performance of the other stress tests outlined in this reliability report, as a result this part is determined to be MSL-1 @ 260C.			

Conclusion

All reliability stresses outlined in the reliability qualification plan Q20030059 were successfully met, and unconditionally qualify for production the FS35C core CMOS process for assembly in the Hana assembled US8 package.

Affected FSIDs

NC7NP14K8X
 NC7SV74K8X
 NC7WP240K8X
 NC7WV125K8X

NC7NP34K8X
 NC7WP00K8X
 NC7WP32K8X

NC7SP74K8X
 NC7WP08K8X
 NC7WP86K8X