



Date Created: 4/30/2004
Date Issued: 5/10/2004
PCN # 20041803

FORECAST CHANGE NOTIFICATION

This is to inform you that a design and/or process change will be made to the following product(s). This notification is for your information and concurrence. This is a preliminary notification. A final PCN will be issued when qualification is complete and data is available.

If you require data or samples to qualify this change, please contact **Fairchild Semiconductor within 30 days of receipt of this notification.**

If you have any questions concerning this change, please contact:

Name: Wong, Martin
E-Mail: Martin.Wong@notes.fairchildsemi.com
Phone: 408-822-2635

PCN Originator

Name: Wong, Martin
E-mail: Martin.Wong@notes.fairchildsemi.com
Phone: 408-822-2635

REL Engineer

Name: Jose, Maggie
E-mail: Maggie.Jose@notes.fairchildsemi.com
Phone: 1-408-822-2329

PCN Type: Die Shrink

Effectivity

Expected 1st Device Shipment Date: 11/1/2004
Earliest Year/Work Week of Changed Product: 0445
(Note: Package marking may differ from this format)

Product ID (Description):

This notification applies to the FAN5009 and FAN5009A products. They are Dual Bootstrapped 12V MOSFET Drivers. See below for a detailed list of affected FSIDs.

Description of Change:

The FAN5009 and FAN5009A are fabricated with BICMOS CS80CBIH30V process at FCS South Portland, Maine. The die has been redesigned to a more competitive DMOS FS35CDMOS12_2LM process at FCS South Portland, Maine. The result is a significantly smaller die size.

The products manufactured with CS80CBIH30V die are identified by the product ID FAN5009 and FAN5009A while the products manufactured with FS35CDMOS12_2LM die is identified by product ID FAN5009C.

Effect of Change:

The FAN5009C die manufactured with the FS35CDMOS12_2LM process has no effect on the performance of the FAN5009/FAN5009A in the intended application. The specifications in the current data sheet are not changed.

Both die versions will ship interchangeably until inventory of the CS80CBIH30V wafers is depleted.

Qualification:

See Qual plan Q20040032A.

Qual/REL Plan Numbers

Additional Qualification Data



**RELIABILITY
QUALIFICATION PLAN**

Q20040032A

Project Charter

Project Title: FS35CDMOS12_2LM New Process Qual

<p>Purpose of the Qualification: The purpose of this procedure is to qualify the FS35 fab process at Fairchild's fab in South Portland, Maine. The device used will be a FAN5009C, which was previously qualified in the CS80 fab process at South Portland. The devices will be assembled into a 8 lead narrow SOIC package at fairchild's facility in Penang, Malaysia.</p>	<p>Author: Glen Marcus Requestor: Martin Wong Project Category: New Fabrication Process Reliability Lab Location: Penang Test Location: San Jose Date: Feb 27, 2004</p>
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Project Scope:

Release Criteria:
Three diffusion lots and three assembly lots are required by FSC-QAR-0006.
Required environmental stresses:

- ACLV
- DOPL/SOPL
- HTSL
- THBT/HAST
- TMCL

ALR Required on all lots:
Wire Pull
Ball Shear
Die Shear

Production release after successful completion of environmental stresses. Additionally, the device must adhere to Fairchild's ESD standards.

Zero failures are allowable for this qual. Failure analysis reports will be generated and corrective actions will be taken in case of any failure occurs.

Additional Information:

Related Qualification Plans:

Signatures:

Author:	Date:
Requestor:	Date:
Approver:	Date:



**RELIABILITY
QUALIFICATION PLAN**

Q20040032A

Qualification Device Detail

Device A:	FAN5009CM
Package:	NMSON
# Leads:	008

Process of Record:

Fabrication Process Flow: New - Not Yet Qualified
Fabrication Site/Fabrication Area: ME - Nsme, S. Portland, Maine (Nsc)
Assembly Site: PENANG
Assembly Package: NMSON008 - 008, PLASTIC MOLDED, SOIC-8 PKG, NARROW BODY, SMD (S1)
Assembly Build Diagram: FAN5009CM
Comments: New Fab process - FS35CDMOS12_2LM

Subgroup A Precondition Description: - PCNL1A: MSL(1), PKG(Small), PeakTemp(260c), Cycles(3)

#	Stress Type	Condition Description	Value	Measurement Units
1	TMCL1	Duration	5	CYCLES
		Low Temperature	-65	C
		High Temperature	150	C
2	VIS	Duration		
		High Temperature	125	C
3	BAKE	Duration	24	HOURS
		High Temperature	168	C
4	MOIS	Duration	168	HOURS
		High Temperature	85	C
		Relative Humidity	85	%RH
5	REFL2	Duration		
		High Temperature	260	C
6	FLUX	Duration		
7	RINSE	Duration		
8	DRY	Duration		

Subgroup Descriptions:

SUBGROUP	UNIQUE IDENTIFIER DESCRIPTION
A	Qual Lot A
B	Qual Lot B
C	Qual Lot C

Subgroup POR Detail:

	A	B	C
Die Revision	Step A Rev A	Step A Rev A	Step A Rev A
Die Size	1020 x 1450 MC	1020 x 1450 MC	1020 x 1450 MC
Fab Lot Number			
Fab Location	ME	ME	ME
Assy Lot Number			
Wafer Number			
Assy Location	FSC Penang	FSC Penang	FSC Penang
Subgroup Comments			



**RELIABILITY
QUALIFICATION PLAN**

Q20040032A

Qualification Stress Test and Sample Size Detail

Device A:	FAN5009CM
Package:	NMSON
# Leads:	008

Environmental Stress Detail:

Stress	P/C	Standard	Conditions	Readpoints			Sample		
				TP1	TP2	TP3	A	B	C
ACLV	X		100%RH, 121C	96			77	77	77
DOPL			125C, 0V	168	500	1000	77	77	77
HAST1	X		85%RH, 130C, 0V	96			45	45	45
HTSL			150C	168	500	1000	77	77	77
TMCL1	X		-65C, 150C	100	500		77	77	77

Electrical Stress Detail:

Stress	P/C	Standard	Conditions	Readpoints	Sample		
				TP1	A	B	C
CDM			1000V,	1	3		
HBM			2000V,	1	3		
LU			.3amps,	1	3		
MM			200V,	1	3		

WLR/ALR Stress Detail:

Stress	P/C	Standard	Conditions	Readpoints	Sample		
				TP1	A	B	C
BPULL				1	5	5	5
BSHR				1	5	5	5
DSHR				1	5	5	5

Affected FSIDs

FAN5009AM
FAN5009MPX

FAN5009AMX
FAN5009MX

FAN5009M