High Performance Backplane Architecture

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DesignCon2000
High-Performance System Design Conference

Abstract

Before changing your backplane transceiver technology to more expensive components in order to increase performance consider choosing a different way of designing your backplane to improve data throughput while simplifying backplane design. The synchronous clock architecture is today's most prevalent architecture, utilizing a zero-nanosecond-skew distributed clock. This approach is commonly used because it fits most synchronous systems and is a direct mapping of a typical synchronous architecture. However, there are other ways of associating the data across a backplane with a reference clock that can offer improved performance levels. By changing your backplane architecture slightly, speed advantages can be gained without incurring the additional cost of higher performance devices.

This paper will discuss the basic synchronous architectural approach and then present an analysis to demonstrate how to achieve higher performance levels (higher throughputs) from this common backplane architecture. Performance levels of over 100MHz in a multi-drop, synchronous backplane architecture will be discussed and demonstrated using readily available components.

Author/Speaker

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Current Activities

Lee has been with Fairchild Semiconductor for 10 years. He is currently a Senior Engineer in the Applications Engineering Department and has held this position for the last 2 years.

Background

Previous to his current assignment, Lee was a hardware / verification engineer for PCMCIA and Cardbus products writing test bench code and designing prototype hardware for a Cardbus Host Controller. In addition to the Cardbus activity, Lee co-designed the industry's first simultaneous-operation combo LAN+Modem PCMCIA card. Lee has a BS degree in Electrical Engineering from the University of Connecticut.

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INTRODUCTION:

Slide #1

High Performance Backplane Architecture

DesignCon 2000
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This paper will discuss the basic synchronous architectural approach and then present an analysis to demonstrate how to achieve higher performance levels (higher throughputs) from a source-synchronous architecture. Performance levels of over 100MHz in a multi-drop, source-synchronous backplane architecture will be discussed and demonstrated using readily available bus interface components.

Slide 2: Traditional Synchronous Interface

Traditional Synchronous Interface

- Limited by physical topology
- Requires clock skew control across entire system
- Interface works in “absolute” time
- Uses buswidth to increase system bandwidth

System performance goals are in a constant march towards higher and higher levels of throughput and bandwidth. This progression is forcing designers to leave the comfort of traditional synchronous interfaces behind. The main reason for the performance limitation of traditional synchronous design is purely physical. This interface works in “absolute” time. All agents in a synchronous interface take marching orders from a dedicated clock source distributed via equal length traces to minimize skew across the system.

Current levels of integration and IC process capability have significantly reduced the timing delays associated with interface IC’s and skew from clock drivers. However, the transport delay cannot be eliminated or ignored, it just takes time to move signals from one agent to another. Since the transport delay or flight time of a signal limits the system’s frequency of operation, designers have resorted to larger buswidths to gain overall system bandwidth requirements. Beyond a certain point, the pain associated with larger and larger buswidths overshadows the performance gained and alternative solutions must be considered.

Slide #3: Source-Synchronous Interface

Source-Synchronous Interface

- Not flight time limited
- Eases system clock skew requirements
- Interface works in “relative” time
- Uses I/O frequency to increase system bandwidth

A Source-Synchronous system can be defined as a system using a strobe or clock signal generated by the address/data signal source to latch or clock the address/data signals at the receiving agent. Using a self-timed strobe at the receiver eliminates the flight time variable from system timing equations. Eliminating flight time allows the designer to maximize the potential bandwidth of any interface technology by increasing the frequency of operation. Because interface signal timing is now working in “relative” time the global skew requirements of a system clock have likely been reduced.

Slide #4: Traditional Synchronous Interface

Traditional Synchronous Interface

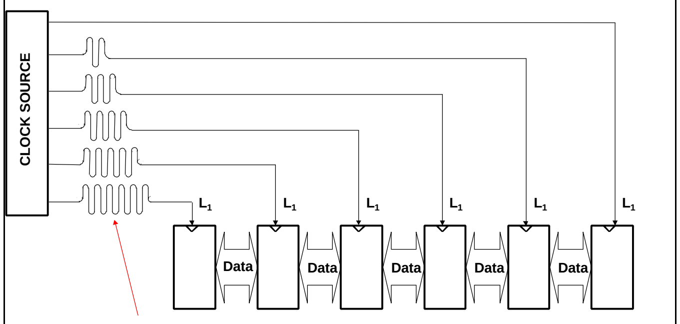
- Clock distribution and routing
- Data / Address routing
- Likely solutions
- Visual timing analysis (Setup)
- Visual timing analysis (Hold)
- Tabular results

SYNCHRONOUS INTERFACE

By studying a traditional synchronous design we can establish a baseline performance level for a given interface. Our study will include clock distribution, signal routing, a typical solution. The solution results will be shown in a graphical or visual form to better understand all the variables and the degree to which they effect overall system timing and performance.

Slide #5: Typical Clock Distribution

Typical Clock Distribution

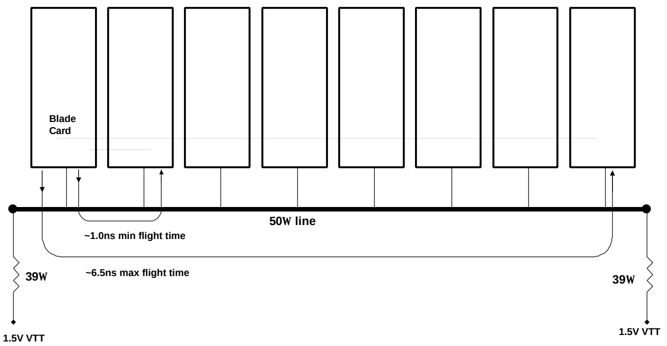


A Centrally located Clock Source will use matched trace delay (line length) to generate clock edges which arrive at all synchronous elements or cards at the exact same instant in time.

A centrally located clock source will use matched trace delay to generate and distribute multiple clock signals. Ideally these signals will arrive at all synchronous elements or card edges at the same instant in time. In most systems an additional level of clock distribution will be undertaken at the card level. This 2nd level of clock distribution is often handled by some form of Phase Locked Loop (PLL). In this way all cards, independent of on-card clock requirements, will present an equal load to the central clock source eliminating one source of clock skew.

Slide #6: Data Routing

Data Routing

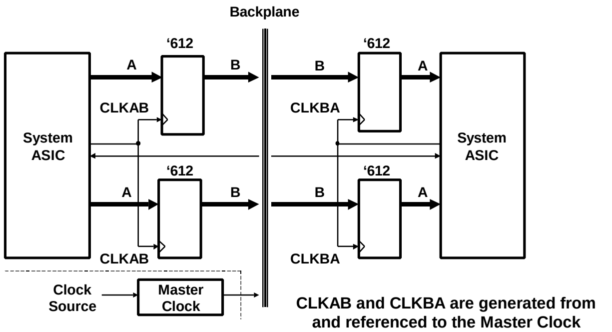


Unlike the clock lines, data, address, and control signals are typically routed in a multidrop or daisychain arrangement. This topology allows for varied card to card routing delays based on the relative card positions. In an unterminated backplane design like Compact PCI (cPCI) the designer will need to account for an additional "settling time" equal to the maximum flight time of the interface.

In an effort to improve the signal integrity and performance of multidrop interfaces like VME an alternative routing structure may be employed. This structure is commonly reffered to as a star configuration. The star configuration routes signals in such a manner as to equalize the delays of any card to card transmission. Routing signals in this manner also serves to improve the switching behavior of traditional I/O drivers because the interface now looks and behaves more like a lumped capacitive load.

Slide #7: Likely Solution using the GTLP16612

Likely Solution using GTLP '612

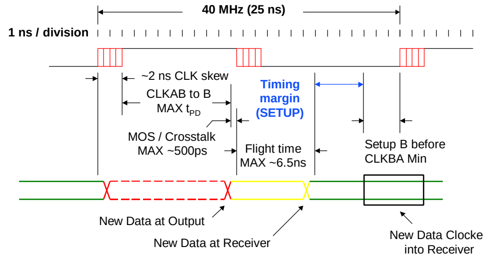


CLKAB and CLKBA are generated from and referenced to the Master Clock

While it would be possible to produce higher system speeds using PECL or LVDS technology, the GTLP family makes for a nice case study since traditional and source synchronous products are available.

Slide #8: Visual Timing Analysis

Visual Timing Analysis



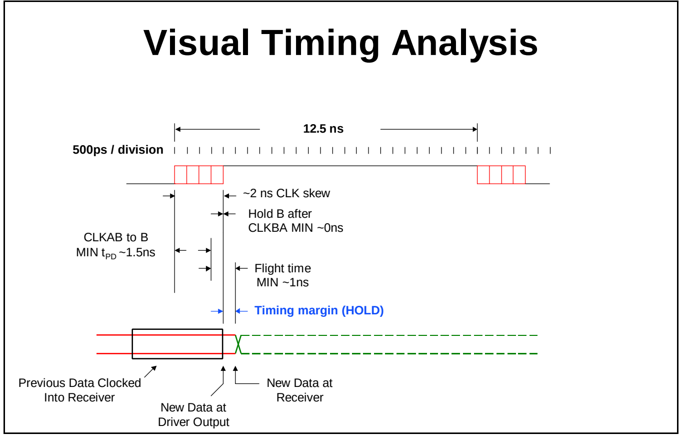
In order to complete the analysis we'll need to choose some values for max clock skew, min and max flight time, crosstalk, and multiple output switching (MOS) events. The numbers shown do not necessarily represent state of the art, but are reasonable placeholders with which to do this type of study.

Robust design techniques, traditional or source synchronous, demand the designer work all potential system variables to their extreme values. By pushing and stretching the design variables a 3D space is created that defines the solution boundaries. For example, the SETUP margin calculation includes the following variables.

1. Maximum Clock Skew
2. Maximum Interface IC Propagation Delay
3. Maximum MOS and Crosstalk Signal Effects
4. Maximum Card to Card Flight Time
5. Minimum Interface IC Setup Time

Using the worst case numbers will define the maximum possible datarate for this particular system. Changing any of the variables changes the system constraints and therefore the maximum datarate.

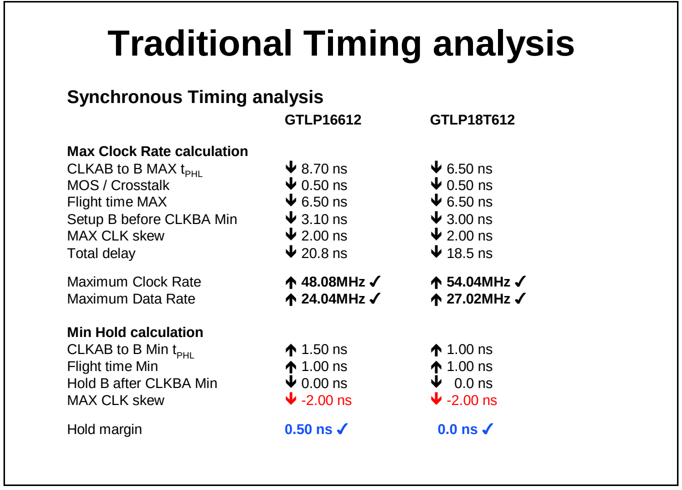
Slide #9: Visual Timing Analysis



Visual Timing Analysis

In contrast to the SETUP calculation, the HOLD calculation is independent of datarate. In the SETUP analysis all the variables were stretched to datasheet maximums, now they are compressed, allowing IC transitions and data flight times to occur as soon as physically possible. One particular point to notice with clock skew, in HOLD time calculations clock skew is subtracted from IC delay and flight time, in SETUP time calculations clock skew is added to IC delay and flight time.

Slide #10: Traditional Timing Analysis



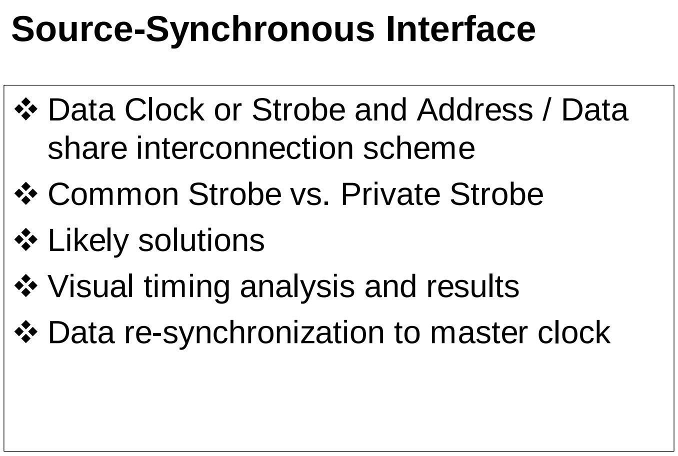
Traditional Timing analysis

Synchronous Timing analysis

	GTLP16612	GTLP18T612
Max Clock Rate calculation		
CLKAB to B MAX t_{PHL}	↓ 8.70 ns	↓ 6.50 ns
MOS / Crosstalk	↓ 0.50 ns	↓ 0.50 ns
Flight time MAX	↓ 6.50 ns	↓ 6.50 ns
Setup B before CLKBA Min	↓ 3.10 ns	↓ 3.00 ns
MAX CLK skew	↓ 2.00 ns	↓ 2.00 ns
Total delay	↓ 20.8 ns	↓ 18.5 ns
Maximum Clock Rate	↑ **48.08MHz ✓**	↑ **54.04MHz ✓**
Maximum Data Rate	↑ **24.04MHz ✓**	↑ **27.02MHz ✓**
Min Hold calculation		
CLKAB to B Min t_{PHL}	↑ 1.50 ns	↑ 1.00 ns
Flight time Min	↑ 1.00 ns	↑ 1.00 ns
Hold B after CLKBA Min	↓ 0.00 ns	↓ 0.0 ns
MAX CLK skew	↓ -2.00 ns	↓ -2.00 ns
Hold margin	**0.50 ns ✓**	**0.0 ns ✓**

Putting the results into tabular form and reducing the SETUP margin to zero nets a maximum datarate of 27MHz with the GTLP Interface IC. These results have been extracted from a spreadsheet where they can be manipulated to perform "What if?" analyses on any of the system parameters.

Slide #11: Source-Synchronous Interface



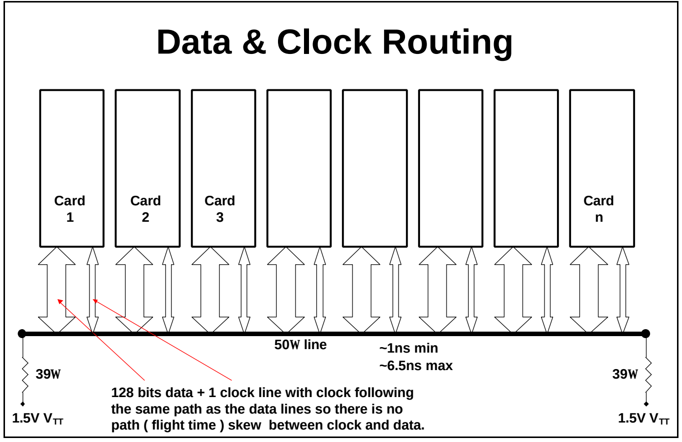
Source-Synchronous Interface

- Data Clock or Strobe and Address / Data share interconnection scheme
- Common Strobe vs. Private Strobe
- Likely solutions
- Visual timing analysis and results
- Data re-synchronization to master clock

SOURCE-SYNCHRONOUS INTERFACE

Moving from the traditional synchronous design to the source synchronous design by swapping components and leaving the physical interface intact allows for a direct architecture comparison. As with the traditional design, our study will include signal and clock routing, possible architecture variations, and representative solutions. The solution results will be shown in a graphical or visual form to better understand all the variables and the degree to which they effect overall system timing and performance.

Slide #12: Data and Clock Routing

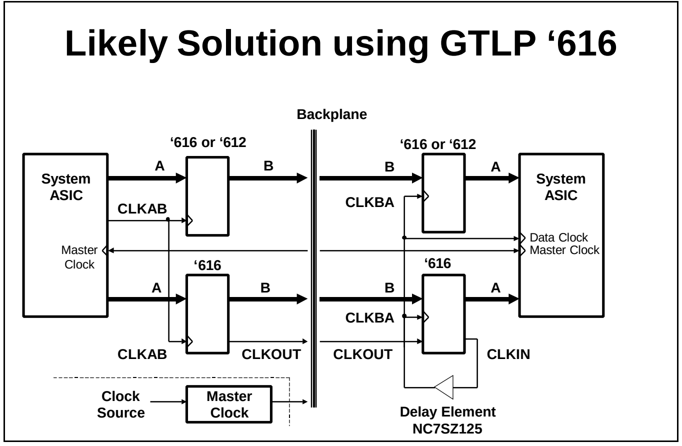


Data & Clock Routing

128 bits data + 1 clock line with clock following the same path as the data lines so there is no path (flight time) skew between clock and data.

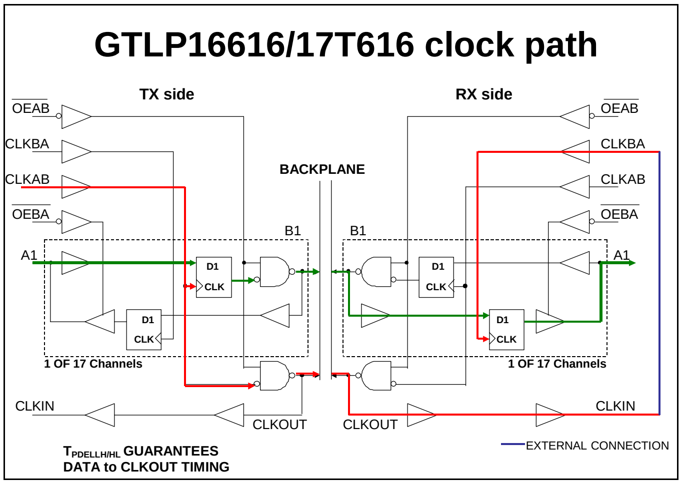
In this study it will require 8 GTLP devices to implement the 128-bit buswidth. The single clock line needs to follow the same path, use the same trace width, and have the same device loading as the data path bits. This will reduce the clock to data skew due to PCB effects to a minimum possible value.

Slide #13: Solution using the GTLP17T616



Likely Solution using GTLP '616

Slide #14: Clock and Data Architecture

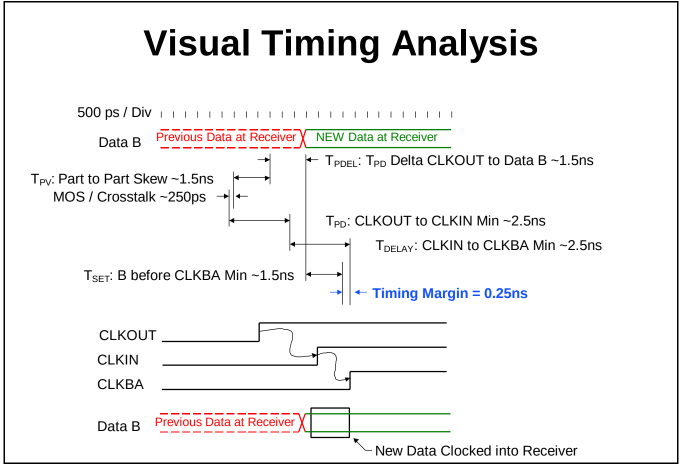


GTLP16616/17T616 clock path

T$_{PDELLH/HL}$ GUARANTEES DATA to CLKOUT TIMING

The solution showing a GTLP17T616 interface sends out the datapath clock signal on the CLKAB to CLKOUT path. This path has skew specifications designed to guarantee timing relative to all the CLKAB to B datapath signals (T$_{PDEL}$). Because multiple devices are used across the parallel interface, device to device skew must be accounted for in the timing calculations. The addition of the device to device timing variable requires a delay element to be added in the CLKIN to CLKBA path. This delay element works to guarantee the B to CLKBA data setup time specification.

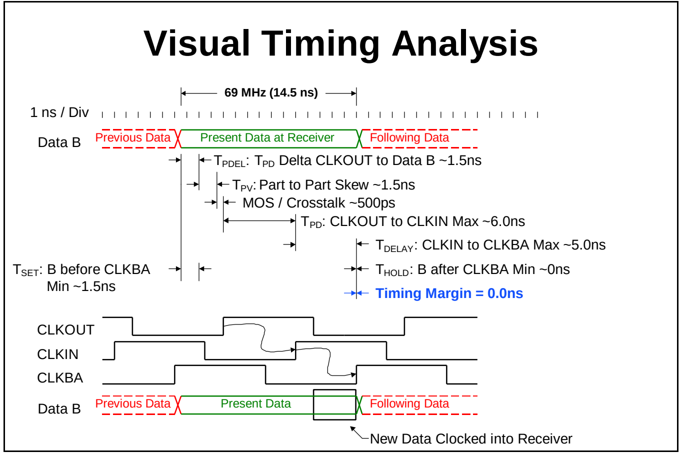
Slide #15: Visual Timing Analysis



Visual Timing Analysis

Now that the interface is a source synchronous environment, master clock skew has been eliminated from the variable list. In this analysis the designer must ensure the data or interface clock adheres to the setup and hold requirements of the receiving device for the accompanying data. Pushing the data clock 1.5ns ahead of it's accompanying data, adding worst case device to device skew, and potential signal to signal interference (crosstalk) provides a mechanism to ensure the correct data is always clocked into the receiver.

Slide #16: Visual Timing Analysis

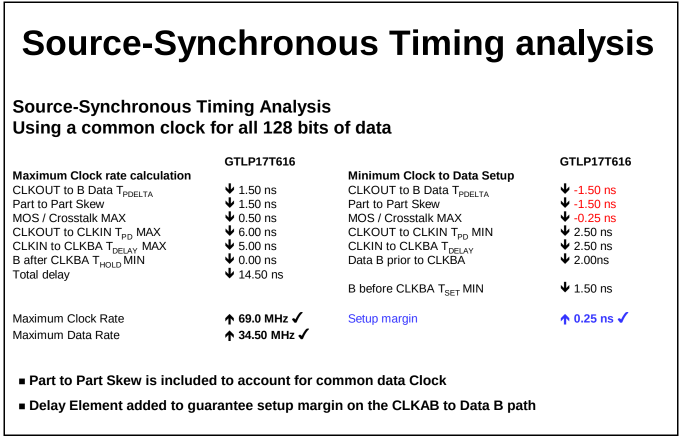


Visual Timing Analysis

By slowing the clock relative to the data, one end of our timing window has been established. The second half of the analysis will determine how quickly new data may be clocked into the receiver.

The data clock now lags it's accompanying data by 1.5ns. The part to part skew assumes the data clock (CLKOUT) is being driven from a "slow" device adding another 1.5ns of potential delay. A multiple output switching event and/or signal to signal interaction on the PCB must also be accounted for in the timing analysis. Now that the data clock has reached the receiving device, maximizing the loop delay through the '616 and it's additional delay element will determine the best possible data rate. Again, a "What if?" analysis can be used to look at available options which can improve the performance or reduce the cost of the system.

Slide #17: Source-Synchronous Timing Analysis



Source-Synchronous Timing analysis

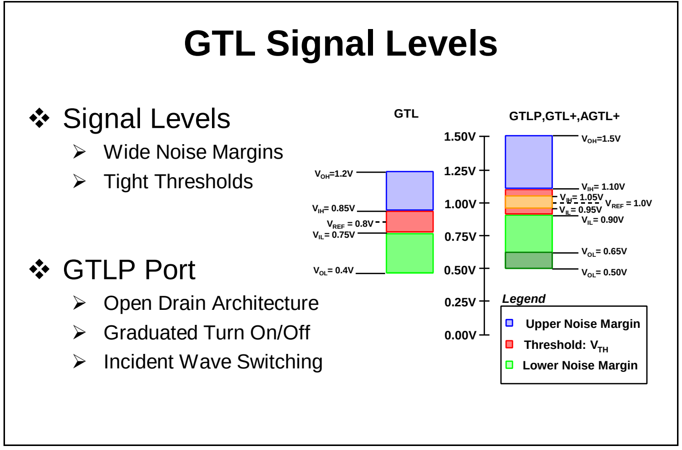
Source-Synchronous Timing Analysis
Using a common clock for all 128 bits of data

Maximum Clock rate calculation	**GTLP17T616**	**Minimum Clock to Data Setup**	**GTLP17T616**
CLKOUT to B Data T_{PDELTA}	↓ 1.50 ns	CLKOUT to B Data T_{PDELTA}	↓ -1.50 ns
Part to Part Skew	↓ 1.50 ns	Part to Part Skew	↓ -1.50 ns
MOS / Crosstalk MAX	↓ 0.50 ns	MOS / Crosstalk MAX	↓ -0.25 ns
CLKOUT to CLKIN T_{PD} MAX	↓ 6.00 ns	CLKOUT to CLKIN T_{PD} MIN	↓ 2.50 ns
CLKIN to CLKBA T_{DELAY} MAX	↓ 5.00 ns	CLKIN to CLKBA T_{DELAY}	↓ 2.50 ns
B after CLKBA T_{HOLD} MIN	↓ 0.00 ns	Data B prior to CLKBA	↓ 2.00ns
Total delay	↓ 14.50 ns		
		B before CLKBA T_{SET} MIN	↓ 1.50 ns
Maximum Clock Rate	↑ **69.0 MHz** ✓	Setup margin	↑ **0.25 ns** ✓
Maximum Data Rate	↑ **34.50 MHz** ✓		

- **Part to Part Skew is included to account for common data Clock**
- **Delay Element added to guarantee setup margin on the CLKAB to Data B path**

All the system variables consume 14.5ns of time, which works out to a clock frequency of ~69MHz. Any attempts to clock data through the interface cannot guarantee there will be enough time to clock in valid data before the incoming data has started to change state.

Slide #18: GTL Signal Levels



GTL Signal Levels

- Signal Levels
  - Wide Noise Margins
  - Tight Thresholds
- GTLP Port
  - Open Drain Architecture
  - Graduated Turn On/Off
  - Incident Wave Switching

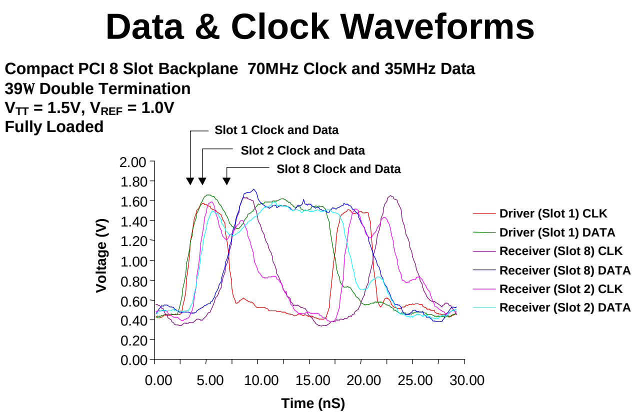
GTLP signaling is based on an open drain output structure. This type of I/O uses termination voltage and resistance to develop the output HIGH voltage or V_{OH}. There are several advantages of GTL over LVTTL logic.

1. Reduced output swing eases dynamic current requirements during output transitions.
2. Reduced output swing can reduce system EMI.
3. Tightened input threshold guarantees improve the available noise margin. V_{REF} input is used to set the actual input threshold.

The key GTL feature for a sucessful, easy to use interface product is the Graduated Turn-On / Turn-Off output buffer. Sudden release of the pulldown transistor in the open drain output will allow for extremely high di/dt values during LH transitions. There are two primary factors driving the potentially high rate of current change.

1. The large (>40mA) static current component present in each bit of the termination scheme.
2. The ideal termination for a heavily loaded backplane interface can be as low as 18-25Ω.

Slide #19: Source-Synchronous Data and Clock Waveforms

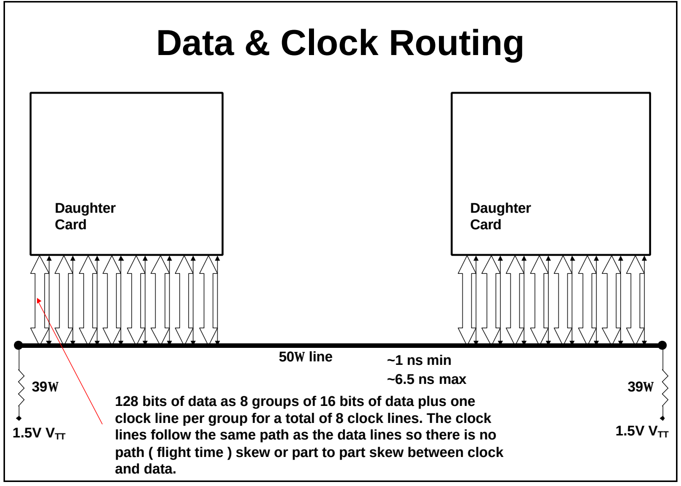


Data & Clock Waveforms

Compact PCI 8 Slot Backplane 70MHz Clock and 35MHz Data
39W Double Termination
V_{TT} = 1.5V, V_{REF} = 1.0V
Fully Loaded

All of the upfront design and simulation work leads to a verification of the backplane interface. Starting with the LH edges from left to right show the driver waveforms, adjacent slot waveforms, and far end waveforms. This particular cPCI backplane has a 1ns delay to an adjacent slot and a 4ns delay end to end. In this instance the clock / data timing relationship is +/- 125ps at the driver, adjacent and far slot receivers. All propagation delays have been measured at 1.0V.

Slide #20: Data and Clock Routing with private clock

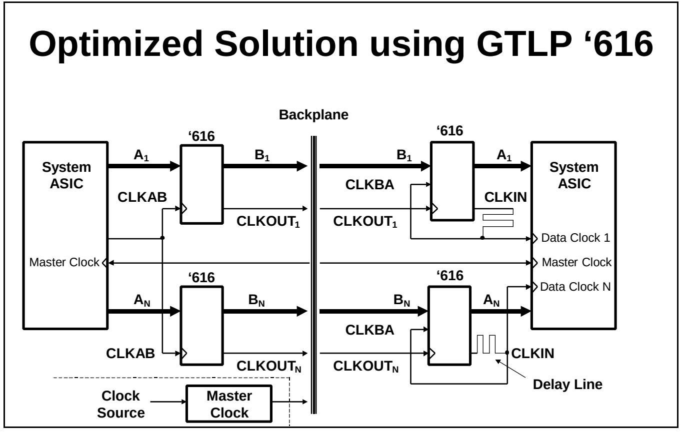


Data & Clock Routing

128 bits of data as 8 groups of 16 bits of data plus one clock line per group for a total of 8 clock lines. The clock lines follow the same path as the data lines so there is no path (flight time) skew or part to part skew between clock and data.

In this study it will require 8 GTLP devices to implement the 128 bit buswidth. Accepting the routing overhead of seven (7) additional clock lines benefits the potential overall system performance. Sending a "private" clock for each interface device eliminates the device to device skew variable, which had to be included in the "common" clock calculation. As with the common clock line, private clock lines need to follow the same path, use the same trace width, and have the same device loading as the data path bits. This will reduce the clock to data skew due to a minimum possible value.

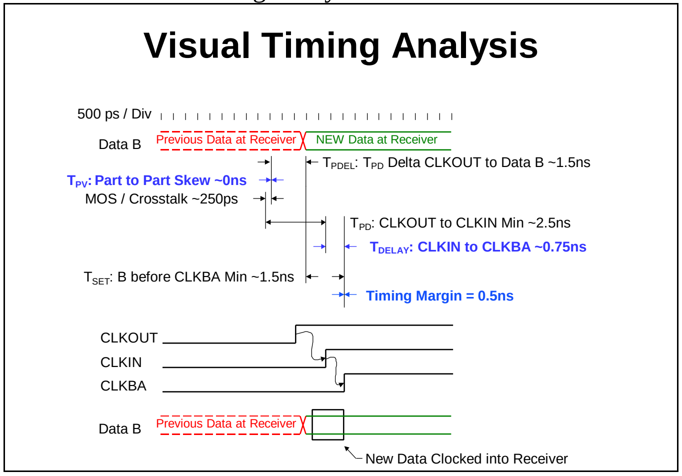
Slide #21: Optimized Solution using the GTLP17T616



Optimized Solution using GTLP '616

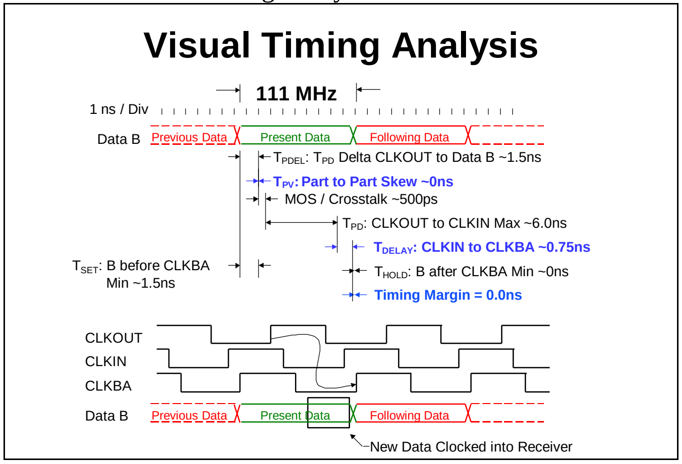
The solution showing a GTLP17T616 interface sends out the datapath clock signal on the CLKAB to CLKOUT path. This path has skew specifications designed to guarantee timing relative to all the CLKAB to B datapath signals (T_{PDEL}). As shown in the block diagram in Slide #20 multiple "private" clocks eliminate the device to device skew variable. Instead of the delay element used in the common clock scenario, a short delay line constructed of PCB trace provides all the delay necessary to guarantee the B to CLKBA data setup time specification.

Slide #22: Visual timing Analysis



Visual Timing Analysis

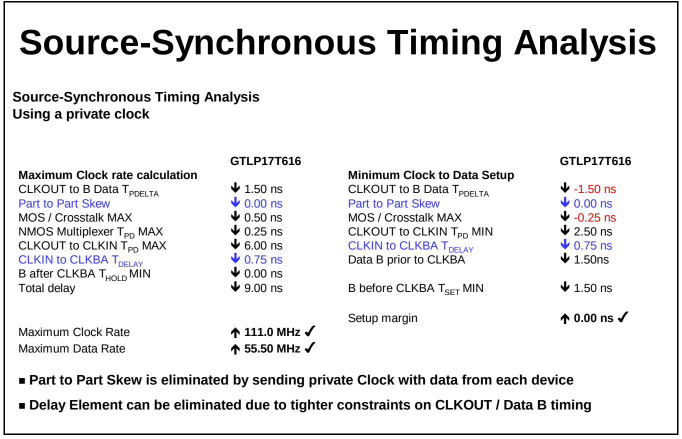
Slide #23: Visual Timing Analysis



Visual Timing Analysis

By eliminating performance limiting variables and minimizing the loopback delay (CLKOUT to CLKIN to CLKBA path) associated with the GTLP17T616 an optimal solution can be achieved. Variable elimination creates a tighter set of constraints surrounding the clock data relationship allowing higher bandwidth across the same 128-bit interface. The key variable eliminated is the device to device skew. Removing skew from the datarate calculation allows the maximum CLKIN to CLKBA delay to be reduced by 4.25ns.

Slide #24: Source-Synchronous Timing Analysis



Source-Synchronous Timing Analysis

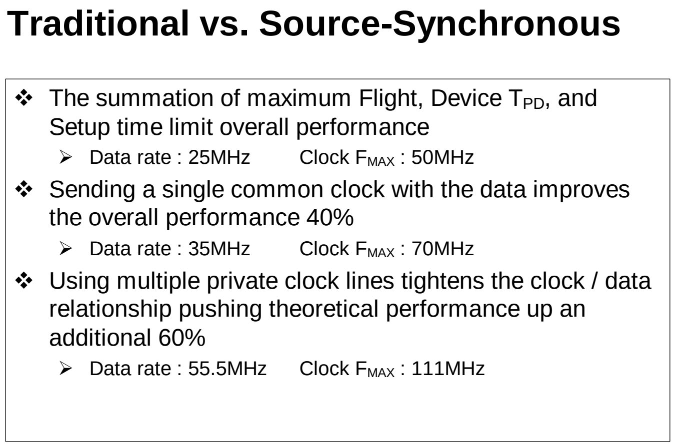
Source-Synchronous Timing Analysis
Using a private clock

Maximum Clock rate calculation	**GTLP17T616**
CLKOUT to B Data T_{PDELTA}	↓ 1.50 ns
Part to Part Skew	↓ 0.00 ns
MOS / Crosstalk MAX	↓ 0.50 ns
NMOS Multiplexer T_{PD} MAX	↓ 0.25 ns
CLKOUT to CLKIN T_{PD} MAX	↓ 6.00 ns
CLKIN to CLKBA T_{DELAY}	↓ 0.75 ns
B after CLKBA T_{HOLD} MIN	↓ 0.00 ns
Total delay	↓ 9.00 ns
Maximum Clock Rate	↑ **111.0 MHz** ✓
Maximum Data Rate	↑ **55.50 MHz** ✓

Minimum Clock to Data Setup	**GTLP17T616**
CLKOUT to B Data T_{PDELTA}	↓ -1.50 ns
Part to Part Skew	↓ 0.00 ns
MOS / Crosstalk MAX	↓ -0.25 ns
CLKOUT to CLKIN T_{PD} MIN	↓ 2.50 ns
CLKIN to CLKBA T_{DELAY}	↓ 0.75 ns
Data B prior to CLKBA	↓ 1.50ns
B before CLKBA T_{SET} MIN	↓ 1.50 ns
Setup margin	↑ **0.00 ns** ✓

- **Part to Part Skew is eliminated by sending private Clock with data from each device**
- **Delay Element can be eliminated due to tighter constraints on CLKOUT / Data B timing**

Slide #25: Traditional vs. Source-Synchronous Comparison

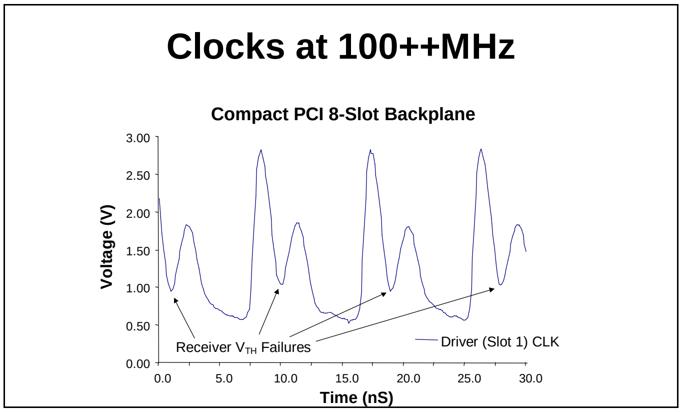


Traditional vs. Source-Synchronous

- The summation of maximum Flight, Device T_{PD}, and Setup time limit overall performance
  - Data rate : 25MHz   Clock F_{MAX} : 50MHz
- Sending a single common clock with the data improves the overall performance 40%
  - Data rate : 35MHz   Clock F_{MAX} : 70MHz
- Using multiple private clock lines tightens the clock / data relationship pushing theoretical performance up an additional 60%
  - Data rate : 55.5MHz   Clock F_{MAX} : 111MHz

Looking back and comparing the results shows a 120% bandwidth enhancement over the traditional design. Same backplane, similar products, and a new architecture, impressive results indeed. There are some costs to this performance. We've added 8 clock lines, or taken away 8 data lines, if you look at it another way. The source-synchronous nature of the backplane signals dicates that the data must now be retimed to either a master system clock or on-card clock. The basic retiming will probably take place in a system ASIC. This generally consists of at least a register and most likely a synchronous FIFO. Either of these solutions adds to the latency of information across the backplane interface.

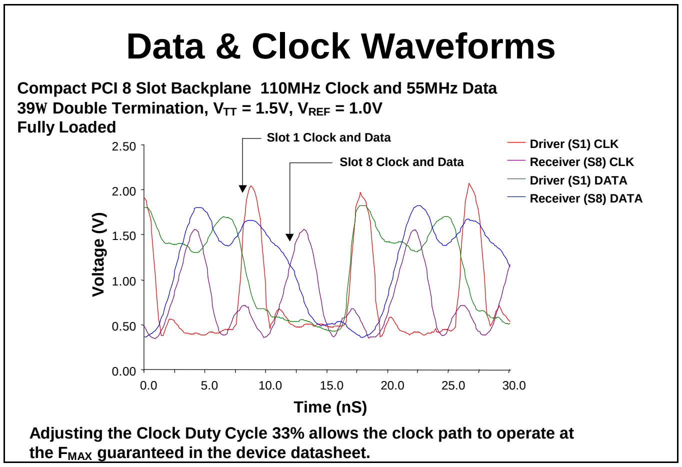
Slide #26: Clocks at 100++MHz



Clocks at 100++MHz

As the GTLP17T616 nears the datasheet specified F_{MAX}, the clock can get a little challanging to implement. Due to excessive ringing on the LH transition, receivers will likely "double clock" data at this frequency of operation. Double clocking would render the received information useless so alternative solutions must be found to maintain this newfound level of backplane performance. Fortunately, the signal integrity of the clock line can be improved by reducing the pulse width high from 50% to about 33%. This type of tuning, although difficult, does deliver impressive bandwidth gains. Combining a 1X and a 1.5X clock (ie. 100 and 150MHz) could yield a 33.3% duty cycle clock at the 1X frequency.

Slide #26: Data and Clock Waveforms



Data & Clock Waveforms

Compact PCI 8 Slot Backplane 110MHz Clock and 55MHz Data
39W Double Termination, V_{TT} = 1.5V, V_{REF} = 1.0V
Fully Loaded

Adjusting the Clock Duty Cycle 33% allows the clock path to operate at the F_{MAX} guaranteed in the device datasheet.

To put this performance into perspective you must consider current PCI specifications at 66MHz allow 4-5 slots. In addition a PCI-X proposal allows only 3 slots. The waveforms shown here are on a fully loaded 8 slot cPCI backplane. At nearly twice the frequency and twice the number of slots, this source synchronous design offers a serious performance advantage.

Slide #27: Issues and Solutions

Issues and Solutions

- Changing to a source synchronous architecture allows for a 2.5X increase in the theoretical Clock F_{MAX}. Preliminary data and simulations indicate a small solution space as the data clock approaches 100MHz.
- The question then becomes one of how to maintain backplane bandwidth. Design Contraints:
  - Same bus width
  - Reduce the clock frequency
  - No added bus latency
- SOLUTION: Send the Data Clock across the backplane interface at 1/2 speed (equal to the data rate). Multiply the Data Clock 2X on the receive card to recover the data.

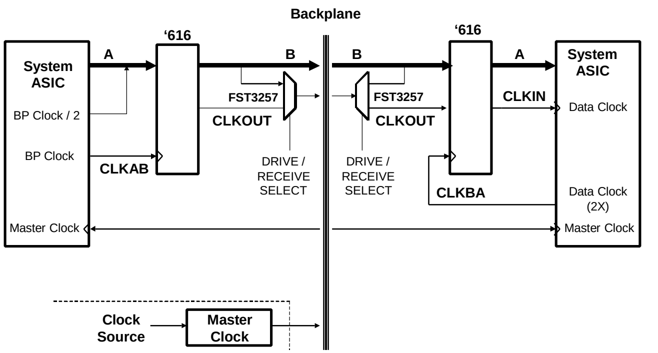
The performance on Slide #26 is a huge leap forward in potential PCI bandwidth. This performance level is however at the limit of the current GTLP product capabilities. Pushing a clean 100+ MHz clock signal down a net originally designed for 16.5MHz data is not an easy task.

So the question arises: How can we improve the solution space without throwing away all the bandwidth gains of the source-synchronous design?

The solution uses a page from the CPU design handbook. If you can't cycle any faster then do more on every cycle. By sending a ½ speed clock with the data much of the interface bandwidth can be maintained.

Slide #28: The GTLP17T616 with a ½ Speed Clock

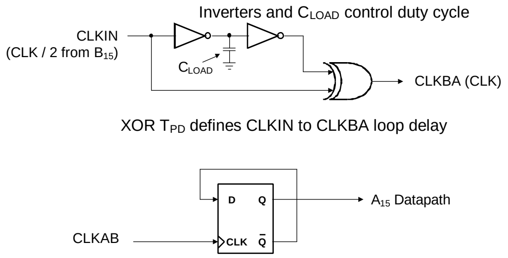
The GTLP '616 with a 1/2 speed CLK



The ½ speed clock forces the designer to multiplex the CLKOUT path with one of the datapath bits. Stuffing this datapath bit with alternating 1's and 0's will produce the ½ speed clock we need at the receiver. The full speed clock would still be needed to clock the data and the half speed clock onto the backplane interface. Due to the nature of GTL I/O and our need to preserve the clock / data timing relationship a busswitch multiplexer is used. With a typical ON resistance of 2-3Ω, little if any signal degradation will occur.

Slide #29: Clock Division and Multiplication

Clock Division and Multiplication



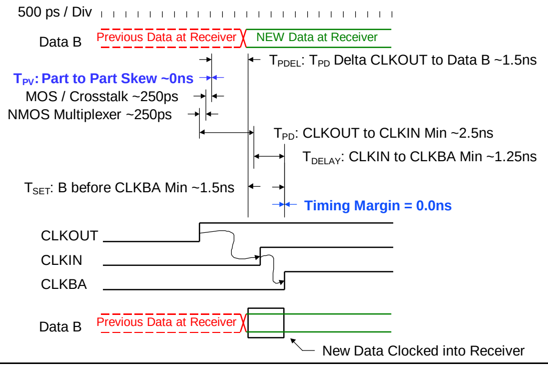
XOR T_{PD} defines CLKIN to CLKBA loop delay

D Type Flip-Flop makes a simple divide by 2 circuit

In many cases, clock division and multiplication is handled via an onboard PLL. In this case the PLL solution is unsuitable due to its lock time requirements. This design requires immediate multiplication and division. The multiplication task is handled via an inverter chain and XOR gate. The inverter delay controls duty cycle and the XOR T_{PD} defines the multiplier delay. A simple D-type FF makes a good divide by 2 circuit.

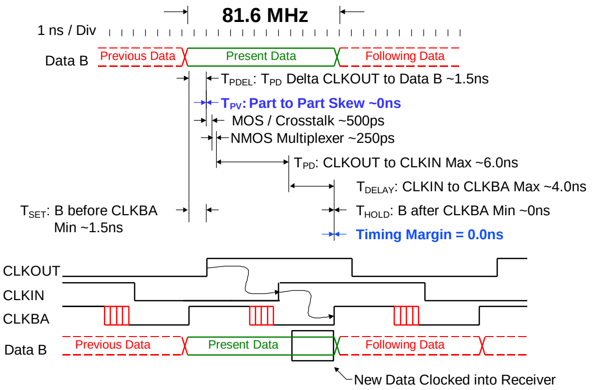
Slide #30: Visual Timing Analysis

Visual Timing Analysis



Slide #31: Visual Timing Analysis

Visual Timing Analysis



Reworking the timing analysis to account for the additional delay associated with the NMOS Multiplexer and the XOR propagation delay in the CLKIN to CLKBA path yields a maximum effective clock rate of over 80MHz. Using a faster XOR gate and adjusting the propagation delay guarantee to account for a light capacitive load would push the effective clock rate to almost 100MHz. That's just 10MHz shy of the theoretical maximum we calculated for this backplane interface in Slide #23.

Slide #32: Source-Synchronous Timing Analysis

Source-Synchronous Timing analysis

Source-Synchronous Timing Analysis
Using a 1/2 speed private clock

Maximum Clock rate calculation	**GTLP17T616**	**Minimum Clock to Data Setup**	**GTLP17T616**
CLKOUT to B Data T_{PDELTA}	↓ 1.50 ns	CLKOUT to B Data T_{PDELTA}	↓ -1.50 ns
Part to Part Skew	↓ 0.00 ns	Part to Part Skew	↓ 0.00 ns
MOS / Crosstalk MAX	↓ 0.50 ns	MOS / Crosstalk MAX	↓ -0.50 ns
NMOS Multiplexer MAX	↓ 0.25 ns	NMOS Multiplexer MAX	↓ -0.25 ns
CLKOUT to CLKIN T_{PD} MAX	↓ 6.00 ns	CLKOUT to CLKIN T_{PD} MIN	↓ 2.50 ns
CLKIN to CLKBA T_{DELAY}	↓ 4.00 ns	CLKIN to CLKBA T_{DELAY}	↓ 1.25 ns
B after CLKBA T_{HOLD} MIN	↓ 0.00 ns	Data B prior to CLKBA	↓ 1.50ns
Total delay	↓ 12.25 ns		
		B before CLKBA T_{SET} MIN	↓ 1.50 ns
Maximum Clock Rate (1/2 SPEED)	↑ **40.8 MHz ✓**	Setup margin	↑ **0.00 ns ✓**
Maximum Data Rate	↑ **40.8 MHz ✓**		

- **Part to Part Skew is eliminated by sending private Clock with data from each device**
- **Delay Element included to account for Data Clock (2X) multiplication**

Slide #33: Conclusion

Conclusion

- The source synchronous architecture is an ideal upgrade from traditional synchronous design. It will improve the throughput of many passive backplanes.
  - Eases master clock skew requirements.
  - Adds a FIFO / resynchronization function to system ASICs
  - Removes signal flight time from synchronous timing calculations
  - Eases hold time margin issues
- Future source synchronous devices will utilize differential signaling to enhance the bandwidth of passive parallel backplanes.

The source-synchronous architecture is an ideal upgrade from traditional synchronous interface design. It will improve the throughput of many passive backplanes. All interface architectures are bound to have tradeoffs, in a source-synchronous design the positives can far outweigh the negatives. In general, several statements can be made about source-synchronous architectures.

1. As timing budgets tighten designers are moving toward this type of architecture in many application areas.
2. Master clock skew requirements have been eased. This may allow for some cost savings in the clock distribution sub-system.
3. Source-synchronous architectures add a FIFO or resynchronization requirement to system ASICs.
4. Signal flight time is no longer a performance limiting factor.
5. Hold time margins are easier to meet.

In the future source-synchronous designs will use state of the art differential signaling techniques to further extend the capabilties of passive parallel backplane interfaces.