

Package enhanced layouts, for high frequency DC/DC conversion

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Introduction

In the future, with the continuing demand for higher currents, frequencies in the MHz and smaller footprints, the power converter designer will be forced to utilize the latest packaging available. Fortunately for the designer, these new smaller and innovative packages will not only lessen the size of his design, but also increase the efficiency, while at the same time, lowering its overall temperature. This paper is intended to suggest some physical and practical ways of utilizing the latest packages, in power converter layout.

Buck Converter development

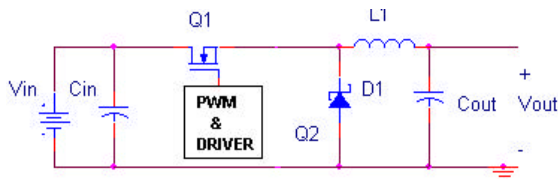


Figure 1. The Buck Converter of 20 years ago

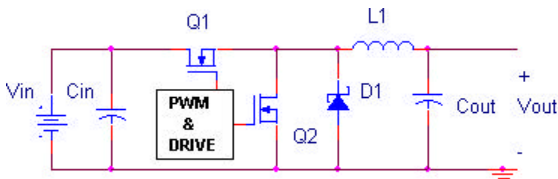


Figure 2. The Synchronous Buck Converter of today

Figure 1, shows the buck converter as it was 20 years ago, before that time the transistor had been the work horse of the buck converter and the electronics industry, in general. In the early 1980's, MOSFETs started to replace transistors in power converter designs, because of their ease of operation and their beneficial effects on efficiency. It was during the 1980's, that the basic research, development and integration of power MOSFETs, into the buck converter, took place. Today's research is focused on the internal and physical aspects of the MOSFET, instead of its applications. The question, which the

MOSFET designer faces, in terms of power conversion is: how to make a low R_g , low Q_g and low $R_{ds(on)}$ MOSFET in a small package, with great heat dissipating characteristics and low package parasitics.

In the 1980's a 200KHz, 20A converter was on the edge of technology and the converter itself was the size of a shoebox. Inductors were not bought, they were designed and the power electronics engineer had to design the control loop. The PWM/Driver box as shown in Figure 1, would have been a whole board. The engineer really had to pay attention to the poles and zeros of the input and output filters and oscillation was always a concern. EMI was another problem, which was solved by using big EMI filters on all of the input/output terminals of the converter.

As MOSFETs gained wider acceptance as a replacement for transistors in buck converters, designers started to parallel them, hence the Q1 of Figure 1, became a parallel combination of MOSFETs. This had the effect of dividing $R_{ds(on)}$ by a factor of n -MOSFETs. The benefits of this were increased load current capability and higher efficiencies, with less heat and stress on the MOSFETs. The need to parallel MOSFETs diminished as advances in MOSFET technology created ever better, smaller MOSFETs, with higher drain current capabilities, lower values of $R_{ds(on)}$ and Q_g .

The synchronous buck converter (Figure 2) is another step in the development of the buck converter. This technological advancement improved efficiency by adding Q2 in parallel to D1 or the catch diode and in effect shorted out D1, by giving the load current a lower impedance path. The purpose of the catch diode was and still is today, to provide a current path, for the current induced by the inductor, as a result of the opening of Q1 and to provide current to the load, by allowing Cout

to discharge, when Q1 remains open. The beauty of the catch diode is that it needs no control circuitry, the inductor and its reversal in voltage, when Q1 opens, activates it – it is a simple solution. Along with the addition of Q2 came the need for more complex controllers and also a new problem: shoot through.

Shoot through is an undesired mode of operation, in which Q1 & Q2 turn on at the same time and V_{in} is shorted. There are various ways that controllers deal with this problem, some add in dead time – a period of time, in which the controller turns off both MOSFETs, Figure 3. During dead time, D1 conducts, which is less energy efficient, than

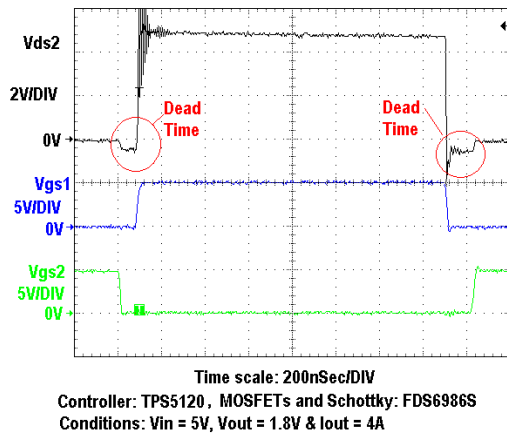


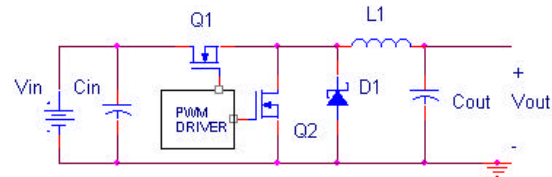
Figure 3. Dead-time: V_{D1} or V_{ds2} , V_{gs1} & V_{gs2}

when Q2 conducts. Hence, companies are developing better and better strategies to deal with this problem. Some companies are monitoring V_{gs} voltages and using those to determine the turn-on of the other MOSFET. However, there is a trade-off; a trade-off between the assurance of no shoot-through and efficiency. The question is: how much dead time is too much dead time. In some cases, shoot through does occur, but for such a small period of time, that it doesn't matter – the MOSFET is not damaged and losses in the efficiency are small. I believe, that there is an optimal trade-off here, where the losses in efficiency due to shoot-through equals the losses in efficiency due to the controller imposed dead time. At this point, more shoot through would cause greater losses, than the losses incurred by the dead time needed to limit the shoot through to a reasonable limit. This is an academic point of operation, which would be impossible to find, for a buck

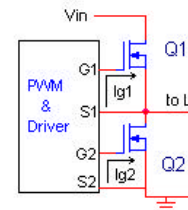
converter composed of real parts, because of the variations in boards, board layouts and parts. However, as technology advances, perhaps, even this will be determinable.

Critical Current Loops – Gate Drive

For just about every current loop in a buck converter, layout is critical. My first priorities are the gate drive loops. These current loops are illustrated in Figure 4b, where the controller (PWM) and drivers are combined into one integrated chip. The gate drive loops control the speed and the ability of the MOSFETs to turn on and off, without damage. As can be seen in Figure 5, fast switching speeds are highly desirable, in terms of efficiency, however they can cause shoot through and excess gate ringing, which if not controlled can cause damage to the MOSFET.



(a) Synchronous Buck Converter



Gate-drive loops

Figure 4. (a) Synchronous Buck Converter, (b) Gate-drive loop

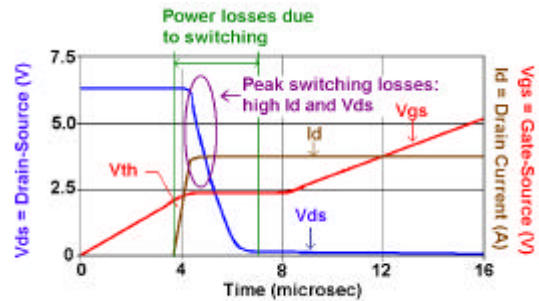


Figure 5. Typical N-Channel MOSFET curves

Part selection, board layout and parasitic inductances all have an effect on switching speeds. Fast switching times depend on using MOSFETs with low Q_g (total gate charge, necessary to turn-on the MOSFET), PWM/drivers capable of charging C_{gs} (gate to

source capacitance) to Qg rapidly and good layout practices - minimizing parasitic loop inductance. Using the Gate Charge Characteristic curve, as given in any MOSFET data sheet, the designer can select the appropriate PWM/driver. What the data sheet doesn't give are the parasitic package inductances of the MOSFET, which are typically: 0.5nH on the Drain and Source terminals, with 2 to 5 nH on the gate terminal. These inductances are out of the designer's control.

Loop Inductance

An inductor is formed anytime current flows through a loop, such as the drive circuit shown in Figure 4b. The current traveling through the loop generates a B-field within the loop, thus converting electrical energy into the magnetic energy of the B-field. The loop of the drive circuit is formed by the traces running from the driver chip to the gate, and from the source back to the driver chip. The amount of inductance created within this loop is a function of loop-area, and the equation for inductance is as follows:

$$L = \mu_o \mu_r N^2 A / l,$$

where μ_o is the permeability of air,
 μ_r is the relative permeability of the material,
 N is the number of loops,
 A is the area of the loop,
 and l is the length of the loop.

Note: A ground plane makes a wonderful return path, because when a signal trace is placed above or below its return, their current induced B-fields cancel one another – as in a microstrip transmission line, Figure 10b.

Minimizing loop inductance

By studying, the inductance equation, as given in the last section, it can be seen, that loop inductance or parasitic inductance can be minimized by board layout. Component placement and packaging is the key. The power converter designer at this stage has to think spacially and in 3-D. The goal is to minimize the area of the current loop. Figure 6, shows one of the advantages of using a PC board in power converter layout. Both Figures, A and B, have the same area, however the shapes are different, in rectangle B, the B-field has been stretched out over a larger length, hence it is weaker than in square A, resulting in less loop inductance.

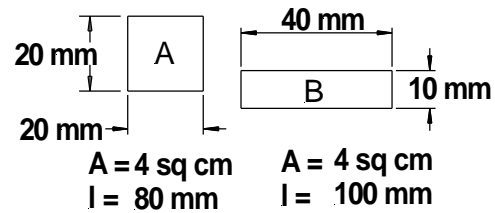


Figure 6. Inductance vs. loop shape

When picking a controller and a matching MOSFET, it is wise to look at the pin configurations of both; each should have consecutive pins for both sets of gate-source connections. A good controller will also have a dedicated source pin for the bottom MOSFET, instead of expecting the user to use one of the ground pins. The driver pins of the controller should all be on one side of the chip and if possible should match up with the corresponding pins of the MOSFET, Figure 7. A physically matching controller – MOSFET chip set is desirable, but not always obtainable. It is important to make the connections between the MOSFET and the controller, as short as possible. The two gate drive loops should never cross one another, but if it becomes necessary, they should cross one another at a 90-degree angle. This spatial positioning will minimize B-field interaction between the two gate drive loops. It is important to remember, that both of these

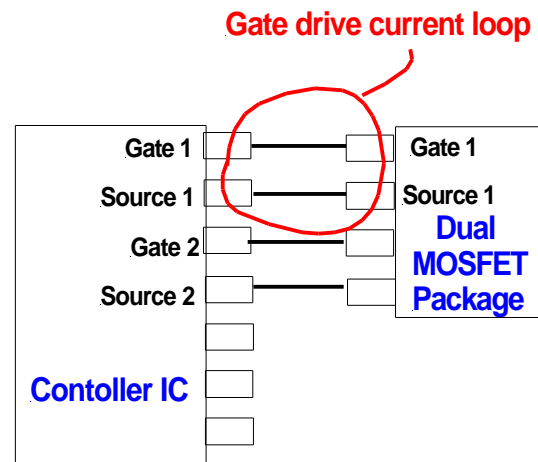


Figure 7. A physically matching, Controller-MOSFET chip set

loops are noise generators, hence any delicate circuitry such as sensing, should be kept well away from these loops. It is a common practice to construct buck converters with two separate ground planes, one for the controller

chip and its associated circuitry, and one for the power stage – Cin, Q1, Q2, D1, L and Cout. This separation is intended to keep the noise, generated through the switching action of the power MOSFETs, from entering the delicate circuitry of the controller, Figure 8. These two grounds are normally tied together, at the output of the converter.

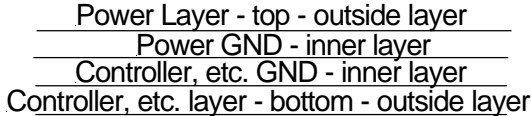


Figure 8. Example, layer arrangement for a 4-layer board

The strictness by which the rules of power conversion layout must be applied is determined by the operating frequency of the power converter. Lower frequency converters are more layout tolerant. Hence, the buck converter that ran well with MOSFETs packaged in SO-8 packages, at a low frequency, may not operate well or at all, at a higher frequency. Packaging is another issue, the designer must consider. The importance of checking pin layout, in the process of designing low parasitic inductance into the gate drive loop has already been discussed and illustrated, in Figure 7. Package pins also introduce another source of parasitic inductance – the physical shape of them and their physical distance from the board, hence the die. While the designer can't control the inner inductances of the package, he can choose a package that minimizes them. Again, as switching frequency increases, these packaging choices become more critical. MOSFET manufacturers are continually looking for better and better packaging solutions, to solve the problems of high frequency operation in buck converters. One of these solutions is International Rectifier's DirectFET packaging, Figure 9.

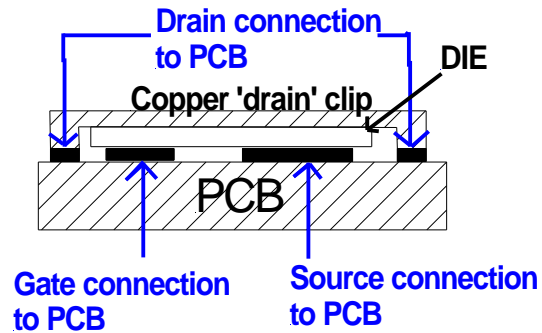


Figure 9. International Rectifier's DirectFET packaging

This packaging lays the die right on the PCB traces and either eliminates wirebonding or replaces it, with a copper clip. These improvements reduce the Rds(on) resistance of the MOSFET. Further reductions in Rds(on) are accomplished by shortening the distance; the current has to travel through the package – Id, the current flowing from the drain to the source.

Note: With the demand for higher frequency circuits, manufacturers have started designing parts that only work well within certain frequency ranges – magnetics, capacitors, etc. So beware, your high frequency part may not work well in a low frequency application.

Parasitic Board Effect

The advent of the high frequency, high current buck converter has forced designers to view the PCB board, less as a fixture for parts and more as a circuit element. In fact, the board itself, the insulator material between the layers, acts as a capacitor. As circuit frequency increases, the parasitic capacitance of the board decreases. The board parameter describing this electrical property is the "dielectric constant" = $\epsilon = C(\text{board trace}) / C$ of the same traces, with air as the material of separation. Therefore, the parasitic capacitance of two traces, separated by a PCB board is proportional to ϵ of the board material and parasitic $C = C(\text{air}) * \epsilon$. For a board material such as FR-4, with $\epsilon @ 1\text{MHz} = 4.4$ and $\epsilon @ 1\text{GHz} = 3.9$, the parasitic capacitance decreases, as circuit frequency increases.

At high frequencies (1MHz and above), the gate-drive circuit needs to be viewed as a transmission line. This allows the board designer to calculate the inductance and the

capacitance of the traces, in terms of characteristic impedance, $Z_0 = \text{Sq.root}(L/C)$.

The characteristic impedance of a transmission line is the ratio of V/I of a pulse traveling along it. The gate-drive circuit is a single ended transmission line (Figure 10a), which when placed on a PC board takes the physical form of a microstrip, Figure 10b. The gate-drive transmission line starts at the driver (source) and ends at the gate-source connection of the MOSFET (load), Figure 10a.

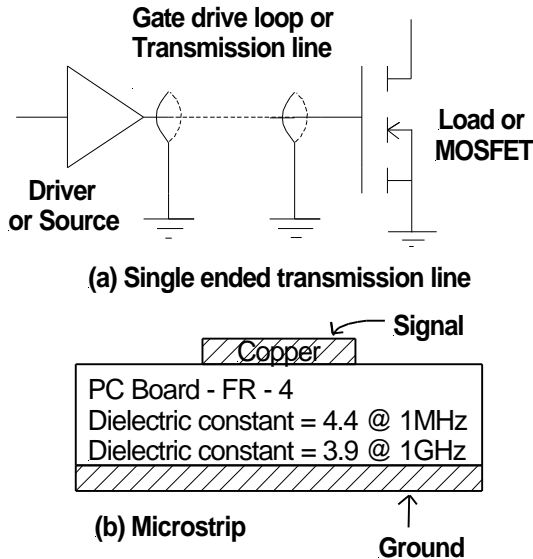


Figure 10.

In this new view, the gate-drive turn-on pulse is viewed as a propagating pulse, which takes on wave properties. These wave properties are comparable to the wave properties of light, passing through glass. When a light wave passes through a pane of glass, some of it is reflected back and some of it goes through the pane. The light passing through the pane is weaker in intensity, than the original light - before it entered the pane. This loss in intensity is due to the reflection of light, at the boundary between air and glass and its associated energy loss. This is exactly what happens to a voltage/current waveform, when it meets a different value of impedance. At the boundary, where the difference in impedance occurs, some of the voltage/current waveform will be reflected back, along the transmission line and the energy in the forward moving wave will be reduced. The goal of the designer is to match all of the impedances in the circuit, which in the case of the gate-drive circuit includes: driver, transmission line and the MOSFET's gate-source connection. Since, the impedance of the gate-source connection

is variable and dependent on the turn-on characteristics of the MOSFET, the search for the perfect match is and will continue to be an R&D project for the immediate future. When it is solved, it will usher in a new era in the ever-evolving development of the buck converter.

IC solutions

The layout of the gate-drive circuitry is a complicated affair, at high frequencies (1MHz and above). Today's converters generally operate within a frequency range of between 300KHz and 1MHz. For the 300KHz to 600KHz range, a designer can use a chip set such as the FAN5234 controller, with the FDS6986S, in the arrangement illustrated in Figures 8 & 11.

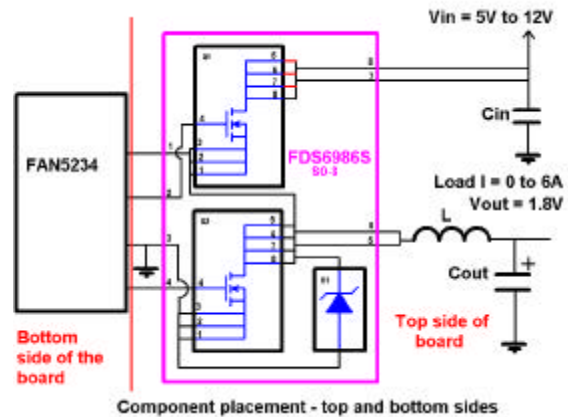


Figure 11.

The FDS6986S contains, two different, application-selected power MOSFETs (Q1 and Q2) and a schottky diode or catch diode. This arrangement reduces the reverse recovery losses of Q2, by placing the schottky diode in parallel and as close to Q2 as possible, thus minimizing the parasitic inductance between the two.

Another IC solution comes from Texas instruments, with their Swift family of DC/DC regulators, packaged in their PowerPAD packaging. This family of regulators puts the controller, drivers, MOSFETs and schottky diode all in one thermally enhanced package. The PowerPAD package mounts the dies on a heat sink and leaves the heat sink exposed, on the bottom of the package, so that the designer can solder it to the PC board. The Swift family of regulators by TI simplifies the designer's layout task. The designer is left only to design and layout C_{in} , L , C_{out} and the misc. sense and control circuitry, Figure 12.

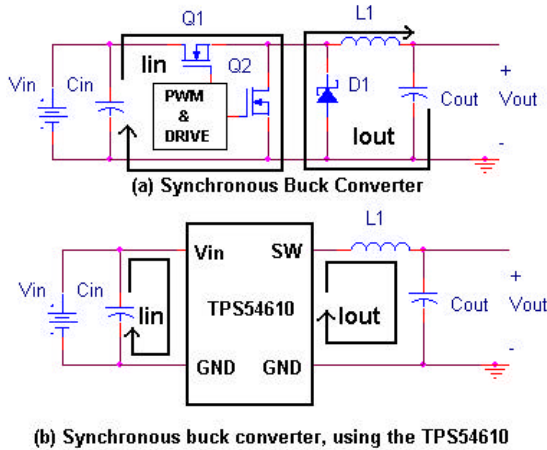


Figure 12. Synchronous buck converter, using one of the Swift family of regulators

Critical Loops – C_{in} and C_{out}

C_{in} layout is a matter of keeping the Q1, Q2 and D1 current loop small, Figure 13a and Figure 13b. In order to understand why this must be so, the input current into a buck converter must be viewed as a series of current pulses. When Q1 is closed, current flows out of C_{in} and when Q1 is open C_{in} is recharged by the power source (V_{in}).

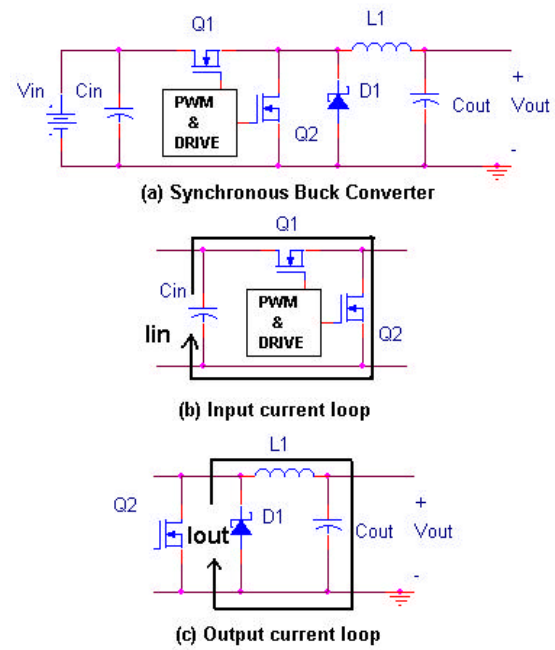
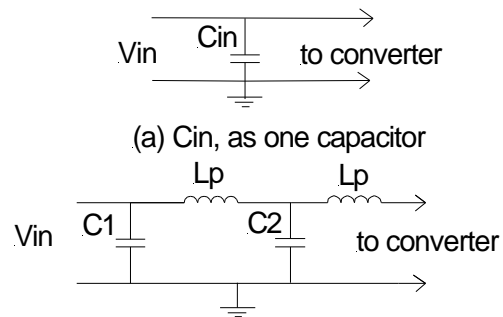


Figure 13. Synchronous buck converter, with critical current loops indicated

Any parasitic loop inductance will slow down this process and increase the switching losses of Q1. This is especially true of high frequency power converters. The trick is to maintain a good ground plane and to layout the input capacitors, as close to one another and V_{in} , as possible. Note: When designing C_{in} as a group of parallel capacitors, which reduces ESR, each parallel connection becomes a source of parasitic inductance, Figure 14.



(b) $C_{in} = C1 + C2$, L_p = parasitic inductance

Figure 14. C_{in} and parasitic inductance

Laying out the output circuitry – Q2, D1, L and C_{out} is basically the same as laying out C_{in} and its associated circuitry, Figure 13a and Figure 13b – l_{in} and l_{out} . Figure 12b shows how good IC selection can simplify the layout of both l_{in} and l_{out} . Good IC selection can



make board layout easier, simpler and smaller, resulting in a better functioning buck converter.

Summary

More and more, the layout issues of today are being solved on the IC level. In the future, the power converter designer is going to be part IC designer, part Rf designer and part board designer. The future of power electronics looks bright and interesting.

Reference:

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