Non-Volatile Memory Quality and Reliability Information

Overview

The reliability and performance of Fairchild Semiconductor's Non-Volatile Memories is assured through the use of conservative design rules, ongoing statistical Process Control (SPC) of all Fab and Assembly processes, stringent product qualification criteria and monthly ongoing reliability audits. These quality systems assure the end user that all Fairchild memory products provide outstanding Quality (adherence to datasheet specifications) and Reliability (Quality over time) in all applications.

Initial Device/Package Qualification

All new products and process changes, including, but not limited to, Fabrication, Assembly and Test, are subjected to rigorous testing prior to release to production. All Fairchild EPROM, EEPROM and Flash memories are subjected to stress testing which includes, but may not be limited to, the tests shown in the table below.

In addition to the standard qualification, other tests unique to memory devices are employed to screen out failure modes specific to EPROM, EEPROM and Flash memories. The ability to program and erase repeatedly (endurance) and data retention (data stability over time) are fundamental attributes that are tested prior to product release.

The combination of these general and NVM-specific stresses assures the end user that all devices will continue to exceed the customer's expectations over the lifetime of the part in all applications.

Qualification Table*

Test	Conditions	Duration
Dynamic Operating Life (Dynamic Burn-In)	V_{CC}: 5.5V Temperature: 125°C	1,000 Hours
Temperature/ Humidity/Bias	V_{CC}: 5.5V Temperature: 85°C Humidity: 85% RH	1,000 Hours
Temperature Cycle (Unbiased)	-65°C ÷ +150°C	1,000 Cycles
Autoclave (Unbiased)	Temperature: 121°C Pressure: 15 PSIG RH = 100%	500 Hours
High Temperature Data retention	Temperature: 150°C (Plastic) 250°C (Ceramic)	1,000 Hours
Electrostatic Discharge (ESD)	Human Body Model Voltage: 2,000V Machine Model Voltage: 200V	
Latch-up	Current: ± 200mA Voltage: 1.5x	
Endurance Cycling	V_{CC} = 5V Temperature: + 25°C	1,000KC

* Please note that these are minimum conditions used and may change as market conditions require

Ongoing Reliability Audits

Each month, samples of device families and package styles are drawn from production lots and submitted to variety of tests including Operating Life, Temperature Humidity Bias, Temperature Cycling, Data Retention, Endurance, and Autoclave Tests. This ongoing assessment of Fairchild's product families and technology provides assurance to the customer that all Fairchild processes and products are fully under control during all phases of manufacturing.

Periodic Audit Table

Test	Conditions	Duration	Sample Size	Accept Number
Dynamic Operating Life (Dynamic Burn-In)	V_{CC}: 5.5V Temperature: +150°C	1,000 Hours	100	0
Temperature/Humidity (Biased)	V_{CC}: 5.5V Temperature: 85°C Humidity: 85% RH	1,000 Hours	100	0
Temperature Cycle (Unbiased)	-65°C ÷ +150°C	1,000 Cycles	100	0
Autoclave (Unbiased)	Temperature: 121°C Pressure: 15 PSIG RH = 100%	500 Hours	100	0
High-Temperature Data Retention	Temperature: +150°C	1,000 Hours	100	0
Endurance	Cycling: Room Bake +150 2 hrs	800K Cycling	80	0-5

Surface-Mount Package Pre-Conditioning

It has been well established that surface mount IC package reliability can be compromised by the stress of various SMD solder attachment techniques during customer assembly (such as IR, Vapor Phase, or other SMD soldering methods). This harsh assembly environment, which represents actual practice in manufacturing, must also be simulated in the SOIC qualification process in additional to the stresses and tests described above. If SOIC 'preconditioning' is not used before environmental stress tests, the results could be misleading (devices pass the qualification, but may fail in the actual application).

Fairchild, as all industry leaders have done, has implemented the following series of preconditioning stresses which are applied to the devices prior to the Temperature-Humidity-Bias (THBT), Autoclave (ACLV) and Temperature Cycling (TMCL) stresses.

Surface Mount (SOIC and related) Package Preconditioning Flow

- 30 temp cycles, -65°C to +150°C
- Bake, 8 hrs @ 125°C
- Moisture soak
- 3 Simulated IR or VP Reflow cycles
- Flux immersion and clean

DIP ("through-hole") Package Preconditioning Flow

- 30 temp cycles, -65°C to +150°C
- Moisture soak
- Flux immersion and clean

Reliability Testing Details

Reliability is defined as "*The characteristic of an item expressed by the probability that it will perform its required function under stated conditions for a stated period of time,"* otherwise known as 'quality over time.'

Because the qualification and periodic audit focus is Reliability, rather than Quality (initial conformance to specifications), any statement about reliability, directly or indirectly, must include some measure of time (as the focus is on a device's *future* state will be). As such, reliability testing attempts to predict the future with 'accelerated' stress tests, in which techniques, such as heating the part up to +150°C, are utilized to "speed up the clock." If temperature acceleration (for example) were not used, the devices would be under stress for periods up to 50 years! Therefore, stress tests typically employ conditions such as temperature, voltage, mechanical shock and humidity to satisfy the conditions of 'Quality over time' for integrated circuits.

Dynamic Operating Life Test (DOPL)

The high temperature operating life test is the most commonly used, and generally accepted, accelerated life test in the semiconductor industry. The role of high temperature in accelerating chemical and physical failure mechanisms has been well established. In this stress, sample devices are exercised under bias while being subjected to elevated temperatures (most frequently +125°C or +150°C) for extended periods of time. The voltage and temperature stresses of this test can actively promote such failure mechanisms as oxide breakdown, electromigration, surface or bulk leakage, ionic contamination or channeling that may indicate design or manufacturing deficiencies.

There are two types of burn-in, *Static*, wherein the device is only placed under Vcc bias, and *Dynamic*, wherein the device's inputs and functions are 'exercised' by product-specific signals designed to make the part function as close to ‘normal operation’, while under burn-in. Fairchild Semiconductor uses Dynamic burn-in as it’s default condition in order to more-fully stress the part.

Temperature Cycle Test (TMCL)

In this test, devices are cycled between hot and cold chambers to determine the resistance of devices to *non-extreme* temperature changes (The more extreme temperature change is known as ‘Thermal Shock’ and is not used for plastic packages). The rapid change in temperature extremes from ‘cold’ to ‘hot’ (see Table I) provides accelerated mechanical stresses far greater than those expected during a typical device’s lifetime of operation.

Temperature-Humidity-Bias Test (THBT)

‘Temperature-Humidity-Bias’ stress at +85°C/85% RH (Relative Humidity) is the industry standard environmental stress test whose role is to accelerate electrochemical failure of plastic packaged devices through the application of moisture, temperature, and DC bias. Unlike hermetic cavity packages, moisture can permeate the plastic ‘body’ and potentially affect the device’s performance. The applied bias is used to create potential silicon bias to accelerate the corrosion of die metallization (the primary failure mechanism).

Autoclave Test (ACLV)

Autoclave is another accelerated environmental test that assesses the mechanical integrity of the plastic package and the resultant effects of galvanic corrosion. This test uses pressure, as well as temperature and humidity, to stress the plastic encapsulated devices. Unlike the THBT stress, the device is not under DC bias.

High Temperature Data Retention (HDTR)

This test uses heat on unbiased, programmed devices, to measure the ability non-volatile memories to retain data after having been programmed. This is also referred to as the ‘Data Retention’ test.

ESD Test

Establishes the device susceptibility to Electro-Static Discharge damage.

Latch-Up Test

This test attempts to induce a ‘latch-up’ condition in the device by forcing voltage/current on the I/O pins, raising the V_{CC} level or pulsing the I/Os or V_{CC} in an effort to trigger an “SCR” high current latched condition (wherein the device draws excessive current and is completely non-functional. Typically, this can be reset by removing V_{CC} and re-biasing the device)