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GTLP vs. GTL: A Performance Comparison from a System Perspective

Abstract

GTL/GTLP is an I/O technology for driving high speed backplanes. Both Fairchild Semiconductor and Texas Instruments offer interface devices designed around the GTL JEDEC specification. This applications note compares the Fairchild GTLP16612 device and the TI GTL16612 device based on key backplane system performance attributes. The results show that Fairchild's GTLP16612 is a superior overall backplane driver solution.

Introduction

When designing a high performance system backplane, device selection is as critical as backplane topology, connector design and termination methods. Choosing a technology and supplier of a backplane device is often limited to viewing and comparing device datasheets. However, comparing datasheet specifications does not provide a complete understanding of which I/O technologies will perform best in a system environment.

This paper compares two competing backplane driver offerings, each designed around the Gunning Transceiver Logic (GTL) JEDEC specification. Using a combination of bench fixtures and an evaluation backplane, data was collected on the Fairchild Semiconductor GTLP16612 device and the Texas Instruments GTL16612 device (Note 1). The results show that, when comparing critical system parameters (speed, noise, power and EMI) in a system environment, the Fairchild GTLP16612 device is a superior overall solution than the TI GTL16612 offering.

Note 1: For each comparison parameter, data was collected on each product using identical test fixtures and loads. The TI GTL16612 samples were 56 lead SSOP devices from date code 5BCH14K while the Fairchild GTLP16612 samples were 56 lead SSOP devices from the Fairchild GTLP16612 product characterization build.

Background

GTL, approved as a JEDEC Standard in 1993, was originally created as a CMOS, reduced swing I/O driver technology to support high speed busses and backplanes. Since its approval, a wide range of products, ranging from ASICs and processors to interface components, have been designed with GTL standard I/O or a derivative of the GTL standard I/O specification. While interest in GTL has crossed a variety of applications, the use of GTL as a backplane driver technology has surfaced as a clear focus for the technology.

Both Fairchild Semiconductor and Texas Instruments offer interface components designed around the GTL specification. However, there are significant design differences between the Fairchild and TI offerings. Texas Instruments chose to fully meet the GTL JEDEC specifications with devices designed on a BiCMOS process and with fast output edge rates. This decision resulted in a compliant part, but with trade-offs on static power and output noise. Fairchild Semiconductor chose a derivative of the GTL specification with the objective of providing a better overall backplane driver. Fairchild's offering, called GTLP, includes controlled edge rate circuitry that results in reduced switching noise and reduced signal settling times (i.e. faster system speeds). GTLP still provides GTL JEDEC Standard benefits including incident wave switching into a 50Ω transmission line, reduced swing, open drain outputs; tight threshold, differential inputs; and low I/O capacitance.

Specification Differences Between GTLP and the GTL Standard

With the CMOS process and edge rate control implemented on GTLP, the primary deviations from the GTL standard are the specified V_{OL}, V_{TT} and V_{REF} levels. Fairchild's GTLP product has a specified V_{OL} of 0.65V @34 mA vs. the GTL specification of 0.4V @40 mA. As well as higher V_{OL}, corresponding adjustments were made to the open drain termination voltage (V_{TT}) and differential input voltage reference (V_{REF}) values for GTLP increasing the output level to input level noise margins. Figure 1 summarizes the V_{OL}, V_{TT} and V_{REF} differences, and the resulting noise margins.

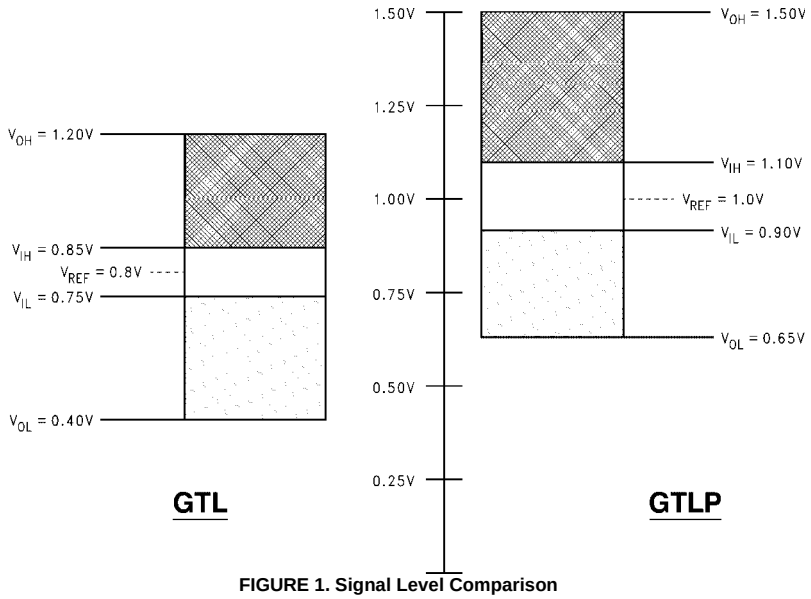


FIGURE 1. Signal Level Comparison

Comparing Key System Level Performance Parameters

The Impact of Noise on System Level Speed

Comparing device datasheet specifications does not always provide a true comparison of how devices will perform in a system environment. An example of this fact is found when comparing AC propagation delays between the TI GTL16612 and Fairchild GTLP16612 products. While the datasheet specifications for propagation delays are faster for the GTL16612 device than for the GTLP16612 device, a comparison on an evaluation backplane shows that the Fairchild GTLP16612 is faster in a backplane system.

AC propagation delays provide an indication of how long it takes for a signal to propagate through a device. Propagation delays are only one piece of the system timing equation. System timing is dependent on both device propagation delay and flight times.

Flight time is the time delay between a driver output transition at one location on a bus and a corresponding receiver input transition at another location on the bus. It is measured from the point when the driver output transitions through the switching threshold until the receiver input transitions to, and maintains, a level above V_{IH} (for a LH transition) and below V_{IL} (for a HL transition). Flight time is dependent on backplane trace characteristics (e.g. inductance, capacitance and length), incident wave voltage level requirements vs. device drive levels, bus loads, reflections and signal settling times. The settling times, incident wave switching and bus loads are all directly influenced by device I/O.

Both GTL and GTLP support incident wave switching into a 50Ω transmission line and have low I/O capacitance (i.e. less bus loading per device). However, evaluation data indicates that, with the addition of the edge rate control circuitry on GTLP, the settling time for Fairchild GTLP16612 is less than TI GTL16612. This improved settling time gives the Fairchild GTLP16612 a definitive performance advantage.

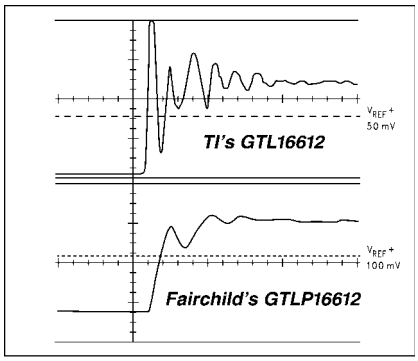
Settling time is a by-product of device output noise and ground/V_{CC} shift. Each of these parameters is a function of output edge rates, dynamic current and lead/trace inductance (–L di/dt). When an output transitions, the rate of current change through both the power pins and output pin results in output noise and power plane shifting. With slower edge rates and lower lead/trace inductance, the output noise and power plane shift results in a small amplitude, damped oscillation around the V_{OL} and V_{OH} levels. The settling time of this oscillation adds to system flight time since the many system timing specifications require that the output must settle within a specified percentage of V_{OL} or V_{OH} prior to the next output transition.

As edge rates get faster, the power plane shift and output noise increases. This output noise can increase to a point where the output signal oscillates back through the input threshold of the receiving device. This condition is often called ringback. As with settling times, ringback directly

Comparing Key System Level Performance Parameters (Continued)

adds to the system flight times and results in slower system level speed.

Figure 2 and Figure 3 show an output waveform comparison between the GTLP16612 and GTL16612 products on the evaluation backplane (Note 2). The data represents a single output switching at 1 MHz in the center of the backplane (Z_o = 65Ω) populated with 8 cards (equally distributed) and terminated at both ends with a 50Ω termination to V_{TT}. Per the datasheet specifications, a 1.2V V_{TT} was used when collecting GTL data while 1.5V was used when collecting GTLP data. Similar waveforms were also found on a lumped load bench fixture.

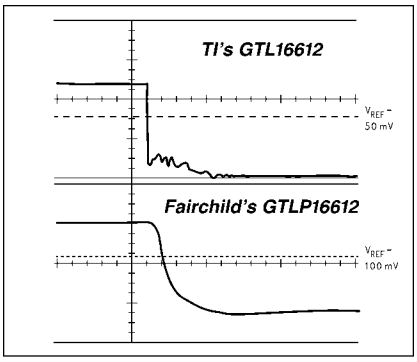


Prop delay (spec'd)	t_{PLH}
TI GTL16612:	4.0 ns max.
FSC GTLP16612:	8.2 ns max.

FIGURE 2.

Note that, on the TI GTL device, a LOW-to-HIGH output transition results in an output ringback condition (i.e. following the initial output low to high transition, the output rings back through the input threshold region). The ringback condition on TI's GTL16612 results in a longer flight time requirement than with Fairchild's GTLP16612 (Note 3). Therefore, the same application will run faster with Fairchild's GTLP16612.

As with most system performance issues, minimizing noise is a function of factors both internal and external to a device. Proper termination, layout, connector selection, decoupling and noise generated from other devices sharing the same power bussing or I/O bussing must all be considered in minimizing system level noise.



Prop delay (spec'd)	t_{PHL}
TI GTL16612:	3.8 ns max.
FSC GTLP16612:	6.5 ns max.

FIGURE 3.

Note 2: The evaluation backplane was not optimized for stub lengths, connector design or impedance matching and, therefore, data collected on the backplane should be treated as preliminary. While not optimized, the backplane does provide a comparison of performance with the devices in an identical system level environment.

Note 3: The GTLP16612 edge rate control circuit reduces the rate at which the open drain output pull down transistor turns on and turns off. For the LH edge, the slow turn off of the GTLP pull down results in a slower LH transition to V_{TT} and, in turn, faster output settling times.

Table 1 shows the positive impact of the edge rate control on the power and ground pin shift. The table values represent the worst case pin measurements, in the TTL to GTL/GTLP direction, with 17 outputs switching and 1 output quiet (i.e. not switching) for measurement. The outputs were loaded with a 25Ω termination to V_{TT} (i.e. 1.2V for GTL and 1.5V for GTLP) and a lumped 30 pF capacitor to ground. All measurements were made with nominal V_{CC} and room temperature.

TABLE 1. Quiet O/P Switching (Bench Comparison)

	V_{OL}	V_{OLP}	V_{OLV}	V_{OHP}	V_{OHV}
FSC GTLP16612	0.45V	V_{OL} + 0.25V	V_{OL} − 0.25V	V_{TT} + 0.17V	V_{TT} − 0.25V
TI GTL16612	0.25V	V_{OL} + 0.60V	V_{OL} − 1.23V	V_{TT} + 1.03V	V_{TT} − 0.82V

Simulating the GTL16612 vs. GTLP16612 Output Waveforms

The magnitude of the ringback found in the TI GTL16612 LOW-to-HIGH output transition suggests that inductance, edge rate and dynamic current are not the only factors impacting its poor waveform integrity. The TI GTL16612 output ringback appears to be a result of the output transistor actively pulling the output back low after the initial LOW-to-HIGH transition (Note 4). This phenomenon is not easily modeled with a transient waveform simulation.

IBIS simulation models were generated for a GTL16612 device and a GTLP16612 device, using bench I/V data. A subsequent simulation showed that the Fairchild GTLP16612 waveform simulation accurately modeled the lumped load bench data. However, the TI GTL16612 ringback could not be simulated with the IBIS model. A SPICE simulation, using the TI supplied GTL16612 spice model and an internally generated Fairchild GTLP16612 spice model, showed the same results as the IBIS simulation (i.e. correlation between GTLP16612 bench and simulation data, and the inability to simulate the ringback condition on the GTL16612).

Note 4: This ringback explanation is a hypothesis based on the wave form characteristics and the lumped load simulation results. With no access to the internal design information, no definitive explanation for the TI GTL ringback can be provided.

Comparing Key System Level Performance Parameters (Continued)

Power

Power management is a key design requirement in nearly all applications and is essential in portable applications. Reducing power improves system reliability, and can also help simplify the physical layer design and reduce the total system cost.

The total power consumed by an active IC is comprised of a static power component and a dynamic power component. Each of these components are then comprised of two subcomponents accounting for current sourced internally to the device and current supplied to (or from) loads external to the device.

Internal Power Dissipation

An IC's internal static (or quiescent) power is a result of ICCQ current and is most impacted by fabrication process and I/O design. The internal dynamic power, the power dissipated to charge and discharge internal device capacitances, is proportional to operating frequency, output voltage swing amplitude, internal and I/O capacitance, and V_{CC} levels.

Power vs. frequency bench data collected on GTLP16612 and GTL16612 devices shows that both products have similar internal dynamic power per unit frequency performance. However, as a CMOS device, Fairchild's GTLP16612 offering has significantly lower static I_{CC} current than the TI GTL16612 offering. The lower static I_{CC} with Fairchild's GTLP16612 translates to a lower total internal power dissipation.

Figure 4 and Figure 5 show a bench measurement comparison of internal static and dynamic I_{CC} (I_{CCD}) for each product. Separate dynamic I_{CC} measurements were made with the device conditioned in the A to B and B to A directions. Open connections on the outputs ensured that no externally influenced dynamic or static currents were included in the measurements. All measurements were made at nominal V_{CC} and room temperature.

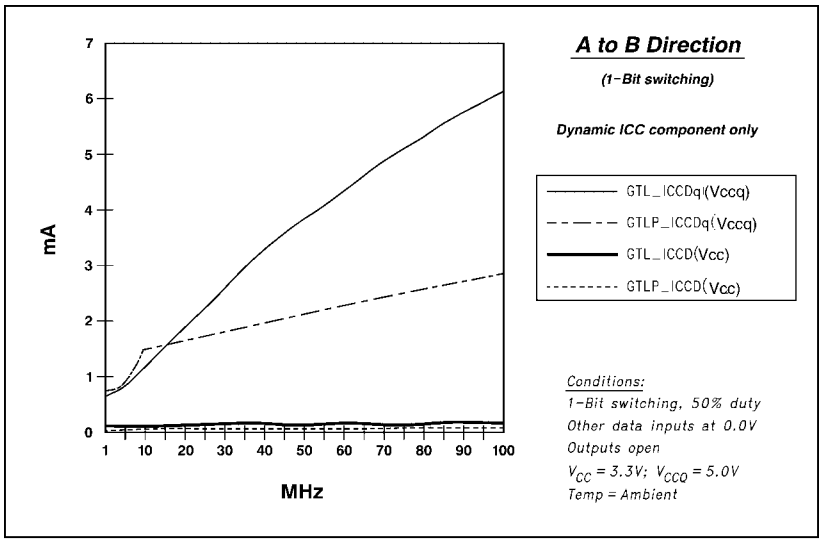


FIGURE 4.

A to B	V_{CC}	V_{CCQ}	Units
I_{CCD} (Dynamic I_{CC})			
FSC	0.000	0.019	mA/MHz
TI	0.001	0.057	mA/MHz
I_{CC}(Static I_{CC})			
FSC	0.0	27.0	mA/MHz
TI	4.0	66.0	mA/MHz

Comparing Key System Level Performance Parameters (Continued)

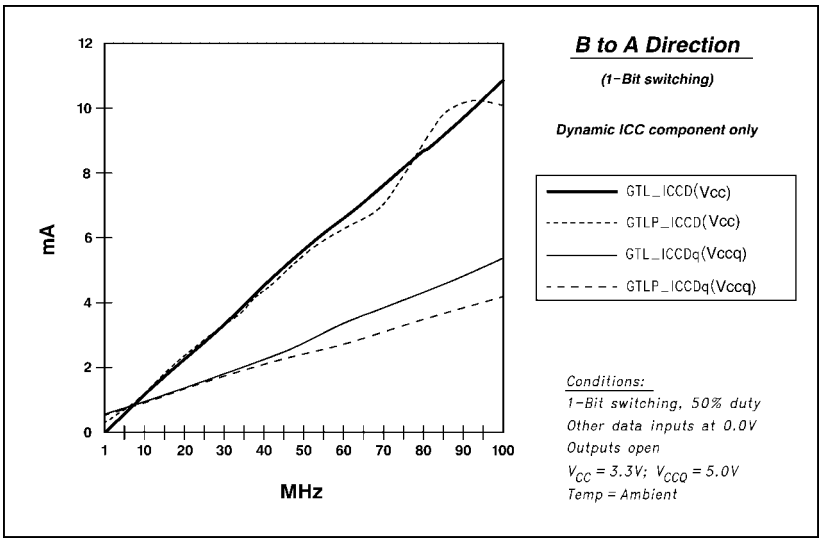


FIGURE 5.

B to A	V_{CC}	V_{CCQ}	Units
I_{CCD} (Dynamic I_{CC})			
FSC	0.105	0.036	mA/MHz
TI	0.107	0.050	mA/MHz
I_{CC}(Static I_{CC})			
FSC	0.0	27.0	mA/MHz
TI	4.0	66.0	mA/MHz

The power calculations (following) assume a 25 MHz data rate with all 18 data bits toggling (i.e. #bits = 18). Since the GTL16612 and GTLP16612 products have two, separate power supply pin levels and separate power planes internally (i.e. 3.3V and 5.0V), separate internal power dissipation calculations were made for each supply. All static and dynamic current data points used in the internal power calculations below are bench measured values.

$\mathbf{P_{internal}} = \mathbf{P_{static}} + \mathbf{P_{dynamic}}$

$\mathbf{P_{static}} = \mathbf{P_{ccq}} + \mathbf{P_{cc}}$

where $P_{ccq} = I_{CCQ} * V_{CCQ}$ (5.0V)

and $P_{cc} = I_{CC} * V_{CC}$ (3.3V)

$\mathbf{P_{dynamic}} = \mathbf{P_{ccdq}} + \mathbf{P_{ccd}}$

where P_{ccdq} = ICCDq/MHz * Data Frequency * V_{ccq} * #bits

and P_{ccd} = ICCD/MHz * Data Frequency * V_{CC} * #bits

Comparing Key System Level Performance Parameters (Continued)

FSC GTLP16612	TI GTL16612
I_{CCQ} = 27 mA	I_{CCQ} = 66 mA
I_{CC} = 0 mA	I_{CC} = 4 mA
P_{static} = 135 mW	P_{static} = 350 mW
A to B direction:	
ICCDq/MHz per bit = 19 µA	ICCDq/MHz per bit = 57 µA
ICCD/MHz per bit = 0 µA	ICCD/MHz per bit = 0 µA
$P_{dynamic}$ = 43 mW	$P_{dynamic}$ = 128 mW
$P_{internal}$(ab) = 178 mW	**$P_{internal}$(ab) = 478 mW**
B to A direction:	
ICCDq/MHz per bit = 36 µA	ICCDq/MHz per bit = 50 µA
ICCD/MHz per bit = 105 µA	ICCD/MHz per bit = 107 µA
$P_{dynamic}$ = 237 mW	$P_{dynamic}$ = 272 mW
$P_{internal}$(ba) = 372 mW	**$P_{internal}$(ba) = 622 mW**

Power Dissipation Related to External Loads

For devices with totem pole output structures and CMOS inputs (negligible input leakage), the external component of power dissipation is limited to the dynamic current needed to charge and discharge external capacitance (interconnect capacitance and I/O capacitance of devices sharing the bus) (Note 5). However, with the open drain output structures implemented on GTL and GTLP, the static and dynamic current supplied by the termination voltage source must also be considered.

The most efficient method of determining externally influenced static and dynamic device power dissipation is to use calculations based on various frequencies and bus loads. A comparison of calculated externally influenced power dissipation for TI's GTL16612 and Fairchild's GTLP16612 is shown below. The comparison assumes a 30 pF lumped load to ground, a 50 MHz (50% duty cycle) clock frequency and all 18 bits toggling (#bits = 18).

The calculations show that lower V_{OL} and V_{TT} values found with TI's GTL result in lower externally influenced power dissipation with the devices conditioned in the A to B (TTL to GTL) direction. However, for the totem pole, A side outputs, the externally influenced power dissipation is identical between the two devices.

Static device output power due to termination

(P_{ST}) = V_{OL} * I_{TT} * #bits (Note 6)

where ITT (static termination current) = $(V_{TT} - V_{OL})/R_{TERM}$

Dynamic output power due to termination

(P_{DT}) = V_{OL} * I_{TT} * dc* #bits

where dc is the duty cycle

Dynamic output power due to C_{LOAD}

(P_{DL}) = V_S* C_{load}* Data Fq * dc * #bits

where Data Fq (data frequency) is 1/2 the clock frequency and V_S is the output voltage swing.

$P_{external}$(ab) = P_{ST} + P_{DL} (Note 7)

$P_{external}$(ba) = P_{DL}

Note 5: Assumes no passive termination to power or ground is included on the bus connected to the totem pole output. If the termination is included, the impact of the dynamic and static leakage from the termination power supply through the output pull down transistor (or from the device V_{CC} to ground through the output pull up transistor if the termination is to ground) must be considered.

Note 6: Calculation includes only the power device level power dissipation and does not consider the power dissipation of the termination resistor. When calculating the total system power dissipation, the total additional power from the GTL/GTLP architecture will be P_{total} * the number of GTLP/GTL devices + the power dissipated by the termination resistors (where the termination resistor power is $(V_{TT} - V_{OL})/R_{TERM}$ * V_{TT} * number of GTLP/GTL bus terminations).

Note 7: Since the output is either switching or static at a given time, only the worst case termination leakage is included in the $P_{external}$ calculation.

FSC GTLP16612	TI GTL16612
A to B direction:	
V_{TT} = 1.5V	V_{TT} = 1.2V
V_{OL} = 0.45V (typ)	V_{OL} = 0.25V (typ)
R_{TERM} = 25Ω	R_{TERM} = 25Ω
P_{ST} = 340 mW	P_{ST} = 171 mW
P_{DT}= 170 mW	P_{DT}= 86 mW
P_{DL} = 7 mW	P_{DL} = 6 mW
$P_{external}$(ab) = 347 mW	**$P_{external}$(ab) = 177 mW**
B to A direction:	
V_S = 1.9V	V_S = 1.9V
$P_{external}$(ba) = 25 mW	**$P_{external}$(ba) = 25 mW**

Comparing Key System Level Performance Parameters (Continued)

Comparing the total power dissipation between the GTL16612 and GTLP16612 devices shows that, for the A to B (i.e. TTL to GTL) direction, the lower CMOS internal static power for Fairchild's GTLP16612 device is marginally offset by the lower termination induced power of the TI GTL product. The result is 20% less total power dissipation with GTLP when the device is conditioned in the A to B (i.e. TTL to GTL) direction. However, when comparing total power dissipation for the B to A (i.e. GTL to TTL) direction, there is no influence from the termination and the lower internal static power results in significantly less total power dissipation (~40% less) with GTLP. The totals are listed below.

$$P_{total} = P_{internal} + P_{external}$$

FSC GTLP16612	TI GTL16612
P_{total}(ab) = 525 mW	P_{total}(ab) = 655 mW
P_{total}(ba) = 397 mW	P_{total}(ba) = 647 mW

System level power calculations will use worst case device power dissipation. Therefore, from a system's perspective, with a 25 MHz data rate (50 MHz clock frequency), a Fairchild GTLP16612 device will dissipate 20% less power than a TI GTL16612 device. As the number of GTL or GTLP devices in a system increases, this 20% power dissipation difference can become substantial.

EMI

EMI (electromagnetic interference) is radiated noise created from the acceleration of electric charge within a device and across the transmission medium between devices. This radiated noise travels in free air and, if not minimized, can lead to corrupted data and intermittent system errors. The federal communications commission (FCC) has set regulations on the maximum system EMI levels. These regulations, along with the inherent link between system reliability and EMI levels, make EMI a critical design parameter.

Device generated EMI is dependent on frequency, duty cycle, output voltage swing amplitude, slew rate and output noise (waveform ringing). EMI generated across the transmission medium between devices is impacted by these same factors plus other device to system generated high frequency signal distortion including cross talk, waveform reflections and power supply noise.

Both GTLP and GTL generate less EMI than TTL and 5V output swing functions due to their reduced output swing. However, with the addition edge rate control circuitry, and its impact on reducing the high frequency content and switching noise of an output transition, Fairchild's GTLP16612 generates lower EMI than its GTL counterpart. In addition, with all other system level conditions equal, the lower noise performance of GTLP vs. GTL will translate to lower EMI across the transmission medium.

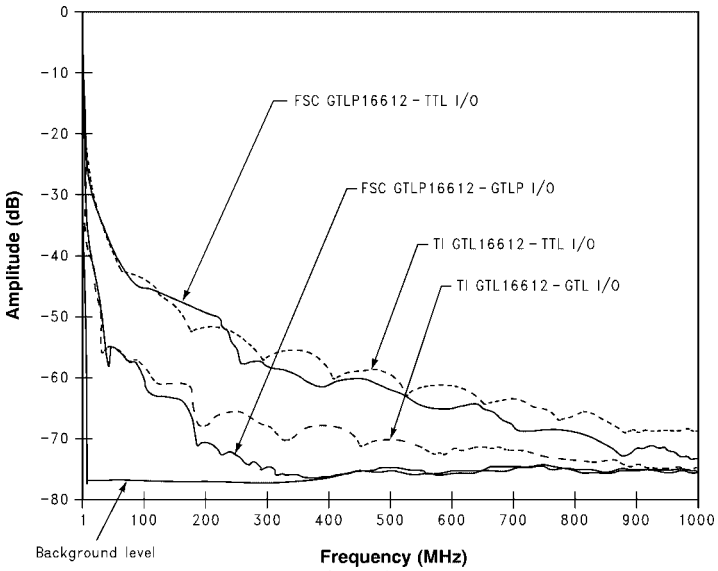


FIGURE 6.

Figure 6 shows a bench measurement comparison of device generated EMI from both a TI GTL16612 device and a Fairchild GTLP16612 device. The data was collected using a direct contact method for the TTL outputs of the device and a modified direct contact method for the GTL/GTLP outputs of the device.

The direct contact method is performed by toggling a single output at 1 MHz (others conditioned to a static low) and directly contacting the output pin with a spectrum analyzer (Note 8) probe to measure the spectral content of the toggling output signal. The probed output is lifted to eliminate the impact of test fixture in loading the output. Output loading can "smooth" the sharp corners of the output transition resulting in lower EMI measurements.

With the open drain output structure used on the GTL and GTLP devices, the V_{TT} connection is required to toggle the output. Therefore, the lifted output requirement of the direct contact method does not accommodate the EMI measure-

Comparing Key System Level Performance Parameters (Continued)

ment on the GTL/GTLP outputs. To provide a comparison of the GTL16612 and GTLP16612 EMI levels, the direct contact method was modified to include output pin contact to the test fixture's V_{TT} termination. While this violates the direct contact requirements and may lower the EMI measurements, it does provide an accurate comparison between the EMI levels with identical fixture impact.

Note 8: Data collected using an HP8591A 1.8 GHz model spectrum analyzer

Summary

When selecting a component for a high performance system design, the datasheet specifications may not fully provide either needed or accurate system level performance information. This applications note attempts to overcome the datasheet limitations by providing and comparing key system level performance data for Fairchild Semiconductor's GTLP16612 device and Texas Instrument's GTL16612 device. The results show that when comparing the system level performance of these two devices, the Fairchild GTLP16612 device has a superior performance advantage.

Both Fairchild's GTLP16612 and TI's GTL16612 products were designed around the JEDEC GTL Standard and share many common characteristics including incident wave switching into a 50Ω (effective) impedance transmission line, reduced swing outputs and tight input thresholds. However, as this applications note shows, Fairchild's derivation of the GTL specification has resulted in a better overall backplane driver solution. Fairchild's GTLP16612 device provides lower power dissipation, lower device generated EMI, lower power supply noise and, contrary to the misleading datasheet propagation delay specifications, provides faster system level performance due to faster output settling times.

To ensure an accurate comparison, all data collected and presented in this applications note was measured using identical fixtures, equipment and setup conditions (Note 9). However, the evaluation is based on specific loads, measurement techniques and fixture characteristics. The true proving ground for any device is the customer's specific application. Samples and simulation models (IBIS and SPICE) are available for the Fairchild GTLP products to support design and prototype evaluations.

Note 9: With the exception of V_{REF} and V_{TT}

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