



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

HC-MOS Power Dissipation

Fairchild Semiconductor
Application Note 303
February 1984



If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, high-speed CMOS draws five to seven orders of magnitude less power than the equivalent LSTTL function. When switching, the amount of power dissipated by both metal gate and high-speed silicon gate CMOS is directly proportional to the operating frequency of the device. This is because the higher the operating frequency, the more often the device is being switched. Since each transition requires power, power consumption increases with frequency.

First, one will find a description of the causes of power consumption in HC-CMOS and LSTTL applications. Next will follow a comparison of MM54HC/MM74HC to LSTTL power dissipation. Finally, the maximum ratings for power dissipation imposed by the device package will be discussed.

Quiescent Power Consumption

Ideally, when a CMOS integrated circuit is not switching, there should be no DC current paths from V_{CC} to ground, and the device should not draw any supply current at all. However, due to the inherent nature of semiconductors, a small amount of leakage current flows across all reverse-biased diode junctions on the integrated circuit. These leakages are caused by thermally-generated charge carriers in the diode area. As the temperature of the diode increases, so do the number of these unwanted charge carriers, hence leakage current increases.

Leakage current is specified for all CMOS devices as I_{CC} . This is the DC current that flows from V_{CC} to ground when all inputs are held at either V_{CC} or ground, and all outputs are open. This is known as the quiescent state.

For the MM54HC/MM74HC family, I_{CC} is specified at ambient temperatures (T_A) of 25°C, 85°C, and 125°C. There are three different specifications at each temperature, depending on the complexity of the device. The number of diode junctions grows with circuit complexity, thereby increasing the leakage current. The worst case I_{CC} specifications for the MM54HC/MM74HC family are summarized in Table 1. In addition, it should be noted that the maximum I_{CC} current will decrease as the temperature goes below 25°C.

TABLE 1. Supply Current (I_{CC}) for MM54HC/MM74HC Specified at $V_{CC}=6V$

T_A	Gate	Buffer	MSI	Unit
25°C	2.0	4.0	8.0	μA
85°C	20	40	80	μA
125°C	40	80	160	μA

To obtain the quiescent power consumption for any CMOS device, simply multiply I_{CC} by the supply voltage: $P_{DC} = I_{CC} V_{CC}$

Sample calculations show that at room temperature the maximum power dissipation of gate, buffer, and MSI circuits at $V_{CC}=6V$ are 10 μW , 20 μW , and 40 μW , respectively.

Dynamic Power Consumption

Dynamic power consumption is basically the result of charging and discharging capacitances. It can be broken down into three fundamental components, which are:

1. Load capacitance transient dissipation
2. Internal capacitance transient dissipation
3. Current spiking during switching.

Load Capacitance Transient Dissipation

The first contributor to power consumption is the charging and discharging of external load capacitances. Figure 1 is a schematic diagram of a simple CMOS inverter driving a capacitive load. A simple expression for power dissipation as a function of load capacitance can be derived starting with:

$$Q_L = C_L V_{CC}$$

where C_L is the load capacitance, and Q_L is the charge on the capacitor. If both sides of the equation are divided by the time required to charge and discharge the capacitor (one period, T , of the input signal), we obtain:

$$\frac{Q_L}{T} = C_L V_{CC} \left(\frac{1}{T} \right)$$

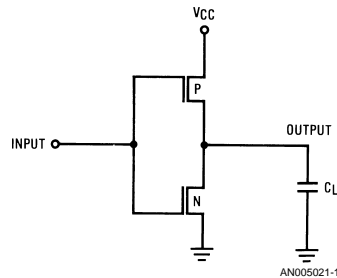


FIGURE 1. Simple CMOS Inverter Driving a Capacitive External Load

Since charge per unit time is current ($Q_L/T=I$) and the inverse of the period of a waveform is frequency ($1/T=f$):

$$I_L = C_L V_{CC} f$$

To find the power dissipation, both sides of the equation must be multiplied by the supply voltage ($P=VI$), yielding:

$$P_L = C_L V_{CC}^2 f$$

One note of caution is in order. If all the outputs of a device are not switching at the same frequency, then the power consumption must be calculated at the proper frequency for each output:

$$P_L = V_{CC}^2 (C_{L1} f_1 + C_{L2} f_2 + \dots + C_{Ln} f_n)$$

Examples of devices for which this may apply are: counters, dual flip-flops with independent clocks, and other integrated circuits containing dual, triple, etc., independent circuits.

Internal Capacitance Transient Dissipation

Internal capacitance transient dissipation is similar to load capacitance dissipation, except that the internal parasitic "on-chip" capacitance is being charged and discharged. *Figure 2* is a diagram of the parasitic nodal capacitances associated with two CMOS inverters.

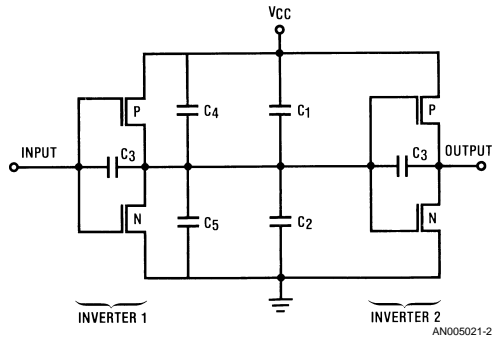


FIGURE 2. Parasitic Internal Capacitances Associated with Two Inverters

C_1 and C_2 are capacitances associated with the overlap of the gate area and the source and channel regions of the P- and N-channel transistors, respectively. C_3 is due to the overlap of the gate and source (output), and is known as the Miller capacitance. C_4 and C_5 are capacitances of the parasitic diodes from the output to V_{CC} and ground, respectively. Thus the total internal capacitance seen by inverter 1 driving inverter 2 is:

$$C_I = C_1 + C_2 + 2C_3 + C_4 + C_5$$

Since an internal capacitance may be treated identically to an external load capacitor for power consumption calculations, the same equation may be used:

$$P_I = C_I V_{CC} 2f$$

At this point, it may be assumed that different parts of the internal circuitry are operating at different frequencies. Although this is true, each part of the circuit has a fixed frequency relationship between it and the rest of the device.

Thus, one value of an effective C_I can be used to compute the internal power dissipation at any frequency. More will be said about this shortly.

Current Spiking During Switching

The final contributor to power consumption is current spiking during switching. While the input to a gate is making a transition between logic levels, both the P- and N-channel transistors are turned partially on. This creates a low impedance path for supply current to flow from V_{CC} to ground, as illustrated in *Figure 3*.

For fast input rise and fall times (shorter than 50 ns for the MM54HC/MM74HC family), the resulting power consumption is frequency dependent. This is due to the fact that the more often a device is switched, the more often the input is situated between logic levels, causing both transistors to be partially turned on. Since this power consumption is proportional to input frequency and specific to a given device in any application, as is C_{I1} , it can be combined with C_I . The resulting term is called " C_{PD} ," the no-load power dissipation capacitance. It is specified for every MM54HC/MM74HC device in the AC Electrical Characteristic section of each data sheet.

It should be noted that as input rise and fall times become longer, the switching current power dissipation becomes more dependent on the amount of time that both the P- and N-channel transistors are turned on, and less related to C_{PD} as specified in the data sheets. *Figure 4* is a representation of the effective value of C_{PD} as input rise and fall times increase for the MM54HC/MM74HC08, MM54HC/MM74HC139, and MM54HC/MM74HC390. To get a fair comparison between the three curves, each is divided by the value of C_{PD} for the particular device with fast input rise and fall times. This is represented by " C_{PD0} ," the value of C_{PD} specified in the data sheets for each part. This comparison appears in *Figure 5*. C_{PD} remains constant for input rise and fall times up to about 20 ns, after which it rises, approaching a linear slope of 1. The graphs do not all reach a slope of 1 at the same time because of necessary differences in circuit design for each part. The MM54HC/MM74HC08 exhibits the greatest change in C_{PD} , while the MM54HC/MM74HC139 shows less of an increase in C_{PD} at any given frequency. Thus, the power dissipation for most of the parts in the MM54HC/MM74HC family will fall within these two curves. One notable exception is the MM54HC/MM74HC04.

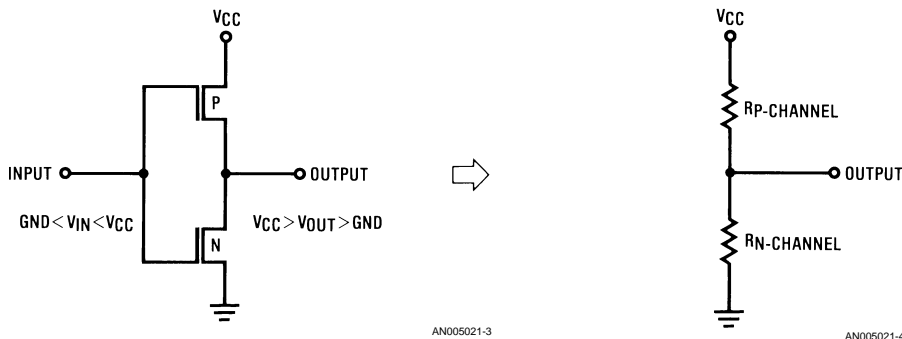


FIGURE 3. Equivalent schematic of a CMOS inverter whose input is between logic levels

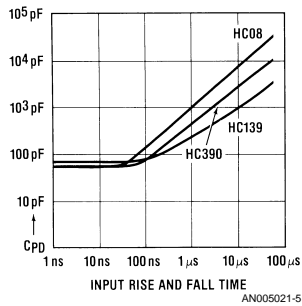


FIGURE 4. Comparison of Typical C_{PD} for MM54HC/MM74HC08, MM54HC/MM74HC139, MM54HC/MM74HC390 as a Function of Input Rise and Fall Time.
 $t_{rise}=t_{fall}$, $V_{CC}=5V$, $T_A=25^\circ C$

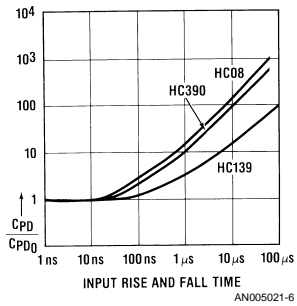


FIGURE 5. Normalized Effective C_{PD} (Typical) for Slow Input Rise and Fall Times.
 $t_{rise}=t_{fall}$, $V_{CC}=5V$, $T_A=25^\circ C$

Inputs that do not pull all the way to V_{CC} or ground can also cause an increase in power consumption, for the same reason given for slow rise and fall times. If the input voltage is between the minimum input high voltage and V_{CC} , then the input N-channel transistor will have a low impedance (i.e., be "turned on") as expected, but the P-channel transistor will not be completely turned off. Similarly, if the input is between ground and the maximum input low voltage, the P-channel transistor will be fully on and the N-channel transistor will be partially on. In either case, a resistive path from V_{CC} to ground will occur, resulting in an increase in power consumption.

Combining all the derived equations, we arrive at the following:

$$P_{TOTAL}=(C_L+C_{PD})V_{CC}2f+I_{CC}V_{CC}$$

This equation can be used to compute the total power consumption of any MM54HC/MM74HC device, as well as any other CMOS device, at any operating frequency. It includes both DC and AC contributions to power usage. C_{PD} and I_{CC} are supplied in each data sheet for the particular device, and V_{CC} and f are determined by the particular application.

Comparing HC-CMOS to LSTTL

Although power consumption is somewhat dependent on frequency in LSTTL devices, the majority of power dissipated below 1 MHz is due to quiescent supply current. LSTTL contains many resistive paths from V_{CC} to ground, and even when it is not switching, it draws several orders of magnitude greater supply current than HC-CMOS. Figure 6 is a bar graph comparison of quiescent power requirements (V_{CC}) (I_{CC}) between LSTTL and HC-CMOS devices.

The reduction in CMOS power consumption as compared to LSTTL devices is illustrated in Figure 7 and Figure 8. These graphs are comparisons of the typical supply current (I_{CC}) required for equivalent functions in MM54HC/MM74HC, MM54HC/MM74C, CD4000, and 54LS/74LS logic families. The currents were measured at room temperature ($25^\circ C$) with a supply voltage of 5V.

Figure 7 represents the supply current required for a quad NAND gate with one gate in the package switching. The MM54HC/MM74HC family draws slightly more supply current than the 54C/74C and CD4000 series. This is mainly due to the large size of the output buffers necessary to source and sink currents characteristic of the LSTTL family. Other reasons include processing differences and the larger internal circuitry required to drive the output buffers at high frequencies. The frequency at which the CMOS device draws as much power as the LSTTL device, known as the power cross-over-frequency, is about 20 MHz.

In Figure 8, which is a comparison of equivalent flip-flops (174) and shift registers (164) from the different logic families, the power cross-over frequency again occurs at about 20 MHz.

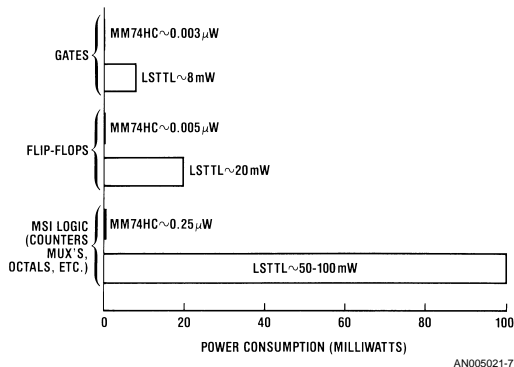


FIGURE 6. High Speed CMOS (HC-CMOS) vs. LSTTL Quiescent Power Consumption

The power cross-over frequency increases as circuit complexity increases. There are two major reasons for this. First, having more devices on an LSTTL integrated circuit means that more resistive paths between V_{CC} and ground will occur, and more quiescent current will be required. In a CMOS integrated circuit, although the supply leakage current will in-

crease, it is of such a small magnitude (nanoAmps per device) that there will be very little increase in total power consumption.

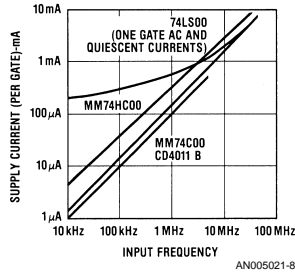


FIGURE 7. Supply Current vs. Input Frequency for Equivalent NAND Gates

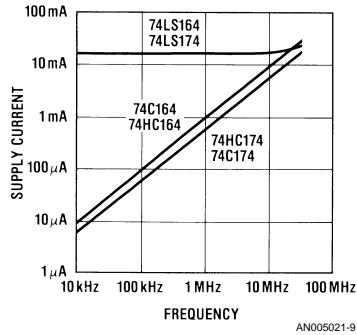


FIGURE 8. Supply Current vs. Frequency

Secondly, as system complexity increases, the percentage of the total system operating at the maximum frequency tends to decrease. Figure 9 shows block diagrams of a CMOS and an equivalent LSTTL system. In this abstract system, there is a block of parts operating at the maximum frequency (F_{max}), a block operating at half F_{max} , a block operating at one quarter F_{max} , and so on. Let us call the power consumed in the first section P_1 . In a CMOS system, since power consumption is directly proportional to the operating frequency, the amount of power consumed by the second block will be $(P_1)/2$, and the amount used in the third section will be $(P_1)/4$. If the power consumed over a large number of blocks is summed up, we obtain:

$$P_{TOTAL} = P_1 + (P_1)/2 + (P_1)/4 + \dots + (P_1)/(2^{n-1})$$

$$\text{and } P_{TOTAL} \leq 2(P_1)$$

Now consider the LSTTL system. Again, the power consumed in the first block is P_1 . The amount of power dissipated in the second block is something less than P_1 , but greater than $(P_1)/2$. For simplicity, we can assume the best case, that $P_2 = (P_1)/2$. The power consumption for all system blocks operating at frequencies $F_{max}/2$ and below will be dominated by quiescent current, which will not change with frequency. The power used by blocks 3 through n will be approximately equal to the power dissipated by block 2, $(P_1)/2$. The total power consumed in the LSTTL system is:

$$P_{TOTAL} = (P_1 + (P_1)/2 + (P_1)/2 + \dots + (P_1)/2)$$

$$P_{TOTAL} = P_1 + (N-1)(P_1)/2$$

and for $n > 2$, $P_{TOTAL} > 2(P_1)$

Thus, an LSTTL system will draw more power than an equivalent HC-CMOS system.

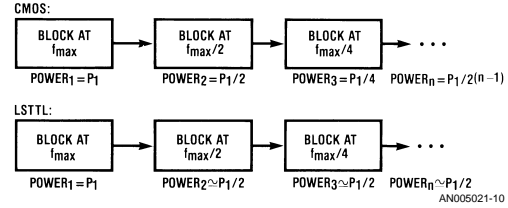


FIGURE 9. Comparison of Equivalent CMOS and LSTTL Systems

This effect is further illustrated in Figure 10. An arbitrary system is composed of 200 gates, 150 counters, and 150 full adders, with 50 pF loads on all of the outputs. The supply voltage is 5V, and the system is at room temperature. For this system, the worst case power consumption for CMOS is about an order of magnitude lower than the typical LSTTL power requirements. Thus, as system complexity increases, CMOS will save more power.

Maximum Power Dissipation Limits

It is important to take into consideration the maximum power dissipation limits imposed on a device by the package when designing with high-speed CMOS. The plastic small-outline (SO) can dissipate up to 500 mW, and the ceramic DIP and plastic DIP can dissipate up to 700 mW. Although this limit will rarely be reached in typical high-speed applications, the MM54HC/MM74HC family has such large output current source and sink capabilities that driving a resistive load could possibly take a device to the 500 or 700 mW limit. This maximum power dissipation rating should be derated, starting at 65°C for the plastic packages and 100°C for the ceramic packages. The derating factor is different for each package. The factor for the plastic small-outline is $-8.83 \text{ mW/}^\circ\text{C}$; the plastic DIP, $-12 \text{ mW/}^\circ\text{C}$; and the ceramic DIP, $-14 \text{ mW/}^\circ\text{C}$. This is illustrated in Figures 11, 12. Thus, if a device in a plastic DIP package is operating at 70°C, then the maximum power dissipation rating would be $700 \text{ mW} - (70^\circ\text{C} - 65^\circ\text{C})(12 \text{ mW/}^\circ\text{C}) = 640 \text{ mW}$. Note that the maximum ambient temperature is 85°C for plastic packages and 125°C for ceramic packages.

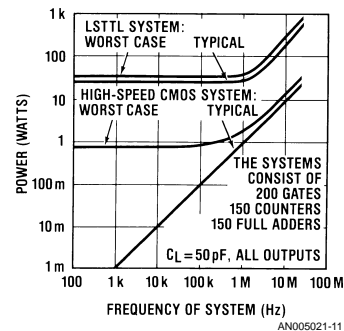
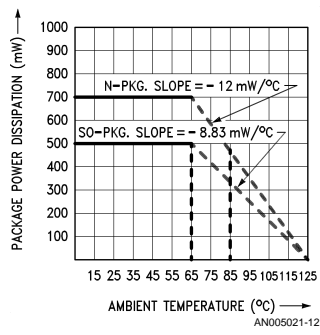
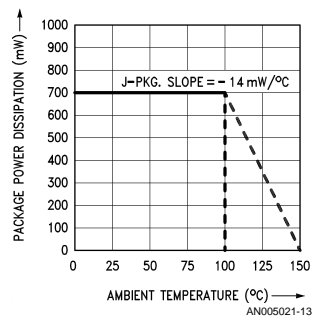


FIGURE 10. System Power vs. Frequency MMHC74HC vs. LSTTL



**FIGURE 11. Plastic Package (MM74HC)
High Temperature Power Derating
for MM54HC/MM74HC Family**



**FIGURE 12. Ceramic Package (MM54HC)
High Temperature Power Derating
for MM54HC/MM74HC Family**

Summary

The MM54HC/MM74HC high-speed silicon gate CMOS family has quiescent (standby) power consumption five to seven orders of magnitude lower than the equivalent LSTTL function. At high frequencies (30 MHz and above), both families consume a similar amount of power for very simple systems. However, as system complexity increases, HC-CMOS uses much less power than LSTTL. To keep power consumption low, input rise and fall times should be fast (less than 50 to 100 ns) and inputs should swing all the way to V_{CC} and ground.

There is an easy-to-use equation to compute the power consumption of any HC-CMOS device in any application:

$$P_{TOTAL} = (C_L + C_{PD})V_{CC}2f + I_{CC}V_{CC}$$

The maximum power dissipation rating is 500 mW per package at room temperature, and must be derated as temperature increases.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

www.fairchildsemi.com

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative