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HCMOS Crystal Oscillators

Fairchild Semiconductor
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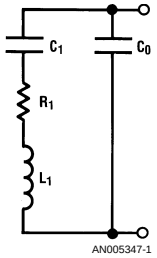
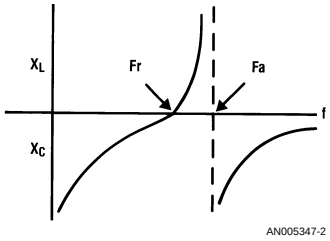
With the advent of high speed HCMOS circuits, it is possible to build systems with clock rates of greater than 30 MHz. The familiar gate oscillator circuits used at low frequencies work well at higher frequencies and either L–C or crystal resonators maybe used depending on the stability required. Above 20 MHz, it becomes expensive to fabricate fundamental mode crystals, so overtone modes are used.



Crystal Equivalent Circuit



Reactance of Crystal Resonator

FIGURE 1.

Basic Oscillator Theory

The equivalent circuit of a quartz crystal, and its reactance characteristics with frequency are shown in *Figure 1*. F_R is called the resonant frequency and is where L_1 and C_1 are in series resonance and the crystal looks like a small resistor R1. The frequency F_A is the antiresonant frequency and is the point where L_1–C_1 look inductive and resonate with C_O to form the parallel resonant frequency F_A, F_R and F_A are usually less than 0.1% apart. In specifying crystals, the frequency F_R is the oscillation frequency to the crystal in a series mode circuit, and F_R is the parallel resonant frequency. In a parallel mode circuit, the oscillation frequency will be slightly below F_A where the inductive component of the $L_1 – C_1$ arm resonates with C_O and the external circuit capacitance. The exact frequency is often corrected by the crystal manufacture to a specified load capacitance, usually 20 or 32 picofarads.

TABLE 1. Typical Crystal Parameters

Parameter	32 kHz fundamental	200 kHz fundamental	2 MHz fundamental	30 MHz overtone
R_1	200 kΩ	2 kΩ	100 Ω	20 Ω
L_1	7000H	27H	529 mH	11 mH
C_1	0.003 pF	0.024 pF	0.012 pF	0.0026 pF
C_0	1.7 pF	9 pF	4 pF	6 pF
Q	100k	18k	54k	100k

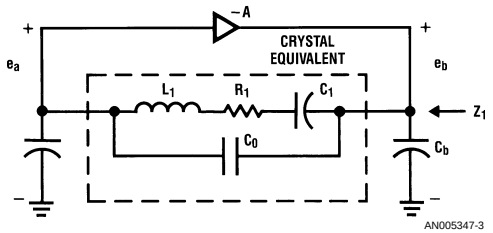


FIGURE 2. Pierce Oscillator

The Pierce oscillator is one of the more popular circuits, and is the foundation for almost all single gate oscillators in use today. In this circuit, *Figure 2*, the signal from the input to the output of the amplifier is phase shifted 180 degrees. The crystal appears as a large inductor since it is operating in the parallel mode, and in conjunction with C_A and C_B, forms a pi network that provides an additional 180 degrees of phase shift from output to the input. C_A in series with C_B plus any additional stray capacitance form the load capacitance for the crystal. In this circuit, C_A is usually made about the same value as C_B, and the total value of both capacitors in series is the load capacitance of the crystal which is generally chosen to be 32 pF, making the value of each capacitor 64 pF. The approximation equations of the load impedance, Z_1, presented to the output of the crystal oscillator's amplifier by the crystal network is:

$$Z_L = \frac{X_C^2}{R_L}$$

Where $X_C = -j/\omega C_B$ and R_L is the series resistance of the crystal as shown in Table I. Also $\omega = 2\pi f$ where f is the frequency of oscillation.

The ratio of the crystal network's input voltage to it's output voltage is given by:

$$\frac{e_A}{e_B} = \frac{\omega C_B}{\omega C_A} = \frac{C_B}{C_A}$$

C_A and C_B are chosen such that their series combination capacitance equals the load capacitance specified by the manufacturer, ie 20 pF or 32 pF as mentioned. In order to oscillate the phase shift at the desired frequency around the oscillator loop must be 360° and the gain of the oscillator loop must be greater or equal to one, or:

$$(A_A)(A_F) \geq 1$$

Where A_A is amplifier gain and A_F is crystal network voltage gain of the crystal π network: e_A/e_B. Thus not only should the series combination of C_B and C_A be chosen. The ratio of the two can be set to adjust the loop gain of the oscillator.

For example if a 2 MHz oscillator is required. Then $R_L = 100\Omega$ *Table 1.* If $e_A/e_B = 1$ and the crystal requires a 32 pF load so $C_B = 64$ pF and then C_A becomes 64 pF also. The load presented by the crystal network is $Z_L = (½\pi\ (2\ MHz)\ (64\ pF)^2)/100 = 16\ k\Omega$.

The CMOS Gate Oscillator

A CMOS gate sufficiently approaches the ideal amplifier shown above that it can be used in almost the same circuit. A review of manufacturers data sheets will reveal there are two types of inverting CMOS gates:

1. Unbuffered: gates composed of a single inverting stage. Voltage gain in the hundreds.
2. Buffered: gates composed of three inverting stages in series. Voltage gains are greater than ten thousand.

CMOS gates must be designed to drive relatively large loads and must supply a fairly large amount of current. In a single gate structure that is biased in its linear region so both devices are on, supply current will be high. Buffered gates are designed with the first and second gates to be much smaller than the output gate and will dissipate little power. Since the gain is so high, even a small signal will drive the output high or low and little power is dissipated. In this manner, unbuffered gates will dissipate more power than buffered gates.

Both buffered and unbuffered gates maybe used as crystal oscillators, with only slight design changes in the circuits.

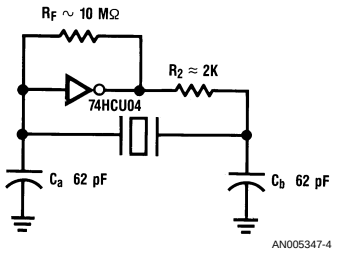


FIGURE 3. Typical Gate Oscillator

In this circuit, R_F serves to bias the gate in its linear region, insuring oscillation, while R_2 provides an impedance to add some additional phase shift in conjunction with C_B. It also serves to prevent spurious high frequency oscillations and isolates the output of the gate from the crystal network so a clean square wave can be obtained from the output of the gate. Its value is chosen to be roughly equal to the capacitive reactance of C_B at the frequency of oscillation, or the value of load impedance Z_L calculated above. In this case, there will be a two to one loss in voltage from the output of the gate to the input of the crystal network due to the voltage divider effect of R_2 and Z_L. If C_A and C_B are chosen equal, the voltage at the input to the gate will be the same as that at the input to the crystal network or one half of the voltage at the output of the gate. In this case, the gate must have a voltage gain of 2 or greater to oscillate. Except at very high frequencies, all CMOS gates have voltage gains well in excess of 10 and satisfactory operation should result.

Theory and experiment show that unbuffered gates are more stable as oscillators by as much as 5 to 1. However, unbuffered gates draw more operating power if used in the same circuit as a buffered gate. Power consumption can be minimized by increasing feedback which forces the gate to operate for less time in its linear region.

When designing with buffered gates, the value of R_2 or C_B may be increased by a factor of 10 or more. This will increase the voltage loss around the feedback loop which is desirable since the gain of the gate is considerably higher than that of an unbuffered gate.

C_A and C_B form the load capacitance for the crystal. Many crystals are cut for either 20 to 32 picofarad load capacitance. This is the capacitance that will cause the crystal to oscillate at its nominal frequency. Varying this capacitance will vary the frequency of oscillation. Generally designers work with crystal manufacturers to select the best value of load capacitance for their application, unless an off the shelf crystal is selected.

High Frequency Effects

The phase shift thru the gate may be estimated by considering it's delay time:

Phase Shift = Frequency X Time delay X 360°

The "typical gate oscillator" works well at lower frequencies where phase shift thru the gate is not excessive. However, above 4 MHz, where 10 nsec of time delay represents 14.4° of excess phase shift, R_2 should be changed to a small capacitor to avoid the additional phase shift of R_2. The value of this capacitor is approximately $1/\omega C$ where $\omega = 2\pi f$, but not less than about 20 pF.

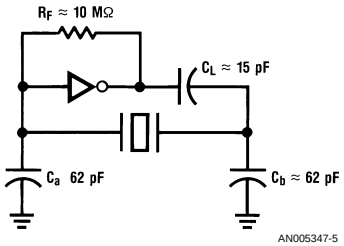


FIGURE 4. Gate Oscillator for Higher Frequencies

Improving Oscllator Stability

The CMOS gate makes a mediocre oscillator when compared to a transistor or FET: It draws more power and is generally less stable. However, extra gates are often available

and are often pressed into service as oscillators. If improved stability is required, especially from buffered gate oscillators, an approach shown in *Figure 5* can be used.

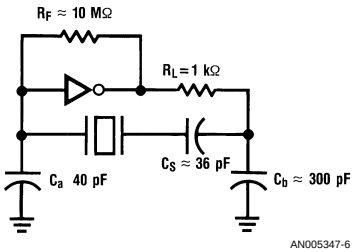


FIGURE 5. Gate oscillator with improved stability

In this circuit, C_A and C_B are made large to swamp out the effects of temperature and supply voltage change on the gate input and output impedances. A small capacitor in series with the crystal acts as the crystal load and further isolates the crystal from the rest of the circuit.

Overtone Crystal Oscillators

At frequencies above 20 MHz, it becomes increasingly difficult to cut or work with crystal blanks and so generally a crystal is used in it's overtone mode. Also, fundamental mode crystals above this frequency have less stability and greater aging rates. All crystals will exhibit the same reactance vs. frequency characteristics at odd overtone frequencies that they do at the fundamental frequency. However, the overtone resonances are not exact multiples of the fundamental, so an overtone crystal must be specified as such.

In the design of an overtone crystal oscillator, it is very important to suppress the fundamental mode, or the circuit will try to oscillate there, or worse, at both the fundamental and the overtone with little predictability as to which. Basically, this requires that the crystal feedback network have more gain at the overtone frequency than the fundamental. This is usually done with a frequency selective network such as a tuned circuit.

The circuit in *Figure 6* operates in the parallel mode just as the Pierce oscillator above. The resonant circuit L_A—C_B is an effective short at the fundamental frequency, and is tuned somewhat below the deferred crystal overtone frequency. Also, C_L is chosen to suppress operation in the fundamental mode.

The coil L_A may be tuned to produce maximum output and will affect the oscillation frequency slightly. The crystal should be specified so that proper frequency is obtained at maximum output level from the gate.

Some Practical Design Tips

In the above circuits, some generalizations can be made regarding the selection of component values.

R_F: Sets the bias point, should be as large as practical.

R1: Isolates the crystal network from the gate output and provides excess phaseshift decreasing the probability of spurious oscillation at high frequencies. Value should be approximately equal to input impedance of the crystal network or reactance of C_B at the oscillator frequency. Increasing value will decrease the amount of feedback and improve stability.

C_B: Part of load for crystal network. Often chosen to be twice the value of the crystal load capacitance. Increasing value will increase feedback.

C_A: Part of crystal load network. Often chosen to be twice the value of the crystal load capacitance. Increasing value will increase feedback.

C_L: Used in place of R1 in high frequency applications. Reactance should be approximately equal to crystal network input impedance.

Oscillator design is an imperfect art at best. Combinations of theoretical and experimental design techniques should be used.

1. Do not design for an excessive amount of gain around the feedback loop. Excessive gain will lead to instability and may result in the oscillator not being crystal controlled.
2. Be sure to worst case the design. A resistor may be added in series with the crystal to simulate worst case crystals. The circuit should not oscillate on any frequency with the crystal out of the circuit.
3. A quick check of oscillator peformance is to measure the frequency stability with supply voltage variations. For HCMOS gates, a change of supply voltage from 2.5 to 6 volts should result in less than 10 PPM change in frequency. Circuit value changes should be evaluated for improvements in stability.

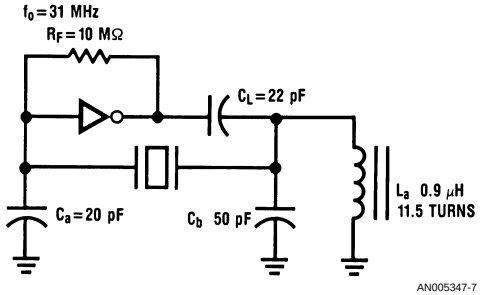


FIGURE 6. Parallel Mode Overtone Circuit

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