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High-Speed-CMOS designs address noise and I/O levels

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To maximize the benefits of high-speed CMOS, you must cope with environmental interactions and component limitations. Especially important are system noise decoupling and both transient and steady-state level control.

Designs using high-speed-CMOS logic, such as the MM54HC/74HC Series, can attain characteristics that mark improvements over LS-TTL designs. To optimize these characteristics, however, you must adopt proper design procedures. This article deals with the ICs' input-output and noise-immunity considerations.

High-speed CMOS logic is essentially a digital-IC family that combines TTL (bipolar) and CD4000 (CMOS) characteristics. Because of the family's high speed, you must be more aware of the requirements of fast systems than in the case of CD4000B logic. Although the 54HC/74HC IC's CMOS construction results in noise immunity comparable to the CD4000 family, its high speed necessitates system-grounding and supply-decoding techniques normally used in LS-TTL system design.

The following sections discuss general usage guidelines, system noise susceptibility and immunity, and the 54HC/74HC logic's power-supply-noise characteristics. Note that, unless specific exceptions are stated, the considerations discussed apply also to 54HCT/74HCT, HC's TTL-compatible subset.

FOLLOW BASIC GUIDELINES

The basic rules for designing with 54HC/74HC circuits are similar to those that apply to 74LS, CD4000B and 54C/74C devices. First, under normal static operating conditions, the input should not exceed V_{CC} or go below ground. In normal high-speed systems, transients and line ringing can cause inputs to violate this rule momentarily, forcing the ICs to enter an SCR-latch-up mode.

Latch-up results if either the input- or output-protection diodes are forward biased because of voltages above V_{CC} or below ground. As a result, the IC's internal parasitic SCR shorts V_{CC} to ground *Figure 1* shows the diodes in a CMOS IC, schematically **(a)** and in a simplified die cross section **(b)**.

Thanks to some processing refinements, SCR latch-up isn't a problem with the MM54HC/74HC Series. There are, however, limitations on the currents that the internal metallization and protection diodes can handle, so for high-level transients (pulse widths less than 20 ms and inputs above V_{CC} or below ground), you must limit the current of the IC's internal diode to 20 mA rms, 100 mA peak. Usually, a simple resistor configured in series with the input suffices.

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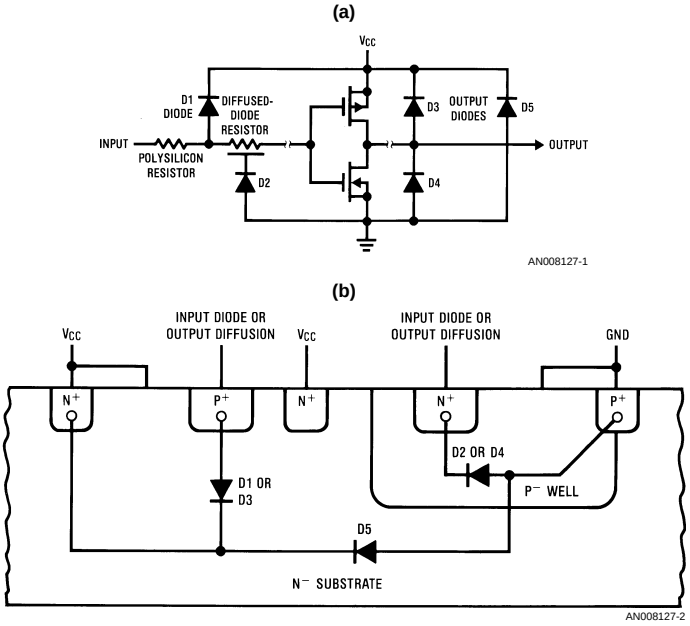

FIGURE 1. Essential but sometimes evil, the diodes in CMOS-logic ICs can be easily damaged by excessive currents. Reversed supplies or large input or output currents can cause diode burnout.

Powering the device is another important design concern. Don't power up inputs before both V_{CC} and ground are connected, and don't plug or unplug pc boards into or from powered connectors unless input currents are short lived or limited in the manner already described. Both conditions can forward bias input diodes, resulting in excessive diode currents. Again, *Figure 1* shows these diodes and the possible current paths. If these conditions are unavoidable, add external current limiting to prevent damage to 54HC/74HC circuits, or use special connectors that apply power before signals. Some family members (notably the HC4049/50) have modified input structures and can survive the application of power to the input before the supply.

Floating inputs are a frequently overlooked problem. CMOS inputs have extremely high impedance and, if left open, can float to any voltage. This situation can result in logic-function mishaps and unnecessary power consumption. Moreover, open inputs are susceptible to electrostatic damage. You should thus tie unused inputs to V_{CC} or ground, either through a resistor or directly.

Finally, for correct logic results you should use inputs with rise and fall times faster then 500 ns. Slower transition times can result in logic errors and oscillation.

OBSERVE OUTPUT RULES

You must observe certain usage rules for 54HC/74HC outputs as well as for inputs. Output voltages shouldn't exceed the supply voltage, and currents in the output diodes shouldn't exceed 20 mA. Moreover, output rms drive currents shouldn't exceed 25 mA for 4 mA standard-output devices or 35 mA for 6 mA devices. The die's metal lines dictate this limitation. Violations can result in long-term deterioration. Much larger currents (greater than 100 mA peak) arising from capacitive-load charging and line driving are normal and pose no real problem. As a rule of thumb, don't allow the output current's rms value to exceed the device's current rating. Unlike the inputs, unused outputs should be left floating to allow the output to switch without drawing any dc current.

When testing a pc board, its often necessary to short the output of one CMOS device to overdrive and force a given level on the input of the IC driven by this output. In other instances, you might need to short the outputs on a one-time basis. You can do so without degrading the IC's life if you follow a few rules. When bench testing 54HC/74HC devices, for example, you can short one output for several minutes without harm. In automatic testing, you can short as many as eight outputs for a 1-sec duration. Here again, the limitation is imposed by the metallization.

POWER-SUPPLY CAVEATS

Now that you've looked at input and output signals, give some extra attention to power-supply considerations. For instance, supply levels affect the device's logical operation. You should, for example, keep the supplies within the 2 to 6V range for HC devices and the 4.5 to 5.5V range for HCT devices. Voltages as high as 7V or as low as 0V won't harm the ICs, but their performance isn't guaranteed at these levels. However, HCs and HCTs (with the exception of one-shots and Schmitt triggers) can typically function with supplies as low as about 1.4V.

As with any IC, it's crucial that you *not* reverse the supply voltages. Doing so will forward bias a substrate diode between V_{CC} and ground (*Figure 1*), resulting in excessive currents and damage to the IC. As with inputs and outputs, don't let V_{CC} or ground rms currents exceed 50 mA for 4 mA devices or 70 mA for 6 mA units. Again, transients pose no real problem as long as their rms values stay within the devices' ratings.

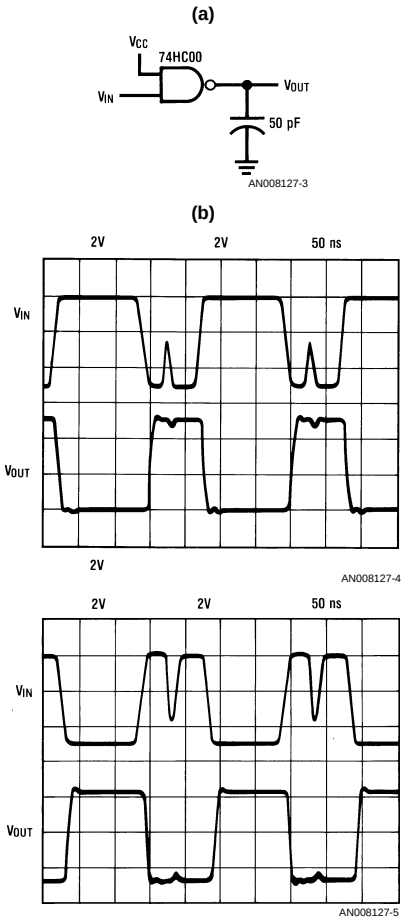

FIGURE 2. The reaction of 74HC00 gates (a) to noise spikes is clearly seen in these scope drawings. The gate exhibits noise immunity of 2V or more (b). Furthermore, the immunity is equally good for positive- and negative-going noise spikes.

UNDERSTANDING NOISE

What happens if the signals just discussed aren't clean? In digital-logic systems, "noise" is defined as extraneous voltage in the signal or supply paths. For CMOS, ECL or TTL devices, system noise that's great enough can affect the logic's integrity. CMOS-logic families such as the CD4000 and 74C are highly immune to certain types of system noise. This immunity is due mainly to the nature of CMOS, but also to the fact that the devices' slowness reduces self-induced supply noise and crosstalk and prevents the logic from responding to short externally induced or radiated transients.

However, in high-speed CMOS (which is about 10 times faster than CD4000 logic), crosstalk, induced supply noise and noise transients become factors. Higher speeds allow the device to respond more quickly to externally induced noise transients and accentuate the parasitic interconnection inductances and capacitances that increase self-induced noise and crosstalk.

Because HC-CMOS specifies input levels similar to those of CD4000 logic, its dc noise rejection is also superior to LS-TTL. And because high-speed CMOS has an output impedance one-tenth that of CD4000 devices, it's less susceptible to noise currents coupled to its outputs. As a result, lower stray voltages are induced for a given amount of current coupling.

To quantify these noise parameters, first define "noise immunity": a device's ability to prevent noise on its input from being transferred to its output. More specifically, it's the amount of voltage that can be applied to an input without causing the output to change state. For HC-CMOS, this immunity is approximately 2V; in the worst case, it's the maximum input Low or High logic levels specified in the data sheet.

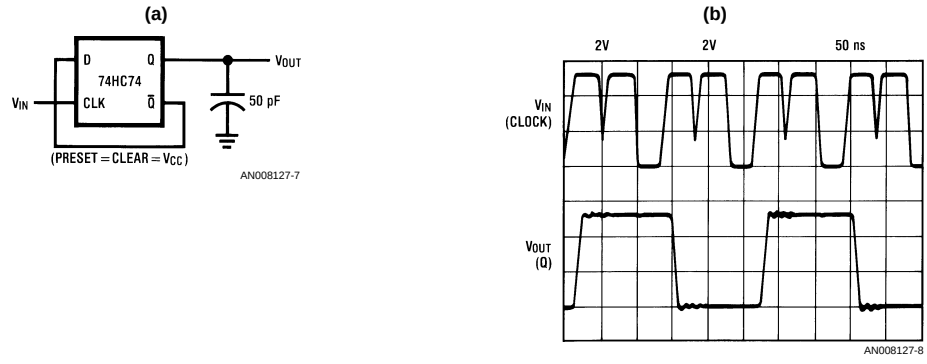

FIGURE 3. Exhibiting high clock-noise immunity, this 74HC74 flip flop (a) shows no change in output for noise spikes greater than 2V (b)

Noise immunity is an important attribute, but noise margin proves more useful because it defines the amount of noise that a system can tolerate and still maintain correct logic operation. It's defined as the difference between the output logic Low (or High) of one gate and the input logic Low (or High) of the gate the given device is driving.

For example, in HC-CMOS using a 4.5V V_{CC}, typical output levels are ground and V_{CC}, and input thresholds are V_{IH}=3.15V and V_{IL}=0.9V. These figures yield noise margins of approximately 1300 mV (logic One) and 850 mV (logic Zero). LS's noise immunity is 700 and 400 mV, respectively. Note that 54HC/74HC input levels are skewed slightly toward ground, so the ICs tolerate slightly more V_{CC} noise than ground noise.

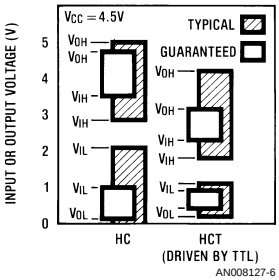

FIGURE 4. Noise margins for HC-CMOS and an HCT-CMOS-TTL combination are illustrated by this graph. You can see that the all-CMOS system exhibits the higher noise immunity.

To illustrate noise margin and immunity, *Figure 2* shows the output that results when you apply several types of simulated noise to a 74HC00's input. Typically, even 2V or more input noise produces little change in the output. *Figure 3* shows how noise affects a 74HC74's clock input. Again, no logic errors occur with 2V or more clock noise.

54HCT/74HCT ICs have an input buffer specially designed to yield TTL input levels of 0.8 and 2V. Their noise-immunity characteristics are therefore substantially different from those of 54HC/74HC devices. In evaluating these differences, note two general applications for HCT logic: in a TTL or NMOS (eg, XMOS, HOMS) system; or in an all-CMOS, HC or HCT system.

In the first case, the HCT inputs get driven by outputs that are essentially TTL and specify output levels of 0.4 and 2.4V (or 0.5 and 2.7V). In this situation, the specified noise margin is similar to the TTL margin: 400 mV for a logic Zero and either 400 or 700 mV for a logic One. These values, shown in *Figure 4*, are significantly less than those of an all-HC system.

Now examine the second case. When using HCT with HC, output logic levels are almost equal to power-supply levels. Therefore, HCT's specified noise margin is approximately 700 mV for a logic Zero and 2.4V for a logic One. At first glance, the high noise margin for Ones might seem strange, but this situation presents a tradeoff against the Zero-level margin. Compare the two gate-transfer functions in *Figure 5*; the HCT device has a logic trip point at 1.4V, while the HC gate trips at 2.4V. Thus, HC's typical performance is twice that of HCT for ground noise; for V_{CC} noise, HCT is about 50% better.

The conclusion? In a normal system (including all-CMOS systems), HC provides better noise immunity than HCT. The one case where HCT could prove more helpful is in systems that are designed with noiseless ground and dirty V_{CC}. Naturally, this design approach isn't good. A second fact highlighted by these transfer functions, HC is conservatively specified for its input and output logic levels, whereas HCT is specified more tightly. So even though data-sheet limits for HCT seem better, actual system performance indicates that HC provides better overall noise margins.

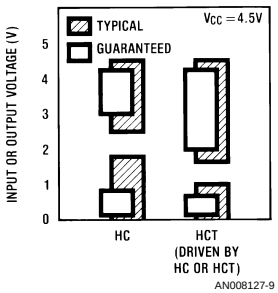

FIGURE 5. Comparing HC and HCT logic, this graph shows noise immunity of the respective families. HC wins for ground noise, HCT for V_{CC} noise.

CONSIDER SYSTEM NOISE

Now take a closer look at system noise, which you can group into several categories, depending on the source. The type of noise dictates the appropriate noise-supression technique.

- Power-supply I_{CC} noise, generated in the power-supply line, comes from logic switching in CMOS circuits.
- Transmission-line reflections, unwanted ringing and overshoot phenomena arise from signals propagating down improperly terminated transmission and signal lines.
- Signal crosstalk is caused by capacitive or inductive coupling of extraneous voltages from one signal line to another or to the power-supply line.
- Radiated noise, an RF phenomenon that originates within a high-speed-logic system, emits to other systems. It arises from the high-frequency energy emitted when logic toggles. This noise, not a major problem with regard to logic integrity, can interfere with other systems.

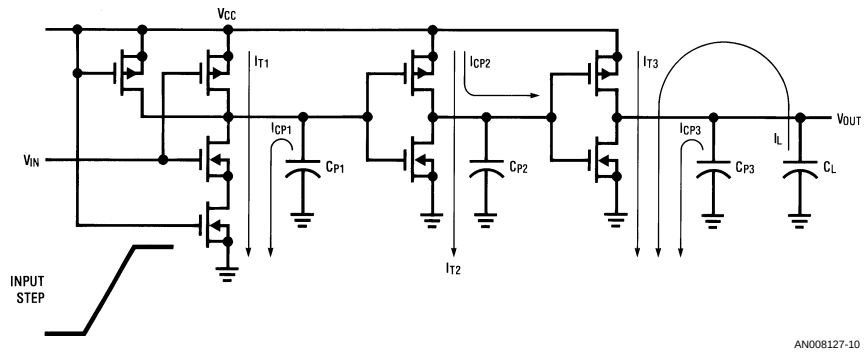

FIGURE 6. This schematic shows the currents in a 74HC00 gate that result when applying a positive input step. Also shown are the internal parasitic and external load capacitances.

Power-supply spiking is perhaps the most important contributor to system noise. When any element switches logic states, it generates a current spike that produces a voltage transient. If these transients become too large, they can cause logic errors because the supply-voltage drop upsets internal logic, or because a supply spike on one circuit's output feeds an extraneous noise voltage into the next device's input.

With CMOS logic in its quiescent state, essentially no current flows between V_{CC} and ground. But when an internal gate or an output buffer switches state, a momentary current flows from V_{CC} to ground. This current has two components: the current required to charge and discharge any stray or load capacitance, and the current that flows directly from V_{CC} to ground when the p- and n-channel transistors turn on momentarily during an input transition.

Figure 6 shows the paths for these current components within a 74HC00 upon application of a positive step to the device's input. C_{P1}, C_{P2}, and C_{P3} represent the internal parasitic capacitances; C_L is the external load capacitance. I_{T1}, I_{T2} and I_{T3} correspond to the currents that flow through both the n- and p-channel transistors during switching. I_{CP1}, I_{CP2} and I_{CP3} are the charging currents for the capacitances.

The switching transient caused by an unloaded output changing state typically equals 40 mA peak. *Figure 7b* shows the current and voltage spikes resulting from switching a single unloaded NAND gate. *Figure 7c* through *(e)* show the current spike's increase due to the addition of 15-, 50- and 100-pF loads. The large amount of ringing results from the test circuit's transmission-line effects.

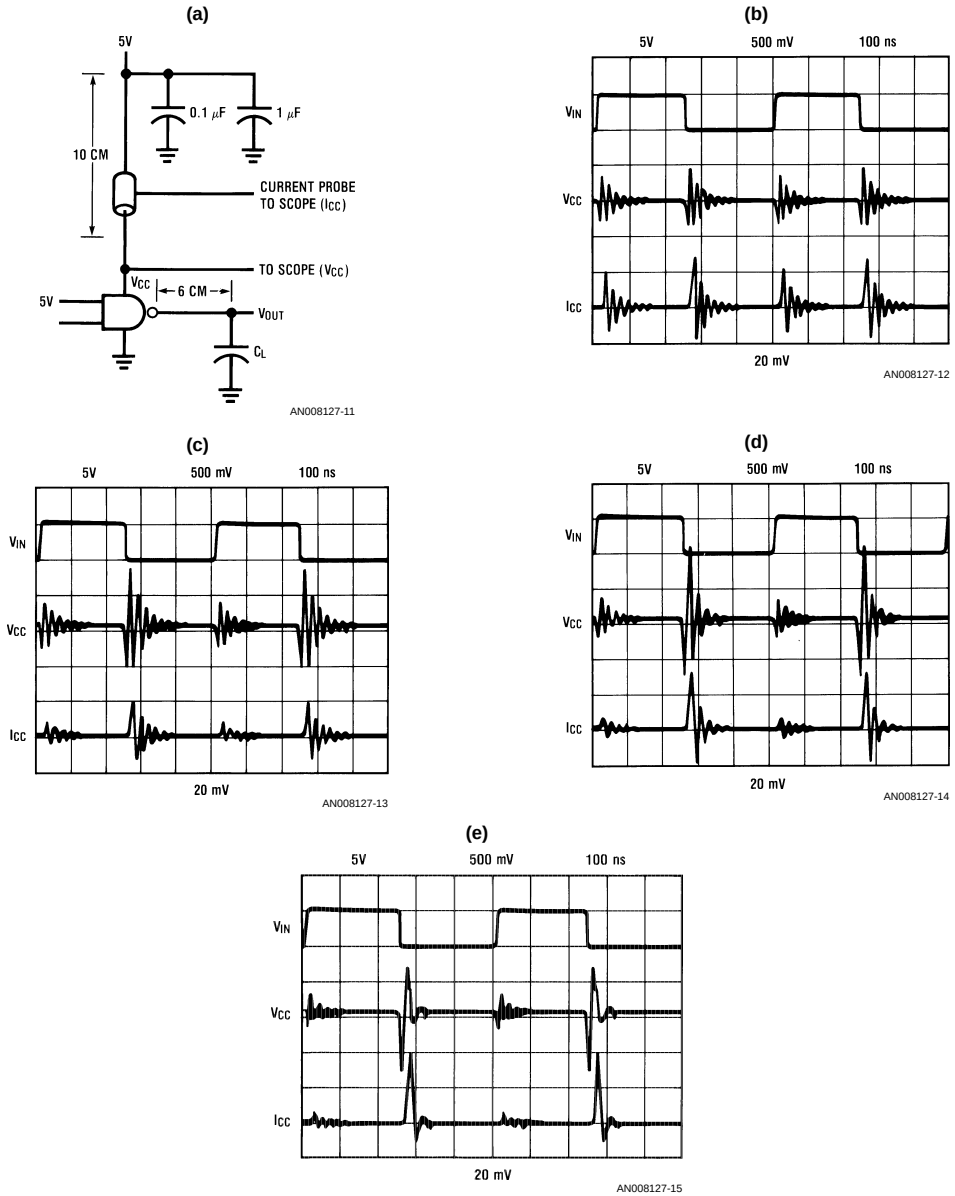

FIGURE 7. The effects of capacitive loads are seen in these drawings; (b) through (e) show the spikes resulting with no load and with 15-, 50- and 100-pF loads, respectively. The ringing arises from the test circuit's transmission-line effects.

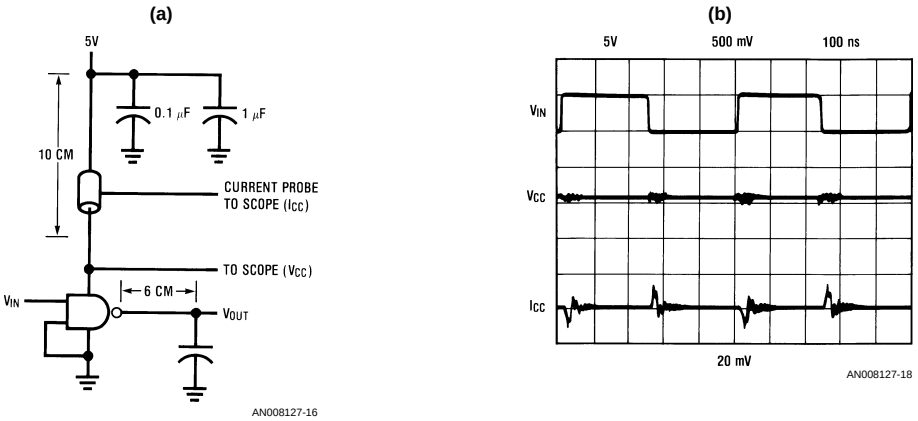

FIGURE 8. On-chip circuitry before a 74HC00's output stage (a) generates little current spiking, as shown in the drawing (b). In the test circuit, one input is switching (but not the output). Note the very small power-supply glitches provoked by the input-circuit transitions.

This ringing occurs partly because the CMOS gate switches from a very high impedance to a very low one and back again. Note that, even for medium-size loads, load-capacitance current becomes a major current contributor, verified by the dramatic increase in current from the unloaded to the 100-pF-load case.

Although internal logic generates current spikes when switching, the bulk of a spike's current comes from output-circuit transitions. Why? Because the outputs have the largest p- and n-channel currents and the greatest parasitic and load capacitances. *Figure 8* shows the I_{CC} current for a 74HC00 gate with one input switching, the other at ground (thus, with no output transitions).

The best way to reduce noise-voltage transients is to implement good power-supply busing. You should maintain a low ac impedance from each circuit's V_{CC} to ground. In one model for a supply bus (*Figure 9*), both V_{CC} and ground traces exhibit inductances, resistances and capacitances. To reduce voltage transients, keep the supply line's parasitic inductances as low as possible by reducing trace lengths, using wide traces, ground planes, strip-line or microstrip transmission-line techniques and by decoupling the supply with bypass capacitors.

For effective supply decoupling, bypass capacitors must supply the charge required by the current spike for its duration with minimal voltage change. You can determine a bypass capacitor's approximate value from the expression:

$$C_{BYPASS} = \frac{Idt}{dV} = \frac{(SPIKE\ CURRENT)\ (SPIKE\ DURATION)}{(ALLOWABLE\ DROOP\ VOLTAGE)}$$

Consider this example: A typical MM54HC/74HC has an I_{CC} transient of about 20 mA, lasting approximately 20 ns (excluding ringing). If you allow 400 mV peak noise, the required bypass capacitance is about (20 mA)(20 ns)/0.4V=1 nF per output.

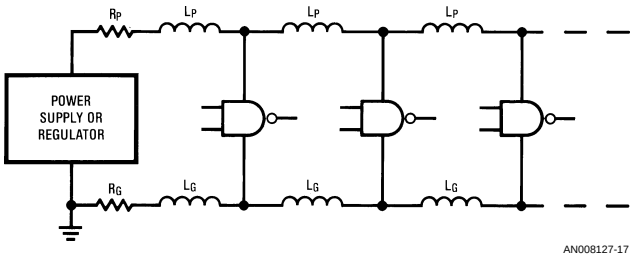

FIGURE 9. This equivalent circuit for a power-supply bus emphasizes both the V_{CC}'s and the ground's series inductances.Try to minimize these inductances through careful circuit layout.

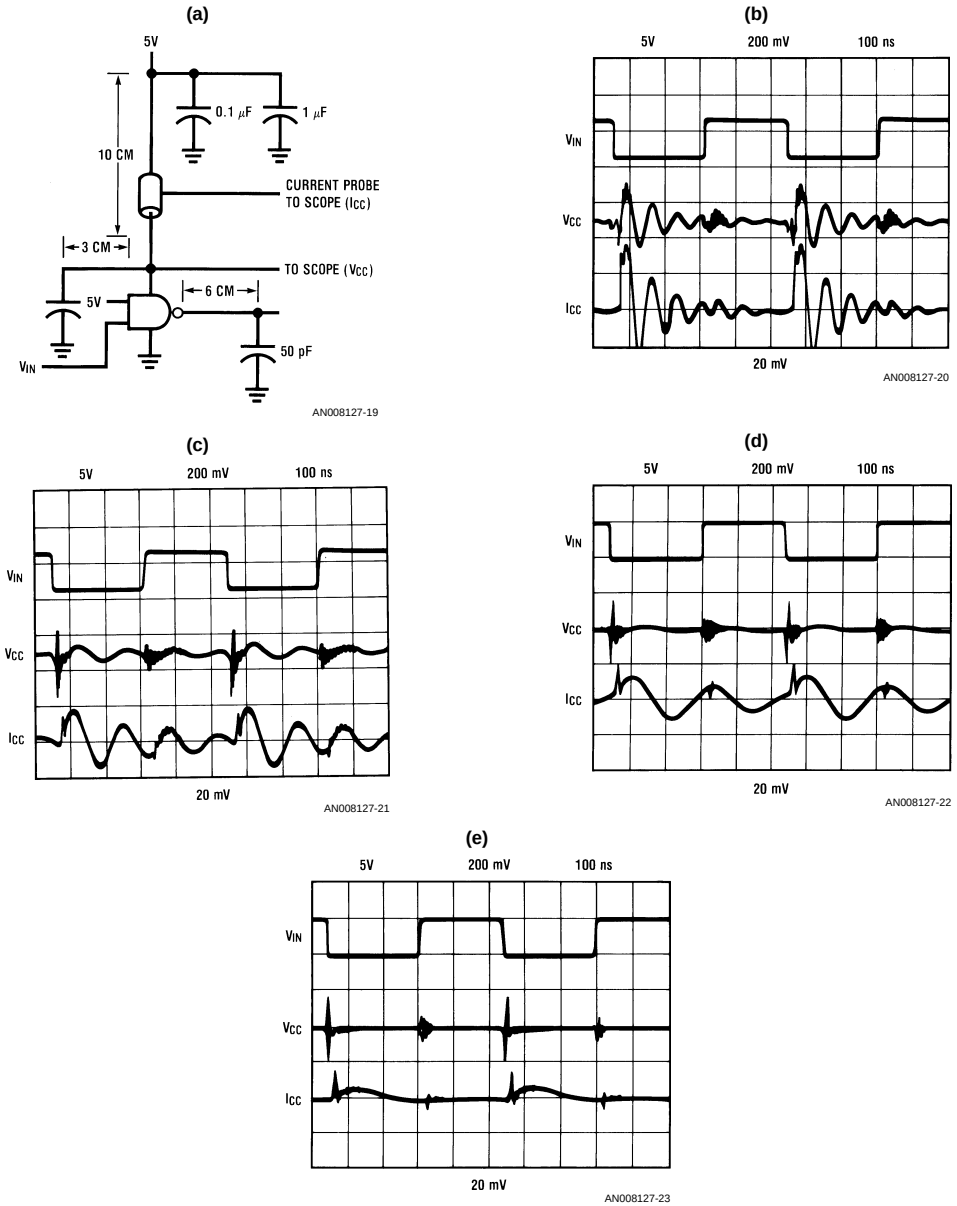

FIGURE 10. Demonstrating the importance of bypassing, drawings (b) through (e) show power-supply transients that occur when a 74HC00 is decoupled with 1-, 4.7-, 10- and 100-nF capacitors, respectively.

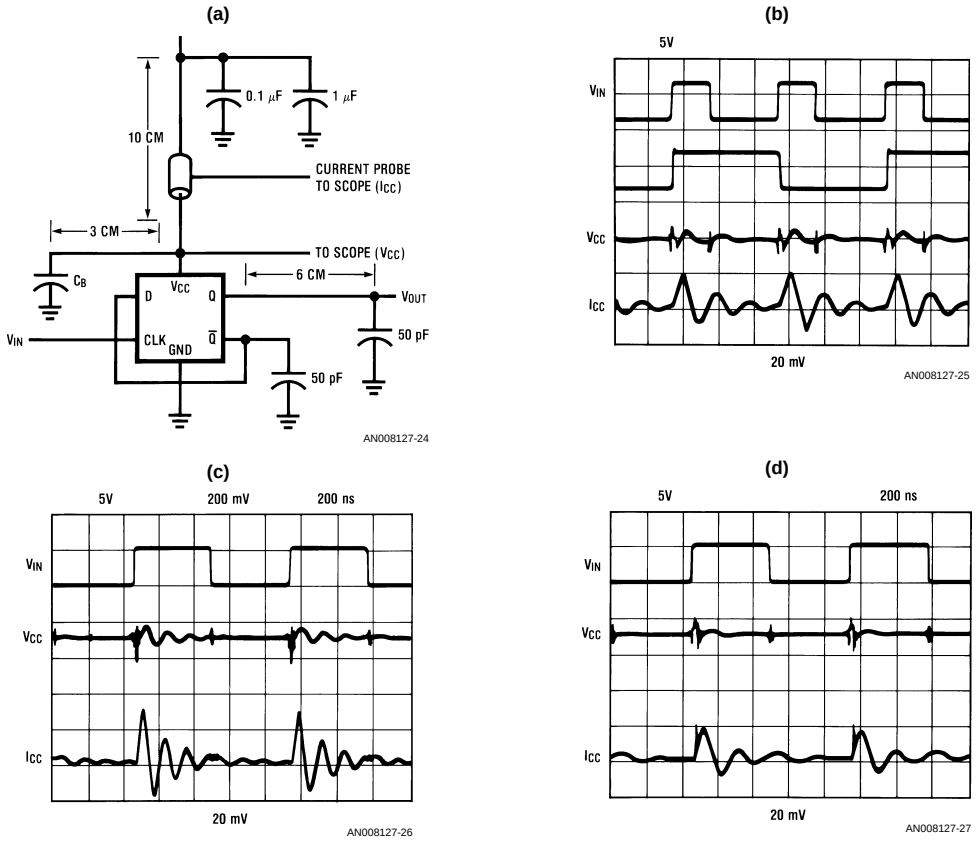

FIGURE 11. Showing results similar to those depicted in *Figure 10*, these drawings show the effects of bypassing a 74HC74 flip flop with capacitors of 1 (b) to 10 nF (d). You can see that the 10 nF bypass yields supply spiking approximately 40% lower than that of the 1-nF capacitor.

In order to prevent additional voltage spiking, this local bypass capacitor must exhibit low inductive reactance. You should therefore use high-frequency ceramic capacitors and place them very near the IC to minimize wiring inductance. The approximate amount of tolerable inductance is given by:

$$L_{SUPPLY} = \frac{Vdt}{di} =$$

$$\frac{\text{(SPIKE VOLTAGE) (SPIKE RISE OR FALL TIME)}}{\text{(SPIKE CURRENT)}}$$

For example, restricting the inductive noise spike to 100 mV peak with 20 mA current and 4 ns rise time yields (0.4V)(4 ns)/20 mA=80 nH max. Note that, in addition to localized decoupling of very fast transients, you also need bulk decoupling of spikes generated by the board's ICs. To decouple, provide a high-value capacitor for smoothing long time periods.

To show how decoupling affects supply noise in real-world situations, *Figure 10* depicts the power-supply transients that result when you choose different values of decoupling capacitors. In this example, one gate of a 74HC00 toggles, and 1-, 4.7-, 10- and 100-nF capacitors have approximately 10 cm of wiring between them and the supply. *Figure 11* presents similar results, obtained with the 74HC74 circuit. Note in both cases (although the unbypassed situation isn't depicted) that a 1 nF capacitor greatly reduces the voltage transient.

Based on empirical and theoretical considerations, you can determine a set of guidelines. These practical maxims serve only as a foundation for a system that should yield good results. Consequently, there's some leeway in following them for particular designs. As a rule of thumb, it's generally good design practice to restrict both V_{CC} and ground noise to less than 250 mV.

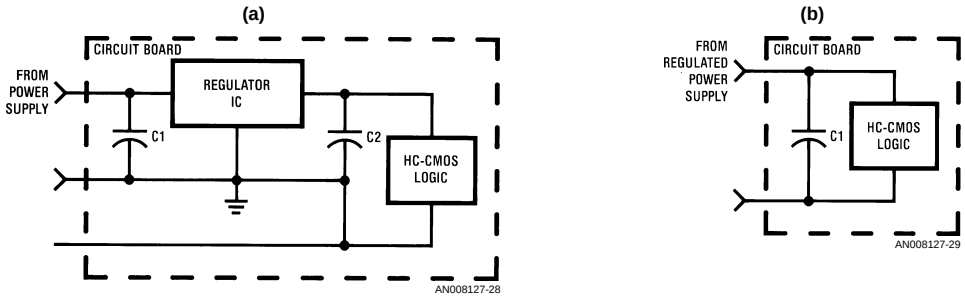

FIGURE 12. Tailor bypassing to the system's supply scheme. Circuit diagram (a) shows the method to use with local regulators; (b) shows the scheme to adopt with a centralized regulated supply. Use tantalum- or aluminum-electrolytic capacitors.

Before presenting the guidelines, examine some comparative attributes of earlier CMOS, HC, HCT and LS-TTL devices. First, because of higher speeds and larger output currents, the supply-bypassing requirements of HC devices are more rigorous than those of earlier metal-gate-CMOS ICs. Compared with those of LS-TTL, the requirements for HC/HCT are similar or a little more stringent, depending on the application.

Furthermore, for random logic, 54HC/74HC and 54LS/74LS are similar, but in bus-driving applications HC devices can produce larger spikes. Finally, HCT logic needs better grounding than HC logic. In fact, its design considerations closely follow those of LS-TTL. However, as with HC, HCT exhibits greater V_{CC} spiking in bus-driving applications.

Now you're ready for the guidelines:

- Keep V_{CC}-bus routing short. When using double-sided or multilayer circuit boards, use strip-line, transmission-line or ground-plane techniques.
- Keep ground lines short, and on pc boards make them as wide as possible, even if trace width varies. Use separate ground traces to supply high-current devices such as relay and transmission-line drivers.
- In systems mixing linear and logic functions and where supply noise is critical to the analog components' performance, provide separate supply buses or even separate supplies.
- If you use local regulators, bypass their inputs with a tantalum capacitor of at least 1 µF (*Figure 12a*), and bypass their outputs with a 10- to 50-µF tantalum- or alumium-electrolytic capacitor *(b)*.
- If the system uses a centralized regulated power supply, use a 10- to 20-µF tantalum-electrolytic capacitor or a 50- to 100-µF aluminum-electrolytic capacitor to decouple the V_{CC} bus connected to the circuit board (*Figure 12b*).
- Provide localized decoupling. For random logic, a rule of thumb dictates approximately 10 nF (spaced within 12 cm) per every two to five packages, and 100 nF for every 10 packages. You can group these capacitances, but it's more effective to distribute them among the ICs. If the design has a fair amount of synchronous logic with outputs that tend to switch simultaneously, additional decoupling might be advisable. Octal flip flops and buffers in bus-oriented circuits might also require more decoupling. Note that wire-wrapped circuits can require more decoupling than ground-plane or multilayer pc boards.
- For circuits that drive transmission lines or large capacitive loads (µP buses, for example), use a 10 nF ceramic capacitor close to the devices' supply pins.
- Finally, terminate transmission-line grounds near the drivers.

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