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1. Introduction

Compared to conventional hard-switched converters with fixed switching frequencies, the quasi-resonant converter (QRC) topology is a very attractive alternative for power supply designers. The increasing popularity of the QRC approach is based on its ability to reduce electromagnetic interference (EMI) while increasing power conversion efficiency.

The FSQ-series FPS™ (Fairchild Power Switch) is an integrated Pulse Width Modulation (PWM) controller and Sense FET specifically designed for quasi-resonant off-line Switch Mode Power Supplies (SMPS) with minimal external components. Figure 1 shows the internal block diagram of the FSQ-series. Compared with discrete MOSFET and PWM controller solution, it can reduce total cost, component count, size and weight, while simultaneously increasing efficiency, productivity, and system reliability. The FSQ-series employs an advanced control technique that allows converter to operate with narrow frequency variation, while keeping the quasi-resonant operation. When the converter operates in discontinuous conduction mode (DCM), the controller finds the valley of the drain voltage and turns on the MOSFET at the minimum drain voltage. Meanwhile, the converter can operate with fixed frequency when operating in continuous conduction mode (CCM), which allows converter design as simple as conventional PWM converters.

This application note presents practical design considerations of a flyback converter employing the FSQ-series FPS™. It covers designing the transformer, output filter, and sync network; selecting the components; and closing the feedback loop.
2. Operation principle of Quasi-resonant flyback converter

Quasi resonant flyback converter topology can be derived from a conventional square wave, pulse-width-modulated (PWM) flyback converter without adding additional components. Figure 2 shows the simplified circuit diagram of a quasi-resonant flyback converter and its typical waveforms. The basic operation principles are:

- During the MOSFET ON time ($t_{ON}$), input voltage ($V_{IN}$) is applied across the primary-side inductor ($L_m$). Then, MOSFET current ($I_{ds}$) increases linearly from zero to the peak value ($I_{pk}$). During this time, the energy is drawn from the input and stored in the inductor as much as $L_m \times I_{pk}^2/2$.

- When the MOSFET is turned off, the energy stored in the inductor forces the rectifier diode (D) to turn on. During the diode ON time ($t_D$), the output voltage ($V_o$) is applied across the secondary-side inductor and the diode current ($I_D$) decreases linearly from the peak value ($I_{pk} \times N_p/N_s$) to zero. At the end of $t_D$, all the energy stored in the inductor has been delivered to the output. During this period, the output voltage is reflected to the primary side as $V_o \times N_p/N_s$. The sum of input voltage ($V_{IN}$) and the reflected output voltage ($V_o \times N_p/N_s$) is imposed on the MOSFET.

- When the diode current reaches zero, the drain-to-source voltage ($V_{ds}$) begins to oscillate by the resonance between the primary-side inductor ($L_m$) and the MOSFET output capacitor ($C_{oss}$) with an amplitude of $V_o \times N_p/N_s$ on the offset of $V_{IN}$, as depicted in Figure 2. Quasi-resonant switching is achieved by turning on the MOSFET when $V_{ds}$ reaches its minimum value. Doing this reduces the MOSFET turn-on switching loss caused by the capacitance loading between the drain and source of MOSFET. If the transformer is designed so that the resonance amplitude is larger than $V_{IN}$ by increasing the turns ratio, $N_p/N_s$, "Zero-Voltage-Switching (ZVS)" of the MOSFET is achieved.

Other than turning on the MOSFET with minimum drain-to-source voltage, a quasi-resonant converter provides "soft" switching conditions to the switching devices. The MOSFET turns on at zero current and the diode turns off at zero current. This soft switching not only reduces the switching losses, but also lowers the switching noise caused by diode reverse recovery.

The major drawback of applying a quasi-resonant converter topology is that it causes the switching frequency to increase as the load decreases and/or input voltage increases. As the load decreases and/or input voltage increases, the MOSFET ON time ($t_{ON}$) diminishes and, therefore, the switching frequency increases. This results in severe switching losses, as well as intermittent switching and audible noise. Due to these problems, the conventional quasi-resonant converter topology has limitations for applications with wide input and load ranges.

3. Control Method of FSQ-Series

To overcome the frequency increase problem at light load, FSQ-series employs an advanced control technique illustrated in Figure 3 with typical switching waveforms. Once the MOSFET is turned on, the next turn-on is prohibited during the blanking time ($t_B$). After the blanking time, the controller finds the valley within the detection time window ($t_W$) and turns on the MOSFET when $V_{ds}$ reaches its minimum value. The controller turns on the MOSFET  at the valley within $t_W$. Accordingly, the switching frequency is limited between 55kHz and 67kHz, as shown in Figure 3 and 4. This allows converter design as simple as in conventional PWM converters.
4. Step-by-step Design Procedure

This section provides a step-by-step design process, illustrated in the design flow chart of the Figure 5. Figure 6 shows the basic schematic of quasi-resonant flyback converter using FSQ-series, which also serves as a reference circuit for the design process described.

![Figure 3. Switching Waveforms of FSQ-Series for Different Input Voltages](image)

**Figure 3. Switching Waveforms of FSQ-Series for Different Input Voltages**

![Figure 4. Frequency Variation as Input Voltage Varies](image)

**Figure 4. Frequency Variation as Input Voltage Varies**

![Figure 5. Flow Chart of Design Procedure](image)

**Figure 5. Flow Chart of Design Procedure**

1. Determine the system specifications 
   \( (V_{\text{line min}}, V_{\text{line max}}, f_L, P_o, E_p) \)

2. Determine DC link capacitor (\(C_{DC}\)) and calculate DC link voltage range

3. Determine the reflected output voltage \( (V_{RO}) \)

4. Determine the transformer primary side inductance (\(L_p\))

5. Choose proper FPS considering input power and \( I_{ds\, \text{peak}} \)

6. Determine the proper core and the minimum primary turns (\(N_{p\, \text{min}}\))

7. Determine the number of turns for each output and Vcc auxiliary circuit

8. Determine the wire diameter for each winding

9. Is the winding window area (\(A_w\)) enough?
   - Yes
   - No

10. Is it possible to change the core?
    - Yes
    - No

11. Choose the secondary side rectifier diodes

12. Determine the output capacitors

13. Design the Snubber network

14. Design the synchronization network

15. Design the feedback control circuit

Design finished
[STEP-1] Define the System Specifications

When designing a power supply the following specifications should be determined first:

- Line voltage range ($V_{\text{line min}}$ and $V_{\text{line max}}$).
- Line frequency ($f_L$).
- Maximum output power ($P_o$).
- Estimated efficiency ($E_{\text{ff}}$): The power conversion efficiency must be estimated to calculate the maximum input power. If no reference data is available, set $E_{\text{ff}} = 0.7$~$0.75$ for low-voltage output applications and $E_{\text{ff}} = 0.8$~$0.85$ for high-voltage output applications. With the estimated efficiency, the maximum input power is given by:

$$P_{\text{in}} = \frac{P_o}{E_{\text{ff}}} \quad \text{(EQ 1)}$$

For multiple output SMPS, the load occupying factor for each output is defined as:

$$K_{L(n)} = \frac{P_{o(n)}}{P_o} \quad \text{(EQ 2)}$$

where $P_{o(n)}$ is the maximum output power for the n-th output. For single output SMPS, $K_{L(1)} = 1$. It is assumed that $V_o$ is the reference output that is regulated by the feedback control in normal operation, as shown in Figure 6.

[STEP-2] Determine DC Link Capacitor ($C_{\text{DC}}$) Value and Calculate the DC Link Voltage Range

In offline SMPS applications, a crude DC voltage ($V_{\text{DC}}$) is obtained first on the DC link capacitor ($C_{\text{DC}}$) by rectifying the AC mains. Then, the crude DC voltage is converted into pure DC outputs. Typically, the DC link capacitor is selected as 2-3µF per watt of input power for universal input range (85~265Vrms) and 1µF per watt of input power for European input range (195~265Vrms). With the DC link capacitor selected, the minimum DC link voltage is obtained as:

$$V_{\text{DC min}} = \frac{2 \cdot (V_{\text{line min}})^2 - P_{\text{in}} \cdot (1 - D_{\text{ch}})}{C_{\text{DC}} \cdot f_L} \quad \text{(EQ 3)}$$

where $C_{\text{DC}}$ is the DC link capacitor value; $D_{\text{ch}}$ is the duty cycle ratio for $C_{\text{DC}}$ to be charged as defined in Figure 7, which is typically about 0.2; $P_{\text{in}}$, $V_{\text{line min}}$ and $f_L$ are specified in STEP-1.

The maximum DC link voltage is given as:

$$V_{\text{DC max}} = \sqrt{2} V_{\text{line max}} \quad \text{(EQ 4)}$$

where $V_{\text{line max}}$ is specified in STEP-1.
[STEP-3] Determine the Reflected Output Voltage ($V_{RO}$)

Figure 8 shows typical waveforms of the drain voltage of quasi-resonant flyback converter. When the MOSFET is turned off, the DC link voltage ($V_{DC}$), together with the output voltage reflected to the primary ($V_{RO}$), is imposed on the MOSFET. The maximum nominal voltage across the MOSFET ($V_{ds,\text{nom}}$) is:

$$V_{ds,\text{nom}} = V_{DC}^{\text{max}} + V_{RO} \quad (\text{EQ 5})$$

where $V_{DC}^{\text{max}}$ is as specified in Equation 4. As shown in Figure 8, the capacitive switching loss of the MOSFET can be reduced by increasing $V_{RO}$. However, this increases the voltage stress on the MOSFET. Therefore, $V_{RO}$ should be determined by a trade-off between the voltage margin of the MOSFET and the efficiency. It is typical to set $V_{RO}$ as 60–90V so that $V_{ds,\text{nom}}$ is 430–460V (65–70% of MOSFET rated voltage).

![DC link voltage waveform](image)

**Figure 7. DC Link Voltage Waveform**

[STEP-4] Determine the Transformer Primary-Side Inductance ($L_m$)

The conventional quasi-resonant converter employs a variable frequency control, which makes the optimum design of the magnetic components difficult. However, FSQ-series can operate in both CCM and DCM with near constant switching frequency thanks to the advanced control technique, which allows engineers to use the conventional transformer design procedure of PWM converters.

In respect of EMI, DCM operation is preferred since the MOSFET is turned on at the minimum drain voltage and the secondary-side diode is softly turned off when operating in DCM. The transformer size can be reduced when using DCM because the average energy storage is low compared to CCM. However, DCM inherently causes higher RMS current, which increases the conduction loss of the MOSFET and the current stress on the output capacitors. When considering efficiency as well as magnetic components size, it is typical to design the converter to operate in CCM for low input voltage condition and in DCM for high input voltage condition.

The transformer primary side inductance is determined for the minimum input voltage and full-load condition. Once the reflected output voltage ($V_{RO}$) is determined in STEP-3, the flyback converter can be simplified, as shown in Figure 9, by neglecting the voltage drops in MOSFET and diode. The design rules are a bit different for CCM and DCM.

**CCM Design:** When designing a converter to operate in CCM at full load and minimum input voltage condition, the maximum duty ratio is given by:

$$D_{\text{max}} = \frac{V_{RO}}{V_{RO} + V_{DC}^{\text{min}}} \quad (\text{EQ 6})$$

where $V_{DC}^{\text{min}}$ and $V_{RO}$ are specified in Equation 3 and STEP-3, respectively.

With $D_{\text{max}}$, the primary-side inductance ($L_m$) of the transformer is obtained as:

$$L_m = \frac{(V_{DC}^{\text{min}} - D_{\text{max}}^2)}{2P_{in}f_sK_{RF}} \quad (\text{EQ 7})$$

where $V_{DC}^{\text{min}}$ is specified in Equation 3, $P_{in}$ is specified in STEP-1, $f_s$ is the free-running switching frequency of the FPS device, and $K_{RF}$ is the ripple factor, shown in Figure 9. The ripple factor is closely related to the transformer size and the RMS value of the MOSFET current. It is typical to set $K_{RF} = 0.5-0.7$ for the universal input range.

**DCM Design:** When designing the converter to operate in DCM at full load and minimum input voltage condition, the maximum duty ratio should be chosen as smaller than the value obtained in Equation 6, as shown in Figure 9:

$$D_{\text{max}} < \frac{V_{RO}}{V_{RO} + V_{DC}^{\text{min}}} \quad (\text{EQ 8})$$

Since reducing $D_{\text{max}}$ increases the conduction loss in
MOSFET, too small $D_{\text{max}}$ should be avoided. Once $D_{\text{max}}$ is determined, the primary-side inductance ($L_m$) of the transformer is obtained as:

$$L_m = \frac{\left(\frac{V_{\text{DC}}}{V_{\text{DC}_{\text{min}}}}\right)^2 D_{\text{max}}}{2P_{\text{in}}f_s} \quad (\text{EQ} \ 9)$$

where $V_{\text{DC}_{\text{min}}}$ is specified in Equation 3, $P_{\text{in}}$ is specified in STEP-1, and $f_s$ is the free-running switching frequency of the FPS device.

Once $L_m$ is determined, the maximum peak current and RMS current of the MOSFET in minimum-input and full-load condition are obtained by:

$$I_{d_{\text{peak}}} = I_{E\text{DC}} + \frac{\Delta I}{2} \quad (\text{EQ} \ 10)$$

$$I_{d_{\text{rms}}} = \sqrt{\frac{3}{2}}(I_{E\text{DC}})^2 + \left(\frac{\Delta I}{2}\right)^2 \frac{D_{\text{max}}}{3} \quad (\text{EQ} \ 11)$$

$$I_{E\text{DC}} = \frac{P_{\text{in}}}{V_{\text{DC}_{\text{min}}} D_{\text{max}}} \quad (\text{EQ} \ 12)$$

$$\Delta I = \frac{V_{\text{DC}_{\text{min}}} D_{\text{max}}}{L_m f_s} \quad (\text{EQ} \ 13)$$

where $P_{\text{in}}$, $V_{\text{DC}_{\text{min}}}$, $D_{\text{max}}$, and $L_m$ are specified in Equations 1, 3, 6, and 7, respectively, and $f_s$ is the FPS free-running switching frequency.

[STEP-5] Choose the Proper FPS Considering Input Power and Peak Drain Current

With the resulting maximum peak drain current of the MOSFET ($I_{d_{\text{peak}}}$) from Equation 10, choose the proper FPS for which the pulse-by-pulse current limit level ($I_{LIM}$) is higher than $I_{d_{\text{peak}}}$. Since FPS has ±12% tolerance of $I_{LIM}$, there should be some margin in choosing the FPS device.

[STEP-6] Determine the Proper Core and the Minimum primary Turn

The initial selection of the core is bound to be crude since there are too many variables. One way to select the proper core is to refer to the manufacturer's core selection guide. If there is no reference, use Table 1 as a starting point. The core recommended in Table 1 is typical for the universal input range, 55kHz switching frequency, and single-output application. When the input voltage range is 195-265 V AC or the switching frequency is higher than 55kHz, a smaller core can be used. For an application with multiple outputs, a larger core than recommended in the table should usually be used.

With the chosen core, calculate the minimum number of turns for the transformer primary side to avoid the core saturation with the following:

$$N_{p_{\text{min}}} = \frac{L_m I_{LIM}}{B_{\text{sat}} A_e} \times 10^6 \text{ (turns)} \quad (\text{EQ} \ 14)$$

where $L_m$ is specified in Equation 7, $I_{LIM}$ is the FPS pulse-by-pulse current limit level, $A_e$ is the cross-sectional area of the core in mm$^2$, as shown in Figure 10, and $B_{\text{sat}}$ is the saturation flux density in tesla. Figure 11 shows the typical characteristics of ferrite core from TDK (PC40). Since the saturation flux density ($B_{\text{sat}}$) decreases as the temperature goes high, the high temperature characteristics should be considered. ±12% tolerance of $I_{LIM}$ should be considered.

If there is no reference data, use $B_{\text{sat}} = 0.3\text{–}0.35$ T. Since the MOSFET drain current exceeds $I_{d_{\text{peak}}}$ and reaches $I_{LIM}$ in a transition or fault condition, $I_{LIM}$ is used in Equation 14 instead of $I_{d_{\text{peak}}}$ to prevent core saturation during transition.
Figure 11. Typical B-H Characteristics of Ferrite Core (TDK/PC40)

![Magnetization Curves](https://example.com/magnetization.png)

**Material:** PC40

- 25°C: B = 0.5 T
- 60°C: B = 0.4 T
- 100°C: B = 0.3 T
- 120°C: B = 0.2 T

**Flux density B (mT)**

- 0 to 1600 A/m

**Magnetic field H (A/m)**

**Material:** PC40

**Table 1. Core Quick selection Table (for Universal Input Range, fs=55kHz and Single Output)**

<table>
<thead>
<tr>
<th>Output Power</th>
<th>El Core</th>
<th>EE Core</th>
<th>EPC Core</th>
<th>EER Core</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-10W</td>
<td>EI12.5</td>
<td>EE8</td>
<td>EPC10</td>
<td>EER</td>
</tr>
<tr>
<td></td>
<td>EI16</td>
<td>EE10</td>
<td>EPC13</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EI19</td>
<td>EE13</td>
<td>EPC17</td>
<td></td>
</tr>
<tr>
<td>10-20W</td>
<td>EI22</td>
<td>EE19</td>
<td>EPC19</td>
<td></td>
</tr>
<tr>
<td>20-30W</td>
<td>EI25</td>
<td>EE22</td>
<td>EPC25</td>
<td>EER25.5</td>
</tr>
<tr>
<td>30-50W</td>
<td>EI28</td>
<td>EE25</td>
<td>EPC30</td>
<td>EER28</td>
</tr>
<tr>
<td>50-70W</td>
<td>EI35</td>
<td>EE30</td>
<td>EER28L</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 12. Simplified Diagram of the Transformer**

**[STEP-7] Determine the Number of Turns for Each Output**

Figure 12 shows the simplified diagram of the transformer. First, determine the turns ratio \( n \) between the primary side and the feedback-controlled secondary side as a reference.

\[
 n = \frac{N_p}{N_{s1}} = \frac{V_{RO}}{V_{O1} + V_{F1}} \tag{EQ 15}
\]

where \( N_p \) and \( N_{s1} \) are the number of turns for primary side and reference output, respectively, \( V_{o1} \) is the output voltage and \( V_{F1} \) is the diode \( (D_{RI}) \) forward voltage drop of the reference output.

Then, determine the proper integer for \( N_{s1} \) so that the resulting \( N_p \) is larger than the \( N_p^{min} \) obtained from Equation 14. The number of turns for the other output \( (n\text{-th output}) \) is determined by:

\[
 N_{s(n)} = \frac{V_{O(n)} + V_{F(n)}}{V_{O1} + V_{F1}} \cdot N_{s1} \quad \text{(turns)} \tag{EQ 16}
\]

The number of turns for \( V_{cc} \) winding is determined as:

\[
 N_a = \frac{V_{cc}^{\star} + V_{Fa}}{V_{O1} + V_{F1}} \cdot N_{s1} \quad \text{(turns)} \tag{EQ 17}
\]

where \( V_{cc}^{\star} \) is the nominal value of the supply voltage of the FPS device and \( V_{Fa} \) is the forward voltage drop of \( D_a \) as defined in Figure 12. It is typical to set \( V_{cc}^{\star} \leq 3\text{~}4 \text{~V} \) below \( V_{cc} \) maximum rating (refer to the datasheet).

With the determined turns of the primary side, the gap length of the core is obtained as:

\[
 G = 0.4 \times \pi A_e \left( \frac{N_p^2}{10^9 L_m} - \frac{1}{A_L} \right) \quad \text{(mm)} \tag{EQ 18}
\]

where \( A_L \) is the AL-value with no gap in nH/turns\(^2\); \( A_e \) is the cross-sectional area of the core in mm\(^2\), as shown in Figure 10; \( L_m \) is specified in Equation 7; and \( N_p \) is the number of turns for the primary-side of the transformer.
[STEP-8] Determine the Wire Diameter for Each Winding Based on the rms Current of Each Output

The rms current of the n-th secondary winding is obtained as:

\[ I_{sec(n)}^{rms} = I_{ds}^{rms} \sqrt{\frac{1-D_{max}}{D_{max}}} \frac{V_{RO} \cdot K_{L(n)}}{(V_{o(n)} + V_{F(n)})} \] (EQ 19)

where \( V_{RO} \) and \( I_{ds}^{rms} \) are specified in STEP-3 and Equation 11, respectively; \( V_{o(n)} \) is the output voltage of the n-th output; \( V_{F(n)} \) is the diode \( (D_{R(n)}) \) forward voltage drop; \( D_{max} \) is specified in Equation 6; and \( K_{L(n)} \) is the load-occupying factor for n-th output defined in Equation 2.

The current density is typically 5A/mm² when the wire is greater than 1m long. When the wire is short, with a small number of turns, a current density of 6-10 A/mm² is also acceptable. Avoid using wire with a diameter larger than 1mm to avoid severe eddy current losses and to make winding easier.

For high current output, it is better to use parallel windings with multiple strands of thinner wire to minimize skin effect.

Verify that if the winding window area of the core, \( A_w \), is enough to accommodate the wires (refer to Figure 10). The required winding window area \( (A_{wr}) \) is given by:

\[ A_w = A_c^{WR} \] (EQ 20)

where \( A_c \) is the actual conductor area and \( K_F \) is the fill factor. Typically the fill factor is 0.2–0.25 for single-output application and 0.15–0.2 for multiple outputs application.

If the required window \( (A_{wr}) \) is larger than the actual window area \( (A_w) \), go back to STEP-6 and increase the core. If it is impossible to change the core due to cost or size constraints and the converter is designed for CCM and the winding window \( (A_w) \) is slightly insufficient, go back to STEP-4 and reduce \( L_m \) by increasing the ripple factor \( (K_{RF}) \). The minimum number of turns for the primary \( (N_p^{min}) \) of Equation 14 decreases, which results in the reduced required winding area \( (A_{wr}) \).


The maximum reverse voltage and the rms current of the rectifier diode \( (D_{R(n)}) \) of the n-th output are obtained as:

\[ V_{D(n)} = V_{o(n)} + \frac{V_{DC}^{max} \cdot (V_{o(n)} + V_{F(n)})}{V_{RO}} \] (EQ 21)

\[ I_{D(n)}^{rms} = I_{ds}^{rms} \sqrt{\frac{1}{1-D_{max}}} \sqrt{\frac{V_{DC}^{min}}{V_{RO}} \cdot \frac{K_{L(n)}}{(V_{o(n)} + V_{F(n)})}} \] (EQ 22)

where \( K_{L(n)} \), \( V_{DC}^{max} \), \( V_{RO} \), and \( I_{ds}^{rms} \) are specified in Equations 2, 4, STEP-3 and Equation 11, respectively; \( D_{max} \) is specified in Equation 6; \( V_{o(n)} \) is the output voltage of the n-th output; and \( V_{F(n)} \) is the diode \( (D_{R(n)}) \) forward voltage. The typical voltage and current margins for the rectifier diode are:

\[ V_{RRM} > 1.3 \cdot V_{D(n)} \] (EQ 23)

\[ I_F > 1.5 \cdot I_{D(n)}^{rms} \] (EQ 24)

where \( V_{RRM} \) is the maximum reverse voltage and \( I_F \) is the average forward current of the diode.

[STEP-10] Determine the Output Capacitor Considering the Voltage and Current Ripple

The ripple current of the n-th output capacitor \( (C_{o(n)}) \) is obtained as:

\[ I_{cap(n)}^{rms} = \sqrt{(I_{D(n)}^{rms})^2 - I_{o(n)}^2} \] (EQ 25)

where \( I_{o(n)} \) is the load current of the n-th output and \( I_{D(n)}^{rms} \) is specified in Equation 22. The ripple current should be smaller than the ripple current specification of the capacitor. The voltage ripple on the n-th output is given by:

\[ \Delta V_{o(n)} = I_{o(n)}D_{max} + \frac{I_{ds}^{peak} \cdot V_{RO} R_{C(n)} K_{L(n)}}{C_{o(n)} f_s \cdot (V_{o(n)} + V_{F(n)})} \] (EQ 26)

where \( C_{o(n)} \) is the capacitance; \( R_{C(n)} \) is the effective series resistance (ESR) of the n-th output capacitor; \( K_{L(n)} \), \( V_{RO} \), and \( I_{ds}^{peak} \) are specified in Equation 2, STEP-3, and Equation 10, respectively; \( D_{max} \) is specified in Equation 6; \( I_{o(n)} \) and \( V_{o(n)} \) are the load current and output voltage of the n-th output, respectively; and \( V_{F(n)} \) is the diode \( (D_{R(n)}) \) forward voltage.

If it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor, additional LC filter stages (post filter) can be used. When using the post filters, be careful not to place the corner frequency too low. Too low a corner frequency may make the system unstable or limit the control bandwidth. It is typical to set the corner frequency of the post filter at around 10-20% of the switching frequency.

[STEP-11] Design the RCD Snubber

When the power MOSFET is turned off, there is a high voltage spike on the drain due to the transformer leakage inductance. This excessive voltage on the MOSFET may lead to an avalanche breakdown and, eventually, failure of the FPS. Therefore, it is necessary to use an additional network to clamp the voltage.
The RCD snubber circuit and MOSFET drain voltage waveform are shown in Figures 13 and 14, respectively. The RCD snubber network absorbs the current in the leakage inductance by turning on the snubber diode (Dsn) once the MOSFET drain voltage exceeds the voltage of node X, as depicted in Figure 13. In the analysis of snubber network, it is assumed that the snubber capacitor is large enough that its voltage does not change significantly during one switching cycle. The capacitor used in the snubber should be ceramic or a material that offers low ESR. Electrolytic or tantalum capacitors are unacceptable for these reasons.

The first step in designing the snubber circuit is to determine the snubber capacitor voltage (\(V_{sn}\)) at the minimum input voltage and full-load condition. Once \(V_{sn}\) is determined, the power dissipated in the snubber network at the minimum input voltage and full-load condition is obtained as:

\[
P_{sn} = \frac{(V_{sn})^2}{R_{sn}} = \frac{1}{2} f_s L_{lk}(I_{ds\,peak})^2 \frac{V_{sn}}{V_{sn} - V_{RO}}
\]  

(EQ 27)

where \(I_{ds\,peak}\) is specified in Equation 10, \(f_s\) is the FPS free-running switching frequency, \(L_{lk}\) is the leakage inductance, \(V_{sn}\) is the snubber capacitor voltage at the minimum input voltage and full-load condition, \(V_{RO}\) is the reflected output voltage, and \(R_{sn}\) is the snubber resistor. \(V_{sn}\) should be larger than \(V_{RO}\) and it is typical to set \(V_{sn}\) to be 2~2.5 times \(V_{RO}\). Too small a \(V_{sn}\) results in a severe loss in the snubber network, as shown in Equation 27. The leakage inductance is measured at the switching frequency on the primary winding with all other windings shorted.

The snubber resistor with proper rated wattage should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained as:

\[
\Delta V_{sn} = \frac{V_{sn}}{C_{sn} R_{sn} f_s}
\]  

(EQ 28)

where \(f_s\) is the FPS free-running switching frequency. In general, 5~10% ripple of the selected capacitor voltage is reasonable.

The snubber capacitor voltage (\(V_{sn}\)) of Equation 27 is for the minimum input voltage and full-load condition. When the converter is designed to operate in CCM under this condition, the peak drain current, together with the snubber capacitor voltage, decrease as the input voltage increases, as shown in Figure 14. The peak drain current at the maximum input voltage and full load condition \((I_{ds\,peak}^{2})\) is obtained as:

\[
I_{ds\,peak}^{2} = \frac{2 \cdot P_{in}}{f_s L_{m}}
\]  

(EQ 29)

where \(P_{in}\) and \(L_{m}\) are specified in Equations 1 and 7, respectively, and \(f_s\) is the FPS free-running switching frequency.

The snubber capacitor voltage under maximum input voltage and full load condition is obtained as:

\[
V_{sn}^{2} = \frac{V_{RO} + \frac{1}{2} (V_{RO})^2 + 2 R_{sn} L_{lk} f_s (I_{ds\,peak}^{2})}{2}
\]  

(EQ 30)

where \(f_s\) is the FPS free-running switching frequency, \(L_{lk}\) is the primary-side leakage inductance, \(V_{RO}\) is the reflected output voltage, and \(R_{sn}\) is the snubber resistor.

From Equation 30, the maximum voltage stress on the internal MOSFET is given by:

\[
V_{ds\,max} = V_{DC\,max} + V_{sn} - V_{RO}
\]  

(EQ 31)

where \(V_{DC\,max}\) is specified in Equation 4.
Verify that $V_{ds}^{\text{max}}$ is below 90% of the rated voltage of the MOSFET ($BV_{dss}$), as shown in Figure 15. The voltage rating of the snubber diode should be higher than $BV_{dss}$. Usually, an ultra fast diode with 1A current rating is used for the snubber network.

In the snubber design in this section, neither the lossy discharge of the inductor, nor stray capacitance, is considered. In the actual converter, the loss in the snubber network is generally less than the designed value.

Figure 15. MOSFET Drain Voltage and Snubber Capacitor Voltage

[STEP-12] Design the Synchronization Network

The optimum MOSFET turn-on point is indirectly detected by monitoring the $V_{cc}$ winding voltage, as shown in Figures 16 and 17. The output of the sync-detect comparator (CO) becomes high when the sync voltage ($V_{sync}$) rises above 0.7V and becomes low when the $V_{sync}$ drops below 0.2V. The MOSFET is turned on at the falling edge of the sync-detect comparator output (CO).

To synchronize the $V_{sync}$ with the MOSFET drain voltage, the sync capacitor ($C_{SY}$) should be chosen so that $T_Q$ is same as a quarter of the resonance period ($T_R/4$), as shown in Figure 17. $T_R/4$ and $T_Q$ are given as:

\[
T_R/4 = \frac{\pi}{4} \sqrt{\frac{L_m}{C_{eo}}} \tag{EQ 32}
\]

\[
T_Q = \frac{R_{SY1} \cdot (R_{SY2} + R_{SY3})}{R_{SY1} + R_{SY2} + R_{SY3}} \cdot C_{SY} + 200\text{ns} \tag{EQ 33}
\]

where $L_m$ is the primary-side inductance of the transformer, $C_{eo}$ is the effective MOSFET output capacitance, and 200ns is the internal delay time.

The peak value of the sync signal is determined by the voltage divider network $R_{SY1}, R_{SY2},$ and $R_{SY3}$ as

\[
V_{sync}^{pk} = \frac{R_{SY3}}{R_{SY1} \cdot R_{SY2} + R_{SY3}} \cdot \frac{N_B}{N_{ST}} \cdot (V_{OF} + V_{FR}) \tag{EQ 34}
\]
where \( N_a \) and \( N_s1 \) are the numbers of the turns for \( V_{cc} \) winding and \( V_{o1} \), respectively, and \( V_{F1} \) is the forward voltage drop of \( D_1 \).

Choose the voltage divider \( R_{SY1}, R_{SY2} \), and \( R_{SY3} \) so that the peak value of sync voltage \( V_{sync}^{\text{pk}} \) is lower than the OVP threshold voltage (6V) to avoid triggering OVP in normal operation. It is typical to set \( V_{sync}^{\text{pk}} \) to be 4–5V.

[STEP-13] Design the Feedback Loop

Since FSQ-series employs current-mode control, the feedback loop can be simply implemented with a one-pole and one-zero compensation circuit, as shown in Figure 18. In the feedback circuit analysis, it is assumed that the current transfer ratio (CTR) of the opto-coupler is 100%.

The current control factor of FPS, \( K \) is defined as:

\[
K = \frac{I_{pk}}{V_{FB}} = \frac{I_{lim}}{V_{FBsat}} \quad \text{(EQ 35)}
\]

where \( I_{pk} \) is the peak drain current and \( V_{FB} \) is the feedback voltage, respectively, for a given operating condition; \( I_{lim} \) is the current limit of the FPS; and \( V_{FBsat} \) is the feedback saturation voltage, which is typically 2.5V.

To express the small signal AC transfer functions, the small signal variations of feedback voltage \( (v_{FB}) \) and controlled output voltage \( (v_{o1}) \) are introduced as \( \hat{v}_{FB} \) and \( \hat{v}_{o1} \).

\[
G_{vc} = \frac{\frac{\hat{v}_{o1}}{v_{FB}}}{\frac{\hat{v}_{FB}}{v_{FB}}} = \frac{V_{o1}}{V_{FB}} \cdot \frac{(1 + s/w_z)}{(1 + s/w_p)} \quad \text{(EQ 36)}
\]

where \( V_{DC} \) is the DC input voltage; \( R_L \) is the effective total load resistance of the controlled output, defined as \( V_{o1}/P_o \); \( N_p \) and \( N_s1 \) are specified in STEP-7; \( V_{RO} \) is specified in STEP-3; \( V_{o1} \) is the reference output voltage; \( P_o \) is specified in STEP-1; and \( K \) is specified in Equation 35. The pole and zeros of Equation 36 are defined as:

\[
w_z = \frac{1}{R_{C1}C_{o1}}, \quad w_p = \frac{R_L(1-D)^2}{D\ell(N_s1/N_p)^2} \quad \text{and} \quad w_p = \frac{(1+D)}{R_C1C_{o1}} \quad \text{(EQ 37)}
\]

where \( L_a \) is specified in Equation 7, \( D \) is the duty cycle of the FPS, \( C_{o1} \) is the reference output capacitor, and \( R_C1 \) is the ESR of \( C_{o1} \).

When the converter has more than one output, the low frequency control-to-output transfer function is proportional to the parallel combination of all load resistance, adjusted by the square of the turns ratio. Therefore, the effective load resistance is used in Equation 36 instead of the actual load resistance of \( V_{o1} \).

Notice that there is a right half plane (RHP) zero \( (w_{z2}) \) in the control-to-output transfer function of Equation 36. Because the RHP zero reduces the phase by 90°, the crossover frequency should be placed below the RHP zero.

Figure 19 shows the variation of a CCM flyback converter control-to-output transfer function for different input voltages. This figure shows the system poles and zeros, together with the DC gain change, for different input voltages. The gain is highest at the high input voltage condition and the RHP zero is lowest at the low input voltage condition.

Figure 20 shows the variation of a CCM flyback converter control-to-output transfer function for different loads. This figure shows that the low frequency gain does not change for different loads and the RHP zero is lowest at the full-load condition.

For DCM operation, the control-to-output transfer function of the flyback converter, using current-mode control, is given by:

\[
G_{vc} = \frac{\frac{\hat{v}_{o1}}{v_{FB}}}{\frac{\hat{v}_{FB}}{v_{FB}}} = \frac{V_{o1}}{V_{FB}} \cdot \frac{(1 + s/w_z)}{(1 + s/w_p)} \quad \text{(EQ 38)}
\]

where \( w_z = \frac{1}{R_{C1}C_{o1}}, \quad w_p = 2/R_LC_{o1} \).

\( V_{o1} \) is the reference output voltage, \( V_{FB} \) is the feedback voltage for a given condition, \( R_L \) is the effective total
resistance of the controlled output, $C_{ol}$ is the controlled output capacitance, and $R_{c1}$ is the ESR of $C_{ol}$.

Figure 21 shows the variation of the control-to-output transfer function of a flyback converter in DCM for different loads. Contrary to the flyback converter in CCM, there is no RHP zero and the DC gain does not change as the input voltage varies. As can be seen, the overall gain, except for the DC gain, is highest at the full-load condition.

The feedback compensation network transfer function of Figure 18 is obtained as:

$$V_{FB} = \frac{w_i}{s} \left( \frac{1 + s/w_{zc}}{1 + 1/w_{pc}} \right) \quad \text{(EQ 39)}$$

where $w_i = \frac{R_B}{R_1R_D C_F}, w_{zc} = \frac{1}{(R_F + R_I) C_F}, w_{pc} = \frac{1}{R_B C_B}$.

$R_B$ is the internal feedback bias resistor of FPS, which is typically 2.8$k\Omega$; and $R_1, R_D, R_F, C_F$ and $C_B$ are shown in Figure 18.

When the input voltage and the load current vary over a wide range, it is not easy to determine the worst case for the feedback-loop design. The gain, together with zeros and poles, varies according to the operating condition. Even though the converter is designed to operate in CCM or at the boundary of DCM and CCM in the minimum input voltage and full-load condition, the converter enters into DCM, changing the system transfer functions as the load current decreases and/or input voltage increases.

One simple and practical solution to this problem is designing the feedback loop for low input voltage and full-load condition with enough phase and gain margin. When the converter operates in CCM, the RHP zero is lowest in low input voltage and full-load condition. The gain increases about 6dB as the operating condition is changed from the lowest input voltage to the highest input voltage condition under universal input condition. When the operating mode changes from CCM to DCM, the RHP zero disappears, making the system stable. Therefore, by designing the feedback loop with more than 45° of phase margin in low input voltage and full load condition, the stability over the operating ranges can be guaranteed.

The procedure to design the feedback loop is as follows:

- Determine the crossover frequency ($f_c$). For CCM mode flyback, set $f_c$ below 1/3 of right half plane (RHP) zero to minimize the effect of the RHP zero. For DCM mode, $f_c$ can be placed at a higher frequency, since there is no RHP zero.
- When an additional LC filter is employed, the crossover frequency should be placed below 1/3 of the corner frequency of the LC filter, since it introduces a -180° phase drop. Never place the crossover frequency beyond the corner frequency of the LC filter. If the crossover
frequency is too close to the corner frequency, the controller should be designed to have a phase margin greater than 90° when ignoring the effect of the post filter.

- Determine the DC gain of the compensator (\(w_c/w_{zc}\)) to cancel the control-to-output gain at \(f_c\).
- Place a compensator zero (\(f_{zc}\)) around \(f_c/3\).
- Place a compensator pole (\(f_{pc}\)) above \(3f_c\).

\[\frac{V_{o1} - V_{OP} - 2.5}{R_D} > I_{FB}\] (EQ 42)

\[\frac{V_{OP}}{R_{bias}} > 1mA\] (EQ 43)

where \(V_{o1}\) is the reference output voltage; \(V_{OP}\) is opto-diode forward voltage drop, which is typically 1V; and \(I_{FB}\) is the feedback current of FPS, which is typically 1mA. For example, \(R_{bias} < 1k\Omega\) and \(R_D < 1.5k\Omega\) for \(V_{o1}=5V\).

**Miscellaneous Notes**

- **Vcc capacitor (\(C_a\)):** The typical value for \(C_a\) is 10-50µF, which is enough for most applications. A smaller capacitor than this may result in an under-voltage lockout of FPS during the startup. Too large a capacitor may increase the start-up time.

- **Vcc resistor (\(R_a\)):** The typical value for \(R_a\) is 5-20Ω. In the case of multiple outputs flyback converter, the voltage of the lightly loaded output, such as Vcc, varies as the load currents of other outputs change due to the imperfect coupling of the transformer. \(R_a\) reduces the sensitivity of Vcc to other outputs and improves the regulations of Vcc.
Design Example

<table>
<thead>
<tr>
<th>Application</th>
<th>Device</th>
<th>Input Voltage</th>
<th>Output Power</th>
<th>Output Voltage (Rated Current)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVD player</td>
<td>FSQ0365RN</td>
<td>85-265VAC (60Hz)</td>
<td>18.1W</td>
<td>5.1V (1.0A)</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.4V (1.0A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>12V (0.4A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>16V (0.3A)</td>
</tr>
</tbody>
</table>

Key Design Notes
To maximize the efficiency, the power supply is designed to operate in CCM for minimum input-voltage and full-load condition and in DCM for high input voltage condition.

1. Schematic
2. Transformer Specifications

<table>
<thead>
<tr>
<th>No</th>
<th>Pin (s→f)</th>
<th>Wire</th>
<th>Turns</th>
<th>Winding Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Np/2</td>
<td>3 → 2</td>
<td>0.25φ × 1</td>
<td>50</td>
<td>Center Solenoid Winding</td>
</tr>
<tr>
<td></td>
<td></td>
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<td></td>
<td>Insulation: Polyester Tape t = 0.050mm, 2 Layers</td>
</tr>
<tr>
<td>N3.4V</td>
<td>9 → 8</td>
<td>0.33φ × 2</td>
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<td>Center Solenoid Winding</td>
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<td></td>
<td></td>
<td>Insulation: Polyester Tape t = 0.050mm, 2 Layers</td>
</tr>
<tr>
<td>N3V</td>
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<td>0.33φ × 1</td>
<td>2</td>
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<td>Insulation: Polyester Tape t = 0.050mm, 2 Layers</td>
</tr>
<tr>
<td>Na</td>
<td>4 → 5</td>
<td>0.25φ × 1</td>
<td>16</td>
<td>Center Solenoid Winding</td>
</tr>
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<td></td>
<td>Insulation: Polyester Tape t = 0.050mm, 2 Layers</td>
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<tr>
<td>N12V</td>
<td>10 → 12</td>
<td>0.33φ × 3</td>
<td>14</td>
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<td></td>
<td>Insulation: Polyester Tape t = 0.050mm, 3 Layers</td>
</tr>
<tr>
<td>N16V</td>
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<td>0.33φ × 3</td>
<td>18</td>
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<td></td>
<td>Insulation: Polyester Tape t = 0.050mm, 2 Layers</td>
</tr>
<tr>
<td>Np/2</td>
<td>2 → 1</td>
<td>0.25φ × 1</td>
<td>50</td>
<td>Center Solenoid Winding</td>
</tr>
<tr>
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<td></td>
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<td></td>
<td>Insulation: Polyester Tape t = 0.050mm, 2 Layers</td>
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</tbody>
</table>

Core: EER2828 (Ae=86.7mm²)
Bobbin: EER2828

Electrical Characteristics

<table>
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<tr>
<th>Pin</th>
<th>Specification</th>
<th>Remarks</th>
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<tbody>
<tr>
<td>Inductance</td>
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<td>1.4mH ± 10%</td>
</tr>
<tr>
<td>Leakage</td>
<td>1 - 3</td>
<td>25µH Max</td>
</tr>
</tbody>
</table>
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