**AN-4164**

**Design Guideline for 3-Channel Interleaved CCM PFC Using the FAN9673 2.5 kW CCM PFC Controller**

**Introduction**

The interleaved boost Power Factor Correction (PFC) converter has become the topology of choice for high-power applications due to the improved efficiency that can be achieved through load current sharing. By sharing the load current in more than one balanced phase, the RMS current stress, current ripple, and boost inductor size per phase can be significantly reduced. Therefore, the heavy load efficiency can be significantly improved, which allows for the selection of cost effective power MOSFET and boost diode as well as improved longevity of the power supply.

The FAN9673 advanced PFC controller can be an optimal solution for implementing high-power PFC (above several kilowatts). The FAN9673 is a Continuous Conduction Mode (CCM) PFC controller for a three-channel interleaved boost-type pre-regulator.

Incorporating circuits for the implementation of leading edge, average current mode, boost-type power factor correction; the FAN9673 enables the design of a power supply that fully complies with the IEC1000-3-2 specification. The FAN9673 also features an innovative channel management function, which allows the power level of the slave channels to be loaded / unloaded smoothly according to the voltage on CM pin, thereby improving the PFC converter’s load transient response.

This application note presents practical design considerations for a 3-channel interleaved CCM boost PFC employing the FAN9673. It includes the procedure for designing the boost inductor and output filter, selecting the components, and implementing average current mode control. The design procedure is then verified through an experimental 2.5 kW prototype converter. Figure 1 shows the typical application circuit of the PFC converter.

*About DBP please reference System Design Precautions*

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**Figure 1. Typical Application Circuit of FAN9673**
Design Procedure

In this section, a design procedure is presented using the schematic of Figure 1 as the reference. A 2.5 kW rated output power, three-channel CCM interleaved PFC with universal input range is selected as a design example. The design specifications are as follows:

### Table 1. Design Specifications

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<td>Switching Frequency</td>
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### [STEP-1] Estimate Input Rated Power and Output Current

The overall system is comprised of three parallel boost PFC stages, as shown in Figure 2, so the input power of the PFC stage is given as:

\[
P_{IN} = \frac{P_{OUT-TOT}}{\eta}
\]

(1)

where \( \eta \) is the combined efficiency of the PFC stages.

The output current of PFC stage is given by:

\[
I_{OUT-TOT} = \frac{P_{OUT-TOT}}{V_{PFC}}
\]

(2)

The output current of each boost stage is given by:

\[
I_{OUT} = \frac{P_{OUT-TOT}}{V_{PFC} \cdot \text{Channel Number}}
\]

(3)

![Figure 2. PFC Stage Configuration](Image)

### [STEP-2] Frequency Setting

The internal oscillator frequency of the FAN9673 is determined by the external resistor \( R_{RI} \) on the RI pin. The switching frequency is determined by the timing resistor \( R_{RI} \), calculated as:

\[
f_{SW} = \frac{8 \times 10^4}{R_{RI}}
\]

(4)

The guaranteed switching frequency ranges are 18 kHz–40 kHz and 55 kHz–75 kHz.

**Design Example:** \( R_{RI} \) of 20 k\( \Omega \) is selected to obtain 40 kHz switching frequency.

\[
R_{RI} = \frac{8 \times 10^4}{f_{SW}} = \frac{8 \times 10^4}{40 \times 10^3} = 20 \text{ k}\Omega
\]

### [STEP-3] \( V_{IN} \) Range & \( R_{IAC} \) Setting

The FAN9673 senses the peak value of line voltage using the IAC pin, as shown in Figure 3. The peak value of the line voltage is obtained by a peak detect circuit using a sample-and-hold method. Meanwhile, the instantaneous line voltage information is obtained by sensing the current that flows into the IAC pin through \( R_{IAC} \).

\( R_{IAC} \) should be selected according to the input voltage range. For universal AC input (85 V–264 V), \( V_{VIR} \) should be set <1.5 V and \( R_{IAC} \) should chosen as 6 M\( \Omega \). If the input is high-voltage single-AC input (180 V–264 V), \( V_{VIR} \) should be set > 3.5 V (maximum is 5 V) and \( R_{IAC} \) should be chosen as 12 M\( \Omega \). \( V_{VIR} \) determines the application based on AC input range. The change of \( V_{VIR} \) influences gain of gain modulator and brown-in/out hysteresis.

\[
V_{AC} = 85 \text{ V} \sim 265 \text{ V} \Rightarrow R_{IAC} = 6 \text{ M}\Omega V_{VIR} < 1.5 \text{ V}
\]

\[
V_{AC} = 180 \text{ V} \sim 265 \text{ V} \Rightarrow R_{IAC} = 12 \text{ M}\Omega V_{VIR} > 3.5 \text{ V}
\]

(5)

The controller needs to set \( V_{VIR} \) for the different input range as:

\[
V_{VIR} = I_{VIR} \cdot R_{VIR}
\]

(6)
The maximum current of boost inductor is:

\[
I_{L-PK} = I_{L-AVG} \cdot (1 + \frac{K_{RF}}{2}) = \sqrt{\frac{2 \cdot P_{OUT}}{V_{LINE-MIN} \cdot \eta}} \cdot (1 + \frac{K_{RF}}{2}) \quad (11)
\]

**Design Example** The PFC is designed for high-voltage single-AC input (180 V~264 V). \( R_{\text{VIR}} \) should be chosen as 12 MΩ and \( R_{\text{VIR}} \) is:

\[
V_{\text{VIR}} = I_{\text{VIR}} \cdot R_{\text{VIR}} = 10 \mu A \cdot 470k\Omega = 4.7V > 3.5V
\]

470 kΩ is selected as \( R_{\text{VIR}} \) for the AC input range of 180 V~264 V.

### [STEP-4] PFC Inductor Design

The duty cycle of the boost switch at the peak of line voltage is given as:

\[
D_L = \frac{V_{\text{PFC}} - \sqrt{2} V_{\text{LINE}}}{V_{\text{PFC}}} \quad (7)
\]

Then, the maximum current ripple of the boost inductor at the peak of minimum AC line voltage is given as:

\[
\Delta I = \frac{\sqrt{2} V_{\text{LINE-MIN}}}{L_{\text{PFC}}} \cdot \frac{V_{\text{PFC}} - \sqrt{2} V_{\text{LINE-MIN}}}{V_{\text{PFC}}} \cdot \frac{1}{f_{\text{SW}}} \quad (8)
\]

The average of boost inductor current over one switching cycle at the peak of the line voltage for minimum AC input is given by:

\[
I_{L-AVG} = \frac{\sqrt{2} P_{OUT}}{V_{\text{LINE-MIN}} \cdot \eta} \quad (9)
\]

\[
K_{RF} = \frac{\Delta I}{I_{L-AVG}}
\]

**Figure 4. Inductor Current**

For a given current ripple factor (\( K_{RF} = \Delta I / I_{L-AVG} \)), the boost inductor value can be obtained as:

\[
L_{\text{PFC}} = \frac{\sqrt{2} V_{\text{LINE-MIN}}}{K_{RF} \cdot I_{L-AVG}} \cdot \frac{V_{\text{PFC}} - \sqrt{2} V_{\text{LINE-MIN}}}{V_{\text{PFC}}} \cdot \frac{1}{f_{\text{SW}}} \quad (10)
\]

The boost inductor is obtained as:

\[
L_{\text{PFC}} = \frac{\sqrt{2} V_{\text{LINE-MIN}}}{K_{RF} \cdot I_{L-AVG}} \cdot \frac{V_{\text{PFC}} - \sqrt{2} V_{\text{LINE-MIN}}}{V_{\text{PFC}}} \cdot \frac{1}{f_{\text{SW}}}
\]

\[
= \frac{\sqrt{2} \cdot 160}{393 - \sqrt{2} \cdot 160} \cdot \frac{1}{40 \times 10^6} = 221\mu H
\]

The maximum current of the boost inductor is given as:

\[
I_{L-PK} = \sqrt{\frac{2 \cdot P_{OUT}}{V_{\text{LINE-MIN}} \cdot \eta}} \cdot (1 + \frac{K_{RF}}{2})
\]

\[
= \frac{\sqrt{2} \cdot 833}{160 \cdot 0.95} \cdot (1 + \frac{1.4}{2}) = 13.17A
\]

### [STEP-5] PFC Output Capacitor Selection

**Figure 5. PFC Output Voltage Ripple**

The output voltage ripple should be considered when selecting the PFC output capacitor. Figure 5 shows the line frequency ripple on the output voltage. With a given specification of output ripple, the value for the output capacitor can be obtained from:

\[
\frac{C_{\text{OUT}}}{2\pi \cdot f_{\text{LINE}} \cdot V_{\text{PFC-ripple}}} > \frac{I_{\text{OUT-TOT}}}{I_{\text{OUT-TOT}}}
\]

where \( I_{\text{OUT}} \) is nominal output current of the boost PFC stage and \( V_{\text{PFC-ripple}} \) is the peak-to-peak output voltage ripple.
The hold-up time should also be considered when determining the output capacitor value:

\[
C_{OUT} > \frac{2 \cdot P_{OUT-TOT} \cdot t_{HOLD}}{V_{PFC} - V_{PFC-MIN}^2}
\]  

(13)

where \(P_{OUT-TOT}\) is nominal output power of boost PFC stage; \(t_{HOLD}\) is the required holdup time; and \(V_{PFC-MIN}\) is the allowable minimum PFC output voltage during the hold-up time.

**Design Example** With peak-to-peak voltage ripple specification of 5% of \(V_{PFC}\), the capacitor should be:

\[
C_{OUT} > \frac{I_{OUT-TOT} \cdot \Delta t_{rip}}{2 \pi \cdot f_{LINE} \cdot \sqrt{V_{PFC-RIPPLE}}}
\]

\[
= \frac{6.36}{2 \pi \cdot 50 \cdot (393 \cdot 5\%)} = 1030 \mu F
\]

Since the minimum allowable output voltage during one cycle (15 ms) drop-out is 300 V, the capacitor value should be:

\[
C_{OUT} > \frac{2 \cdot P_{OUT-TOT} \cdot t_{HOLD}}{V_{PFC} - V_{PFC-MIN}^2} \cdot \frac{2 \cdot 2500 \cdot 15 \times 10^{-3}}{393^2 - 300^2} = 1163 \mu F
\]

In this case, three parallel connected capacitors of 390 \(\mu F\) are selected for the PFC output capacitor. In this design example, the target application for the three-channel PFC is a home appliance power supply, so there is no hold-up time requirement.

**[STEP-6] Output Sensing & PVO Setting**

To improve system efficiency, the FAN9673 incorporates the programmable PFC output voltage function (PVO). As shown in Figure 6, when the PFC output voltage is much higher than the peak voltage of the AC input, the user can input a DC level from the MCU to the PVO pin to decrease the PFC output voltage. (It is recommended that the PFC output voltage is set at least 25 V higher than the peak voltage of AC input. Otherwise, it is necessary to consider other factors closely related to the PFC output voltage regulation, such as hold-up time, PF, and THD standard of input current.)

The relationship between the feedback voltage level for the PFC output voltage and \(V_{PVO}\) is given as:

\[
V_{FBPFC} = V_{REF} - \frac{V_{PVO}}{4}
\]  

(14)

Once the desired PFC output voltage, \(V_{PFC}\), for low AC input is determined; the required DC voltage level \(V_{PVO}\) is given by:

\[
V_{PVO} = 4 \left( V_{REF} - V_{PFC} \left( \frac{R_{FB3}}{R_{FB1} + R_{FB2} + R_{FB3}} \right) \right)
\]  

(15)

**[STEP-7] Current-Sensing & Current-Limit**
Figure 7 shows the PFC compensation circuits. The first step in compensation network design is to select the current-sensing resistor of the PFC converter, considering the control window of voltage loop. Since line feed-forward is used in FAN9673, the output power is proportional to the output of voltage control error amplifier, $V_{VEA}$, as shown below:

$$P_{OUT}(V_{VEA}) = P_{OUT-MAX} \frac{V_{VEA} - 0.6}{V_{VEA-SAT} - 0.6}$$

(16)

The maximum power limit of PFC is:

$$P_{OUT-MAX} = \frac{V_{LINE-MIN}^{2} \cdot G_{MAX} \cdot R_{M}}{R_{AC} \cdot R_{CS}}$$

(17)

The $R_{CS}$ is the output resistor of modulator to transfer the current command to a voltage type signal. $G_{MAX}$ is a coefficient of the internal control loop.

(Design Example) Setting the maximum power limit of each PFC stage as 1.083 kW (130% of full load per channel), the current sensing resistor is obtained from:

$$R_{CS} = \frac{V_{LINE-MIN}^{2} \cdot G_{MAX} \cdot R_{M}}{R_{AC} \cdot P_{OUT-MAX}} = \frac{160^{2} \cdot 2 \cdot 7.5 \times 10^{3}}{12 \times 10^{6} \cdot 1.3 \cdot 833} = 0.0295 \Omega$$

A 30 mΩ resistor is selected.

Figure 8. $I_{LIMIT}$ and $I_{LIMIT2}$ Function

The FAN9673 has three cases of current limit protections via the $V_{VEA}$, $I_{LIMIT}$, and $I_{LIMIT2}$ to protect OCP and inductor saturation. The user can program the current limit threshold $V_{LIMIT}$ and $V_{LIMIT2}$ by resistor.

Case 1, power (normal state): In the normal case, current / power should be controlled by a command from the gain modulator. When $V_{VEA}$ rises to 6 V, the output power and current of the system are at peak. The power and current can’t increase further.

Case 2, current limit 1 (abnormal state): The current command from the gain modulator is $k \cdot I_{AC} \cdot V_{VEA} / V_{L PK}$. When the system works in abnormal state, such as when the AC cycle is missed and returns in a short period, the $V_{L PK}$ has a delay before returning to the original level. This delay significantly increases the current command. If the command is greater than the $I_{LIMIT}$ clamp level $V_{LIMIT}$, it is limited as in Case 2, shown in Figure 8. If the inductor current is not saturated, the peak current of this channel can be the maximum current design for each channel.

Case 3, current limit 2 (saturation state): In case 3, use the level 80%−90% of maximum current of the switch device to be the saturation protection. This current protection is cycle−by-cycle limited.

![Figure 9. Internal Block of $I_{LIMIT}$](image)

$I_{LIMIT}$ should be triggered before $I_{LIMIT2}$, because $I_{LIMIT}$ is used to prevent saturation of the inductor from damaging switches. $I_{LIMIT}$ signal limits the maximum power (current by clamping level $V_{LIMIT}$. $V_{LIMIT}$ is set by the external resistor $R_{LIMIT}$.

It is typical to set the maximum power limit of the PFC stage to around 120%−150% of full load, such that the $V_{VEA}$ is around 4−4.5 V. 

Resistor $R_{LIMIT}$ can be calculated from:

$$R_{LIMIT} = \frac{1.8 \cdot (P_{AC} / 3) \cdot \sqrt{2} \cdot R_{CS}}{V_{LINE-MIN} \cdot I_{LIMIT}}$$

(18)

Regarding the choice for $I_{LIMIT2}$ level, the user can use 150% of maximum power as the setting. It’s used to protect the switching devices. User can also use the maximum current rating of the semiconductor device with 10% to 20% derating as the limit level. $I_{LIMIT2}$ setting is obtained as:

$$R_{LIMIT2} = \frac{150\% \cdot V_{CS-PK}}{I_{LIMIT2}}$$

(19)

(Design Example)

$$V_{CS-PK} = R_{CS} \cdot I_{L-PK} = 0.03 \cdot 13.17 = 0.395V$$

If $f_{SW}$=40 kHz, is selected, $I_{LIMIT2}$ and $I_{LIMIT}$ is:

$$I_{LIMIT} = \frac{1.2 \cdot 1.0208}{20 \cdot 10^{-3}} = 6.13 \times 10^{-5} A$$

$$I_{LIMIT2} = \frac{1.2 \cdot 1.03125}{20 \cdot 10^{-3}} = 6.19 \times 10^{-5} A$$

$$R_{LIMIT} = \frac{150\% \cdot V_{CS-PK}}{I_{LIMIT}} = \frac{1.5 \cdot 0.395}{6.19 \times 10^{-5}} = 9.57 k\Omega$$

A 10 kΩ resistor is selected for $I_{LIMIT2}$.

The setting of $I_{LIMIT}$ is obtained as:

$$R_{LIMIT} = \frac{1.8 \cdot (P_{AC} / 3) \cdot \sqrt{2} \cdot R_{CS}}{V_{LINE-MIN} \cdot I_{LIMIT}} = \frac{1.8 \cdot 877 \cdot 0.03}{160 \cdot 6.13 \times 10^{-3}} = 27.3 \Omega$$

A 27 kΩ resistor is selected for $I_{LIMIT}$.
[STEP-8] LS & GC Design

Figure 10.  LPT Function for Inductor Current at toff

The Linear Predict (LPT) function, shown in Figure 10, is used to anticipate the behavior of inductor current in the switch turn-off region. The Gain Change (GC) pin and LPT pin are used to adjust the parameters of LPT function. The resistance can be determined by the following equation.

\[
R_{LS} = \frac{L_{LPT}}{1.5 \times 10^{-9} \times R_{CS} \times \left( \frac{R_{FB2} + R_{FB2} + R_{FB3}}{R_{FB3}} \right)}
\]

Gain change is to use to adjust the output of the gain modulation. The resistor value is given by:

\[
R_{GC} = \frac{R_{IC}}{ \left( \frac{R_{FB1} + R_{FB2} + R_{FB3}}{R_{FB3}} \right)}
\]

(Design Example) Inductance of 220 μH is selected. R_{LS} and R_{GC} are obtained as:

\[
R_{LS} = \frac{L}{1.5 \times 10^{-9} \times R_{CS} \times \left( \frac{R_{FB2} + R_{FB2} + R_{FB3}}{R_{FB3}} \right)} = \frac{220 \times 10^6}{1.5 \times 10^{-9} \times 3.7 \times 10^8 + 23.7 \times 10^8} = 31.1k\Omega
\]

\[
R_{GC} = \frac{6 \times 10^6}{ \left( \frac{R_{FB1} + R_{FB2} + R_{FB3}}{R_{FB3}} \right)} = \frac{6 \times 10^6}{3.7 \times 10^6 + 23.7 \times 10^8} = 38.19k\Omega
\]

R_{LS} and R_{GC} are 33 kΩ and 38.2 kΩ used.

[STEP-9] PFC Current Loop Design

The transfer function that relates the duty cycle to the inductor current of boost power stage is given as:

\[
\frac{\dot{i}_L}{d} = \frac{V_{PFC}}{sL_{PFC}}
\]

The transfer function relating the output of the current control error amplifier to the inductor current-sensing voltage is obtained by:

\[
\frac{v_{CSSL}}{v_{IEA}} = \frac{R_{CS} \cdot V_{PFC}}{V_{RAMP} \cdot sL_{PFC}}
\]

where V_{RAMP} is the peak-to-peak voltage of the ramp signal for the current-control PWM comparator, which is 3.8 V.

The transfer function of the compensation circuit is given as:

\[
\frac{v_{IEA}}{v_{CS}} = \frac{2\pi f_{IL}}{s} \frac{1 + \frac{s}{2\pi f_{IL}}}{1 + \frac{s}{2\pi f_{IP}}}
\]

where:

\[
f_{IL} = \frac{G_{MI}}{2\pi \cdot C_{IC1}}
\]

\[
f_{IP} = \frac{1}{2\pi \cdot R_{IC} \cdot C_{IC1}}
\]

The procedure to design the feedback loop is as follows:

(a) Determine the crossover frequency (f_{IC}) around 1/10^6~1/6^6 of the switching frequency. Then calculate the gain of the transfer function of Equation (26) at crossover frequency as:

\[
\frac{G_{MI} v_{CS}}{v_{IEA}} |_{f_{IC}} = \frac{R_{CS} \cdot V_{PFC}}{V_{RAMP} \cdot 2\pi f_{IP} \cdot L_{PFC}}
\]

(b) Calculate R_{IC} such that it makes the closed loop gain unity at crossover frequency:

\[
R_{IC} = \frac{1}{G_{MI} v_{CS} |_{f_{IC}}} - f_{IC}
\]

(c) Since the control-to-output transfer function of the power stage has -20 dB/dec slope and -90° phase at the crossover frequency of 0 dB, as shown in Figure 11, it is necessary to place the zero of the compensation network (f_{IZ}) around on third (1/3) of the crossover frequency so that more than 45° phase margin is obtained. Then the capacitor C_{IC1} is determined as:

\[
C_{IC1} = \frac{1}{R_{IC} \cdot 2\pi f_{IC} / 3}
\]

(d) Place compensator high-frequency pole (f_{CP}) at least a decade higher than f_{IC} to ensure that it does not interfere with the phase margin of the current loop at its crossover frequency.

\[
C_{IC2} = \frac{1}{2\pi \cdot f_{IP} \cdot R_{IC}}
\]
(Design Example) Set crossover frequency as 4 kHz:

\[
\frac{\dot{V}_{CS}}{\dot{V}_{IEA} @ f_c} = \frac{R_{VC} \cdot V_{PFC}}{V_{RAMP} \cdot 2\pi f_c \cdot L_{PFC}}
\]

\[
= \frac{0.03 \cdot 393}{(6.5-1.5) \cdot 2\pi \cdot 4 \times 10^2 \cdot 220\times 10^3} = 0.426
\]

\[
R_{VC} = \frac{1}{G_M \frac{\dot{V}_{CS}}{\dot{V}_{IEA} @ f_c}} = \frac{1}{88 \times 10^{-9} \cdot 0.426} = 26.6\Omega
\]

\[
C_{IC1} = \frac{1}{R_{VC} \cdot 2\pi f_{IC} / 3} = \frac{1}{26.6\times 10^3 \cdot 2\pi \cdot 4 \times 10^2 / 3} = 4.49nF
\]

\[
C_{IC2} = \frac{1}{\pi f_{VP} \cdot R_{IC}} = \frac{1}{2\pi \cdot 4 \times 10^2 \cdot 26.6 \times 10^3} = 0.15nF
\]

Modify the DC gain and BW of current loop, use 17.4 kΩ for \( R_{IC} \), 2.2 nF for \( C_{IC1} \), and 100 pF for \( C_{IC2} \).

[STEP-10] PFC Voltage Loop Design

Since FAN9673 employs line feed-forward, the power stage transfer function becomes independent of the line voltage. Then, the low-frequency, small-signal, control-to-output transfer function is obtained as:

\[
\frac{\dot{v}_{PFC}}{\dot{v}_{V EA}} \approx \frac{I_{OUT-TOT} \cdot K_{MAX} \cdot 1}{sC_{OUT}}
\]

where:

\[
\frac{\dot{v}_{PFC}}{\dot{v}_{V EA}} \approx \frac{I_{OUT-TOT} \cdot K_{MAX} \cdot 1}{sC_{OUT}}
\]

![Closed-Loop Gain](image)

Figure 12. Voltage Loop Compensation

Proportional and integration (PI) control with high-frequency pole typically used for compensation. The compensation zero \( (f_{C2}) \) introduces phase boost, while the high-frequency compensation pole \( (f_{VP}) \) attenuates the switching ripple, as shown in Figure 12.

The transfer function of the compensation network is obtained as:

\[
\frac{\dot{V}_{COMP}}{\dot{V}_{PFC}} = \frac{2\pi f_{VZ}}{s + \frac{2\pi f_{VZ}}{2\pi f_{VP}}}
\]

where:

\[
f_{VZ} = \frac{2.5}{V_{OUT} / 2\pi \cdot C_{VC1}}, f_{VP} = \frac{2\pi \cdot R_{VC} \cdot C_{VC1}}{2\pi \cdot R_{VC} \cdot C_{VC2}}
\]

The procedure to design the feedback loop is as follows:

(a) Determine the crossover frequency \( (f_{VC}) \) around 1/10-1/5 of the line frequency. Since the control-to-output transfer function of power stage has -20 dB/dec slope and -90° phase at the crossover frequency, shown in Figure 12 as 0 dB; it is necessary to place the zero of the compensation network \( (f_{C2}) \) around the crossover frequency so that 45° phase margin is obtained. Then, the capacitor \( C_{VC1} \) is determined as:

\[
C_{VC1} = \frac{G_{AV} \cdot I_{OUT-TOT} \cdot K_{MAX} \cdot 2.5}{5 \cdot C_{OUT} \cdot (2\pi f_{VC})^2 \cdot V_{PFC}}
\]

To place the compensation zero at the crossover frequency, the compensation resistor is obtained as:

\[
R_{VC} = \frac{1}{2\pi \cdot f_{VC} \cdot C_{VC1}}
\]

(b) Place compensator high-frequency pole \( (f_{VP}) \) at least a decade higher than \( f_c \) to ensure that it does not interfere with the phase margin of the voltage regulation loop at its crossover frequency. It should also be sufficiently lower than the switching frequency of the converter so noise can be effectively attenuated. Then, the capacitor \( C_{VC2} \) is determined as:

\[
C_{VC2} = \frac{1}{2\pi \cdot f_{VP} \cdot R_{VC}}
\]

(Design Example)

Set the crossover frequency as 20 Hz:

\[
C_{VC1} = \frac{G_{AV} \cdot I_{OUT-TOT} \cdot K_{MAX} \cdot 2.5}{5 \cdot C_{OUT} \cdot (2\pi f_{VC})^2 \cdot V_{PFC}}
\]

\[
= \frac{70 \times 10^{-6} \cdot 6.36 \cdot 1.3 \cdot 2.5}{5 \cdot 1.17 \times 10^{-6} \cdot (2\pi \cdot 20)^2 \cdot 393} = 40nF
\]

\[
R_{VC} = \frac{1}{2\pi \cdot f_{VC} \cdot C_{VC1}} = \frac{1}{2\pi \cdot 20 \cdot 40.5 \times 10^{-9}} = 196k\Omega
\]

\[
C_{VC2} = \frac{1}{2\pi \cdot f_{VP} \cdot R_{VC}} = \frac{1}{2\pi \cdot 100 \cdot 196 \times 10^{-9}} = 8.12nF
\]

Modify the DC gain and BW of voltage loop; using 75 kΩ for \( R_{VC} \), 1 μF for \( C_{VC1} \), and 0.1 μF for \( C_{VC2} \).
[STEP-11] Channel Management Control

Figure 13 shows the CM pin control with an external voltage signal. The V_{VEA} control voltage is generated by regulation error amplifier and is proportional to average current of input. When V_{CM} is pulled LOW to 0 V, the PFC channel is enabled. When the V_{CM} is pulled HIGH and over 4 V, the channel is disabled. Figure 14 shows that channel 3 is disabled by an external signal when the system is operating at half-load condition.

[STEP-12] Soft Start

Figure 17 shows the soft start (SS) waveform. FAN9673 uses soft-start voltage, V_{SS}, to clamp the PFC power command of voltage loop V_{VEA}. To increase the soft-start time, the value of the soft-start capacitance C_{SS} can be increased.

\[
C_{SS} = \frac{I_{SS} \cdot t_{SS}}{V_{SS}}
\]  

(37)

(Design Example)

Assuming that V_{VEA} is out of clamping by V_{SS} at 5 V, the design soft-start time t_{SS} is 50 ms and I_{SS} is 20 μA. The required soft-start capacitor value is:

\[
C_{SS} = \frac{20 \times 10^{-6} \cdot 100 \times 10^{-3}}{5} = 0.4 \mu F
\]

0.47 μF is selected for C_{SS}.
[STEP-13] RLPK Setting

The relationship of \( V_{\text{IN,PK}} \) to \( V_{\text{LPK}} \) is shown in Figure 18. The peak-detection circuits identify the \( V_{\text{IN}} \) information from the IAC current through a ratio (the relationship shown in Equation (42)). Caution: the maximum \( V_{\text{LPK}} \) can’t be over 3.8 V when system operation at maximum AC input.

As with the below design example, assume the maximum \( V_{\text{IN,PK}} \) at 373 V (AC264V). The relationship of \( V_{\text{IN,PK}} / V_{\text{LPK}} \) is 100, then calculate the \( V_{\text{LPK}} = 3.73 \) V < 3.8 V.

\[
V_{\text{LPK}} = \frac{V_{\text{IN,PK}}}{100} \times \frac{R_{\text{RLPK}}}{12.4k}
\]  

(38)

![Figure 18. Relationship of \( V_{\text{RLPK}} \) to \( V_{\text{LPK}} \)](image)

(Design Example) Assuming the \( V_{\text{LPK}} \) is 3.73 V when \( V_{\text{IN,PK}} \) is 373 V, (AC264V):

\[
R_{\text{RLPK}} = 12.4k \cdot \frac{V_{\text{LPK}}}{V_{\text{IN,PK}}} = 12.4k\Omega
\]

12.1 k is selected for \( R_{\text{RLPK}} \).

[STEP-14] Line Sensing for Brown-In / Out

The FAN9673 has an internal AC UVP comparator that monitors the AC input voltage and disables PFC stage when the \( V_{\text{BIBO}} \) is less than 1.05 V for 450 ms. If the \( V_{\text{BIBO}} \) voltage is over 1.9 V/1.75 V, the PFC stage enables. The VIR pin is used to set the AC input range, as shown in Table 2.

![Figure 19. Brown-In / Out Circuits](image)

Table 2. AC Input Range with Controller Setting

<table>
<thead>
<tr>
<th>Input Range</th>
<th>AC (V)</th>
<th>( R_{\text{VIR}} ) Setting</th>
<th>( R_{\text{IAC}} ) Setting</th>
<th>Brown-In/Out Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-Range</td>
<td>85~264</td>
<td>10 kΩ</td>
<td>6 MΩ</td>
<td>AC 85 V/75 V</td>
</tr>
<tr>
<td>HV-Single</td>
<td>180~264</td>
<td>470 kΩ</td>
<td>12 MΩ</td>
<td>AC 170 V/160 V</td>
</tr>
</tbody>
</table>

The FAN9673 senses the RMS value and the instantaneous value of the line voltage using the BIBO pins as shown in Figure 19. The RMS value of the line voltage is obtained by an averaging circuit using a low-pass filter with two poles.

The RMS sensing circuit should be designed considering the nominal operation range of line voltage and brownout protection trip point as:

\[
V_{\text{bo}} = \frac{\sqrt{2} R_{\text{b4}}}{R_{\text{b1}+2} + R_{\text{b3}} + R_{\text{b4}}} \cdot \frac{2}{\pi}
\]  

(39)

\[
V_{\text{hi}} < \frac{\sqrt{2} R_{\text{b4}}}{R_{\text{b1}+2} + R_{\text{b3}} + R_{\text{b4}}}
\]  

(40)

where \( V_{\text{bo}} \) and \( V_{\text{hi}} \) are brownout/in thresholds of \( V_{\text{rms}} \). When \( V_{\text{AC}} \) is full range input (universal input), the brownout / in thresholds \( V_{\text{bo}} \) and \( V_{\text{hi}} \) are 1.05 V (\( V_{\text{BIBO-FL}} \)) and 1.9 V (\( V_{\text{BIBO-FL}} + \Delta V_{\text{BIBO-F}} \)). But if the \( V_{\text{AC}} \) is high voltage single range input (AC 180 V~264 V), the brownout/in thresholds of \( V_{\text{bo}} \) and \( V_{\text{hi}} \) should be 1.05 V (\( V_{\text{BIBO-HL}} \)) and 1.75 V (\( V_{\text{BIBO-HL}} + \Delta V_{\text{BIBO-H}} \)).

It is typical to set \( R_{\text{RMS}} \) as 10% of \( R_{\text{RMS}} \). The poles of the low-pass filter are given as:

\[
f_{p1} = \frac{1}{2\pi \cdot C_{b1} \cdot R_{b3}}
\]  

(41)

\[
f_{p2} = \frac{1}{2\pi \cdot C_{b2} \cdot R_{b4}}
\]  

(42)

To properly attenuate the twice line frequency ripple in \( V_{\text{RMS}} \), it is typical to set the poles around 10~20 Hz.

(Design Example) The brownout protection thresholds are 1.05 V (\( V_{\text{BIBO-HL}} \)) and 1.75 V (\( V_{\text{BIBO-HL}} + \Delta V_{\text{BIBO-H}} \)) respectively. The scaling down factor of the voltage divider is:

\[
\frac{R_{b3}}{R_{b1}+2 + R_{b3} + R_{b4}} = \frac{V_{\text{LINE.BO}}}{\frac{\sqrt{2}}{2}} \cdot \frac{\pi}{160} = 7.289m
\]

The startup of the PFC controller at minimum line voltage is checked as:

\[
V_{\text{LINE.MIN}} \cdot \sqrt{2} R_{b4} = 170 \cdot \sqrt{2} \cdot 7.289m = 1.752 > 1.75V
\]

\[
R_{b1} = R_{b2} = 1 MΩ, R_{b3} = 200 kΩ, \text{ and } R_{b4} = 16.2 kΩ.
\]

To place the poles of the low-pass filter at 15 Hz and 22 Hz, the capacitors are obtained as:

\[
C_{b1} = \frac{1}{2\pi \cdot f_{p1} \cdot R_{b3}} = \frac{1}{2\pi \cdot 15 \cdot 200 \times 10^3} = 53nF
\]

\[
C_{b2} = \frac{1}{2\pi \cdot f_{p2} \cdot R_{b4}} = \frac{1}{2\pi \cdot 22 \cdot 16.2 \times 10^3} = 447nF
\]
### Design Summary

<table>
<thead>
<tr>
<th>Application</th>
<th>Output Power</th>
<th>Input Voltage</th>
<th>Output Voltage / Output Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-Stage Three-Channel PFC</td>
<td>2500 W</td>
<td>180–264 V&lt;sub&gt;AC&lt;/sub&gt;</td>
<td>393 V/6.36 A</td>
</tr>
</tbody>
</table>

### Features

- AC180V–264 V, Three-Channel PFC Using FAN9673
- Switch-Charge Technique of Gain Modulator for Better PF and Lower THD
- 40 kHz Low Switching Frequency Operation with IGBT
- Protections: Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), and Over-Current Protection (I<sub>LIMIT</sub>). Inductor Saturation Protection (I<sub>LIMIT2</sub>)

![Figure 20. Final Schematic of Design Example](www.fairchildsemi.com)

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Appendix A

Table 3. Parameters of FAN9673 Evaluation Board

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DD} Maximum</td>
<td>20 V</td>
</tr>
<tr>
<td>V_{DD} OVP</td>
<td>24 V</td>
</tr>
<tr>
<td>V_{CC} UVLO</td>
<td>10.3 V/12.8 V</td>
</tr>
<tr>
<td>PVO</td>
<td>0 V~1 V</td>
</tr>
<tr>
<td>PFC Soft-Start</td>
<td>C_{SS} = 0.47 μF</td>
</tr>
<tr>
<td>Brown-In/Out</td>
<td>170 V/160 V</td>
</tr>
<tr>
<td>Gate Clamp</td>
<td>2.4 V/1.55 V (96%/62%)</td>
</tr>
<tr>
<td>V_{DD} Maximum</td>
<td>20 V</td>
</tr>
</tbody>
</table>

Table 4. MOSFET and Diode Reference Specification

<table>
<thead>
<tr>
<th>Voltage Rating</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>600 V (IGBT)</td>
<td>FGH20N60UFDF</td>
</tr>
<tr>
<td>600 V</td>
<td>Boost Diodes  FFH15S60STU</td>
</tr>
</tbody>
</table>

System Design Precautions

- Pay attention to the inrush current when AC input is first connected to the boost PFC convertor. It is recommended to use NTC and a parallel connected relay circuit to reduce inrush current.
- Add bypass diode D_{BP} to provide a path for inrush current when PFC starts up.
- The PFC stage is normally used to provide power to a downstream DC-DC or inverter. It’s recommend that downstream power stage is enabled to operate at full load once the PFC output voltage has reaches a level close to the specified steady-state value.
- The PVO function is used to change the output voltage of PFC, V_{PFC}. The V_{PFC} should be kept at least 25 V higher than V_{IN}. 
Layout Guide

- The current-sense resistor and current-sense filter (C_F1, C_F2) should be as close to the CS+/CS- pins as possible.
- Similar to other power management devices, when laying out the PCB, it is important to use star grounding techniques and to keep the filter capacitor and control components as close to the controller IC and its GND pin as possible.
- Keep high-current output and power ground paths separate from the signal ground path. Make a single-point connection from signal ground to the power ground. Connect the FAN9673’s GND to the power ground at the negative terminal of C_OUT.
- The return path for the gate drive current should be connected to the power ground. Minimize the ground loops between the driver outputs, totem-pole buffer transistors, power switches, and power ground.
- To minimize the possibility of interference caused by magnetic coupling from the boost inductor, the device should be located at least 2.5 cm (1 inch) away from the boost inductor. It is also recommended that the device not be placed underneath magnetic components.
- Keep the width of PCB track handling the gate drive current to the switching devices wide to handle the high peak current level.

Figure 21.  Layout Diagram
Related Datasheets

FAN9673 — Three Channels Interleaved CCM PFC Controller
FEBFAN9673_B01H5000A — User Guide for FEBFAN9673_B01H5000A
FAN9612 — Interleaved Dual BCM PFC Controller
AN-6086 — Design Consideration for Interleaved Boundary Conduction Mode (BCM) PFC Using FAN9612
FAN6982 — CCM Power Factor Correction Controller
AN-8027 — FAN480X PFC+PWM Combo Controller Application

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.