AN-4185

FL7734 Design Tool Flow

Overview

This application note provides a step-by-step guide for using the FL7734 Design Tool. It should be used in conjunction with the FL7734 product information.

Design Flow

The FL7734 design starts with system definition. Then design parameters will be calculated through the power converter design and control circuit design. In order to increase efficiency, an active damper circuit design can be completed according to user’s preference.
Design Selection

User can select 4 different designs based on target specification.

**Design Selection**

<table>
<thead>
<tr>
<th>Wide Dimming Design</th>
<th>Line</th>
<th>High-line</th>
<th>Low-line</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output power range</td>
<td>&gt; 3 W</td>
<td>&gt; 3 W</td>
<td></td>
</tr>
<tr>
<td>Input voltage range</td>
<td>188–264 Vac (+/-14%)</td>
<td>108–132 Vac (+/-10%)</td>
<td></td>
</tr>
<tr>
<td>Features</td>
<td>Wide dimming range (min. load &lt; 5%) Better flicker immunity against phase angle fluctuation</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[Wide Dimming Design]

In case of high-line, min. phase angle of the most dimmers is large with narrow dimming range. Therefore, high-line driver less than 15 W is mostly designed based on the wide dimming design method.

In case of low-line, min. phase angle of the most dimmers reaches 0 degree and wide dimming range is easily implemented. Another advantage of wide dimming design is better flicker immunity against phase angle fluctuation. Some dimmers have inherent random phase angle fluctuation which could induce weak flicker especially at small phase angle and the wide dimming design relieves the weak flicker by reducing output current.

**Design Selection**

<table>
<thead>
<tr>
<th>Wide Input/Output Design</th>
<th>Line</th>
<th>High-line</th>
<th>Low-line</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output power range</td>
<td>&gt; 15 W</td>
<td>&gt; 5 W</td>
<td></td>
</tr>
<tr>
<td>Input voltage range</td>
<td>180–264 Vac (+/-19%)</td>
<td>90–132 Vac (+/-19%)</td>
<td></td>
</tr>
<tr>
<td>Features</td>
<td>Wide input voltage range</td>
<td>Wide output voltage range</td>
<td></td>
</tr>
</tbody>
</table>

[Wide Input/Output Design]

Wide I/O design can handle input voltage range over +/- 20%. This design method also can allow wide output voltage especially for ballast driver design which should be compatible with various LED load voltages.

In case of high-line, wide input design can be selected for high power design because dimming range can be widened at higher output power (over 15 W) whether high-line dimmers have large min. phase angle.

In case of low-line, the driver should be designed based on wide input design method when input voltage range is 90 – 132 Vac.

[Recommended output voltage range]

- Min. output power limit is 15 W at high-line and 5 W at low-line.
- If max. output power is 20 W at high-line, output voltage range is 90–100% (180/260V – 370/370V)
- If max. output power is 20 W at high-line, output voltage range is 75–100% (180/260V – 370/370V)
- If max. output power is 20 W at low-line, output voltage range is 25–100% (90/132V – 200/370V)
- If max. output power is 10 W at low-line, output voltage range is 80–100% (90/132V – 180/260V)
Every single slide has tag at the right top side.

After selecting design method, please follow the slide which includes the tag you select.
Step 1 – Input / Output Specs

Input/Output Spec

Blue box is input from user, Red box is calculated output.

In wide I/O design, min. Vout can be lowered based on Pout. At high-line, Min. Vout can be reduced to \(V_{out} = \frac{15\text{W}}{P_{out}}\).

At low-line, Min. Vout can be reduced to \(V_{out} = \frac{5\text{W}}{P_{out}}\).

In wide dimming design, recommended min. Vout is 90% rated Vout.

Over voltage protection is triggered at Max. Vout.

Output current is Rated Iout at both dimming and non-dimming conditions.

Step 2 – Dimmer Specs

Dimmer Spec

Output current is constantly regulated from CC (Constant Current) phase angle to 180°. CC phase angle is normally 180°.

Enter \(I_{HOLD}\) (selected) close to \(I_{HOLD}\) (recommended).

The FL7734 system will be compatible with dimmers which have lower holding current than \(I_{HOLD}\) (selected).

In wide dimming design, \(I_{HOLD}\) (selected) close to \(I_{HOLD}\) (recommended) is strongly recommended for system stability.

In wide I/O design, \(I_{HOLD}\) (selected) could be determined higher than \(I_{HOLD}\) (recommended). But, it will reduce dimming range.
### Step 3 – Transformer Specs

#### Transformer Design

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. Duty (%)</td>
<td>20.8</td>
</tr>
<tr>
<td>Switching freq.</td>
<td>60 kHz</td>
</tr>
<tr>
<td>Max. Ton (us)</td>
<td>3.4</td>
</tr>
<tr>
<td>Ae</td>
<td>36 mm²</td>
</tr>
<tr>
<td>BMAX</td>
<td>0.30</td>
</tr>
<tr>
<td>LM</td>
<td>1.49 mH</td>
</tr>
<tr>
<td>Min. Np</td>
<td>97.7 T</td>
</tr>
<tr>
<td>Np (selected)</td>
<td>124 T</td>
</tr>
<tr>
<td>Np (recommended)</td>
<td>44.3 T</td>
</tr>
<tr>
<td>Ns (selected)</td>
<td>44 T</td>
</tr>
<tr>
<td>Ns (recommended)</td>
<td>39.5 T</td>
</tr>
<tr>
<td>Na (selected)</td>
<td>40 T</td>
</tr>
<tr>
<td>Lcx</td>
<td>7.0 µH</td>
</tr>
</tbody>
</table>

- **Max. duty is generally between 10 – 30%**.
- **Switching frequency at non-dimming mode**.
- **This is generally set around 65 kHz**.
- **In general, conduction EMI becomes better as switching freq. is lower**.
- **Max. Ton should be less than 10 us**.
- **Enter Np higher than Min. Np**.
- **Np & Ns (recommended) are dependent on Max. Vcs (expected) in Feedback Circuit Section**.
- **If Np & Ns (recommended) are too many in the allowed window, increase Max. Vcs (expected)**.
- **Design transformer according to the above spec. Then, enter Lcx by measuring the transformer**.

#### Feedback Circuit

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. Vg (expected)</td>
<td>9.3 V</td>
</tr>
</tbody>
</table>

**Max. duty is generally between 10 – 30%**.

**Switching frequency at non-dimming mode**.

**This is generally set around 65 kHz**.

**In general, conduction EMI becomes better as switching freq. is lower**.

**Max. Ton should be less than 10 us**.

**Enter Np higher than Min. Np**.
Step 4 – Snubber Specs

Snubber Design

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{SN}$</td>
<td>152 V</td>
</tr>
<tr>
<td>$\Delta V_{SN}$</td>
<td>10 V</td>
</tr>
<tr>
<td>$R_{SN}$ (w/o active damper)</td>
<td>117 kohm</td>
</tr>
<tr>
<td>$R_{SN}$ (w/ active damper)</td>
<td>193 kohm</td>
</tr>
<tr>
<td>$C_{SN}$</td>
<td>2 nF</td>
</tr>
</tbody>
</table>

$V_{SN}$ is generally set as 2 ~ 2.5 times $n_{PS}$ x $V_{OUT}$.

$\Delta V_{SN}$ is generally set as 5% ripple of $V_{SN}$.

If active damper is not used, select $R_{SN}$ (w/o active damper)
If active damper is used, select $R_{SN}$ (w/ active damper)

Because $R_{OP2}$ path provides biasing current for active damper, snubber voltage is determined by both $R_{SN}$ and $R_{OP2}$ path.
Step 5 – Power Device Rating

Power Device Rating

<table>
<thead>
<tr>
<th>Power Device Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW(<em>{\text{MAIN}}) (V</em>{\text{MAX}})</td>
</tr>
<tr>
<td>SW(<em>{\text{MAIN}}) (I</em>{\text{PK}})</td>
</tr>
<tr>
<td>SW(<em>{\text{MAIN}}) (I</em>{\text{MS}})</td>
</tr>
<tr>
<td>D(<em>{\text{OUT}}) (V</em>{\text{MAX}})</td>
</tr>
<tr>
<td>D(<em>{\text{OUT}}) (I</em>{\text{PK}})</td>
</tr>
<tr>
<td>D(<em>{\text{OUT}}) (I</em>{\text{AVG}})</td>
</tr>
</tbody>
</table>

- \(SW_{\text{MAIN}} V_{\text{MAX}}\): Main switch max. drain–source voltage
- \(SW_{\text{MAIN}} I_{\text{PK}}\): Main switch peak current
- \(SW_{\text{MAIN}} I_{\text{MS}}\): Main switch RMS current
- \(D_{\text{OUT}} V_{\text{MAX}}\): Output diode max. reverse voltage
- \(D_{\text{OUT}} I_{\text{PK}}\): Output diode peak current
- \(D_{\text{OUT}} I_{\text{AVG}}\): Output diode average current

Power Device Rating

<table>
<thead>
<tr>
<th>Power Device Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW(<em>{\text{MAIN}}) &amp; D(</em>{\text{OUT}}) (V_{\text{MAX}})</td>
</tr>
<tr>
<td>SW(<em>{\text{MAIN}}) &amp; D(</em>{\text{OUT}}) (I_{\text{PK}})</td>
</tr>
<tr>
<td>SW(<em>{\text{MAIN}}) &amp; D(</em>{\text{OUT}}) (I_{\text{MS}})</td>
</tr>
<tr>
<td>D(<em>{\text{OUT}}) (I</em>{\text{AVG}})</td>
</tr>
</tbody>
</table>

- \(SW_{\text{MAIN}} \& D_{\text{OUT}} V_{\text{MAX}}\): Main switch & output diode max. voltage
- \(SW_{\text{MAIN}} \& D_{\text{OUT}} I_{\text{PK}}\): Main switch & output diode peak current
- \(SW_{\text{MAIN}} I_{\text{MS}}\): Main switch RMS current
- \(D_{\text{OUT}} V_{\text{MAX}}\): Output diode max. reverse voltage
- \(D_{\text{OUT}} I_{\text{PK}}\): Output diode peak current
- \(D_{\text{OUT}} I_{\text{AVG}}\): Output diode average current
Step 6 – Feedback Circuits

Max. $V_{CS}$ should be lower than 1.08 V current-limit. Higher Max. $V_{CS}$ increases $R_{CS}$ and $n_{op}$. [Effect of higher $n_{op}$.]
- Widens DCM region and reduces BCM region.
- $N_{o}$ and $N_{s}$ are reduced. (more margin for window area)
- Higher snubber loss or higher max. voltage of switching MOSFET
- Lower max. voltage of output diode

In buckboost design, Max. $V_{CS}$ is not set in Feedback Circuit Section. [Difference from flyback design]
- For wider DCM region, reduce Max. Duty in Transformer Section.
- For more margin in the window area, reduce Max. Duty in Transformer Section.
- Max. voltage of switching MOSFET and output diode is fixed.
Feedback Circuit

<table>
<thead>
<tr>
<th>Feedback Circuit</th>
<th>T_GATE_OFF</th>
<th>RCORE</th>
<th>CBB</th>
<th>RV1</th>
<th>RV2</th>
<th>CBB</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>90 ns</td>
<td>159 Ω</td>
<td>1.0 mF</td>
<td>302 kΩ</td>
<td>38 kΩ</td>
<td>10 pF</td>
</tr>
</tbody>
</table>

T_GATE_OFF is the time from VCS peak to ISW (Switch current) peak. ISW should be measured at the node between transformer and MOSFET drain.

R_CORE compensates CC tolerance by line voltage change. (Line CC tolerance is caused by T_GATE_OFF.)

CBB is typically 1 - 2.2 mF. Larger CBB makes slower feedback loop.

CVS relieves voltage spike at gate-off. Increase CBB until VS voltage at 1.5 us after gate-off is flat.

Step 7 – HOLD Circuits

HOLD Circuit

<table>
<thead>
<tr>
<th>HOLD Circuit</th>
<th>RHOLD</th>
<th>CHOLD</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>18 kΩ</td>
<td>1.0 nF</td>
</tr>
</tbody>
</table>

In general, CHOLD is 1 - 5 nF.

Large CHOLD has pros and cons.
Pros: can remove LED shimmer if there is.
Cons: input current at firing drops which can cause TRIAC misfiring with flicker.

How to select CHOLD:
1. Select the worst dimmer which has the highest holding current in user’s dimmer list.
2. Increase CHOLD until input current drop at firing is not lower than TRIAC holding current.
(The test condition should be max. and min. phase angle, in which input current drop is the lowest.)
Step 8 – CIC Circuit

CIC Circuit

Yield and temperature tolerance
R<sub>TDC</sub> should be less than +/- 1%. C<sub>TDC</sub> should be less than +/- 5%.

FB voltage can control HOLD voltage by HOLD pull-up circuit (SW<sub>CIC</sub>, D<sub>CIC</sub>, R<sub>TDC</sub> and R<sub>HO</sub>). When FB voltage is increased, HOLD voltage is pulled up and input current level is increased with more power delivery.

In wide I/O design, FB voltage controls HOLD voltage simply by SW<sub>CIC</sub>.
Step 9 – DIM Circuit

[Yield and temperature tolerance]

\[ R_{\text{DIM1}} \text{ and } R_{\text{DIM2}} \text{ tolerance should be less than } +/- 1\%. \]

\[ \frac{R_{\text{REC}}}{R_{\text{DIM1}} + R_{\text{DIM2}}} \text{ (for Modal selection)} \]

*Max. \( r_{\text{DIM}} \) limit
- FB should not be clamped by MOD voltage at max. phase angle.
- If MOD clamps FB voltage at max. phase angle, output current will be higher than the rated output current.
- Therefore, check if FB is clamped by MOD voltage at max. phase angle condition.
- If FB is pulled up by MOD voltage, reduce \( r_{\text{DIM}} \). (In order to reduce \( r_{\text{DIM}} \), increase \( R_{\text{DIM1}} \), and decrease \( R_{\text{DIM2}} \). Keep \( R_{\text{DIM1}} + R_{\text{DIM2}} \) same as design tool.)

*Min. \( r_{\text{DIM}} \) limit
- If output current oscillation with periodic visible flicker is occurred, increase \( r_{\text{DIM}} \).
Step 10 – VIN Circuit

At high-line, $R_{VIN}$ is 2 Mohm. At low-line, $R_{VIN}$ is 620 kohm.

$C_{VIN}$ filters switching noise into VIN pin.
### Step 11 – Bleeding Circuit

**Bleeding Circuit**

Total EMI filter capacitor behind the bridge diode. If input voltage range is +/- 10%, user can select film capacitor for $C_{N\text{TOTAL}}$ for $C_{N\text{BLEED}}$. If input voltage range is +/- 16%, user needs to use around 50% of $C_{N\text{TOTAL}}$ for $C_{N\text{BLEED}}$ as MLCC. (MLCC capacitance drops at higher voltage and it will help to handle wider input voltage range.)

<table>
<thead>
<tr>
<th>BLD Circuit</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{N\text{TOTAL}}$</td>
<td>115 nF</td>
<td></td>
</tr>
<tr>
<td>$C_{N\text{BLEED}}$</td>
<td>58 nF</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{BLEED}}$</td>
<td>1 kΩ</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{BLEED}}$</td>
<td>35 Ω</td>
<td></td>
</tr>
</tbody>
</table>

Total bleeder capacitor
- Check input current at firing with leading edge dimmer
- Increase $C_{N\text{BLEED}}$ until input current drop is higher than TRIAC holding current at the firing moment.

[$R_{\text{BLEED}}$ selection guidance]
- Test condition: Max./Half/Min. phase angle
- Probe both input current and $R_{\text{BLEED}}$ current.
- Find $R_{\text{BLEED}}$ value which minimizes input current drop at firing.

At the min. input voltage and half phase angle condition, compare the line voltage and the input voltage behind the bridge diode. After referring calculated $R_{\text{BLEED}}$, user needs to adjust $R_{\text{BLEED}}$ so that the line voltage zero crossing point is close to that of the input voltage behind the bridge diode in the condition.

**Bleeding Circuit**

Total EMI filter capacitor behind the bridge diode.
At wide I/O design, user doesn’t need to use MLCC for $C_{N\text{TOTAL}}$ and $C_{N\text{BLEED}}$ to handle wide input voltage.

<table>
<thead>
<tr>
<th>BLD Circuit</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{N\text{TOTAL}}$</td>
<td>200 nF</td>
<td></td>
</tr>
<tr>
<td>$C_{N\text{BLEED}}$</td>
<td>200 nF</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{BLEED}}$</td>
<td>1 kΩ</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{BLEED}}$</td>
<td>20 Ω</td>
<td></td>
</tr>
</tbody>
</table>

Total bleeder capacitor
- Check input current at firing with leading edge dimmer
- Increase $C_{N\text{BLEED}}$ until input current drop is higher than TRIAC holding current at the firing moment.

[$R_{\text{BLEED}}$ selection guidance]
- Test condition: Max./Half/Min. phase angle
- Probe both input current and $R_{\text{BLEED}}$ current.
- Find $R_{\text{BLEED}}$ value which minimizes input current drop at firing.

At wide I/O design, $R_{\text{BLEED}}$ selection is more flexible and user can increase $R_{\text{BLEED}}$ to reduce bleeding current if bleeding switch is too hot, Once increasing $R_{\text{BLEED}}$, Max. $I_{\text{BLEED}}$ (upper limit) will be reduced and $R_{\text{BLEED}}$ will be larger.
Bleeding Circuit

Max. bleeding current: Bleeding current during startup sequence and phase-cut time. Select this value lower than Max. $I_{BLD}$ (upper limit).

Higher Max. $I_{BLD}$ can have more margin to maintain input current higher than holding current during startup sequence.

Lower Max. $I_{BLD}$ can reduce the $SW_{BLD}$ temperature during startup sequence and AR time.

$R_{VDD}$ dampens leading edge spike noise into VDD pin. 100 ohm is recommended at high-line and 50 ohm is recommended at low-line.

BLD Circuit

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Max. I_{BLD}$ (upper limit)</td>
<td>111 mA</td>
</tr>
<tr>
<td>Max. $I_{BLD}$</td>
<td>96 mA</td>
</tr>
<tr>
<td>$R_{HBLD}$</td>
<td>108 kΩ</td>
</tr>
<tr>
<td>$R_{RLO}$</td>
<td>63 Ω</td>
</tr>
<tr>
<td>$R_{VDD}$</td>
<td>100 Ω</td>
</tr>
</tbody>
</table>

BLD Circuit

$C_{PD}$ is total EMI filter capacitor directly connected to transformer.

SRSP (sensing resistor short protection) is triggered when CS voltage is less than 0.1 V at first and second switching. When $L_m$ is highly designed, SRSP could be abnormally triggered due to low CS peak voltage. $R_{SRES}$ can protect system from abnormally triggered SRSP by building voltage offset on $R_{COMP}$. If CS peak is much higher than 0.1 V with small $L_m$, "open" message will appear and user doesn't need to add $R_{SRES}$.
Step 12 – BIAS Circuit

At high-line, $R_{BIAS}$ is 2 Mohm.
At low-line, $R_{BIAS}$ is 620 kohm.

$R_{BIAS}$ protects BIAS pin from leading edge spike.
At leading edge, $SW_{BIAS}$ $C_{BIAS}$ is quickly charged and the charging current spike could damage BIAS pin due to the over voltage.

$R_{BIAS}$ is generally 1kohm.
When $R_{BIAS}$ is too small, the current spike at leading edge will affect the BIAS.
When $R_{BIAS}$ is too big, $SW_{BIAS}$ current regulation is unstable.

$C_{BIAS}$ is generally 0.8 nF.
$C_{BIAS}$ protects BIAS pin from leading edge spike.
Step 13 – Active Damper Circuit

**Active Damper Circuit**

**Damper resistor**

Increase resistor value until mis-firing at leading edge is disappeared.
Larger damper resistor can help to remove shimmer by stabilizing leading edge moment.
So, user can also increase this value until shimmer is removed if shimmer is shown.

If $I_{DP[MAX]}$ is higher than this value, snubber voltage will be lower than desired snubber voltage in snubber design section.

Active damper biasing current is generally $0.3 \sim 1.0 \text{ mA}$.
If $I_{DP[MAX]}$ is too low, $SW_{on}$ gate rising time becomes longer which will increase $SW_{on}$ temperature with large switching loss.

**Recommended max. active damper current limit**

If $I_{DP[MAX]}$ is too large, current limit resistor ($R_{DP}$) should be too small which could occur unstable $SW_{on}$ turn-on.
If $I_{DP[MAX]}$ is too small, $R_{DP}$ will be larger which causes larger power loss with lower efficiency.

Active damper current limit resistor

Delay capacitor for active damper switch turn-on
$C_{DP}$ is generally $10 \text{ nF}$.
Check if input current ringing is almost dampened after leading edge.
If $SW_{on}$ is turned on after enough damping, $C_{DP}$ is appropriate value.
Active Damper Circuit

Minimum snubber voltage at ND.MODE. Enter the snubber voltage at zero crossing voltage.

V_{TH,DP} is generally 30 V and should be lower than V_{VARSUPD}.
If SW_{EP} is always turned on at max. phase angle condition, increase V_{ZD,DP}.
If SW_{EP} gate is turned off with efficiency drop at no dimmer condition, reduce V_{ZD,DP}.

<table>
<thead>
<tr>
<th>Active Damper Circuit</th>
<th>V_{VARSUPD}</th>
<th>V_{ZD,DP}</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>55 V</td>
<td>6.2 V</td>
</tr>
</tbody>
</table>
Related Resources

**FL7734 – Single-Stage Primary-Side-Regulation PWM Controller for PFC and Phase Cut Dimmable LED Driving**

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