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Implementing the Physical Layer in a USB 2.0 Compliant System

Overview

This application note discusses system level design considerations that need to be followed when implementing the physical layer using a discrete transceiver into a Universal Serial Bus (USB) 2.0 compliant system. Special consideration is taken to fully comply with USB 2.0 specification requirements. Proper signal termination as well as correct upstream-downstream configuration requirements will be discussed. Also, this application note covers some of the challenges which arise when voltage translation is needed between low voltage controllers and the higher voltage physical layer devices and how these challenges are overcome.

What is USB 2.0?

Before exploring the details of implementing a USB 2.0 compliant physical layer it is necessary to have a consistent understanding of what it means to be USB 2.0 compliant. A look at the history of the USB specification reveals that prior to the release of USB 2.0, the most updated specification was USB 1.1. The USB 1.1 specification predated the release of high speed USB (480Mbps) and as a result only covered full speed (12Mbps) and low speed (1.5Mbps) operation. The USB 2.0 specification was released specifically for the purpose of addressing the emergence of high speed devices designed to deal with high bandwidth applications like streaming video. To be considered USB 2.0 compliant means that the transceiver must meet all the requirements of the USB 2.0 specification that apply to it whether it is a low speed, full speed, or a

high speed device. When dealing with transceivers, the specification provides different requirements for certain specifications depending on whether or not the part is full speed (12Mbps) or high speed (480Mbps) capable. This explains why many full speed capable transceivers like the USB1T20, USB1T1102, and future devices like the USB1T1104 and USB1T1105 are still USB 2.0 compliant. These devices are forward compatible with high speed capable ports that are shipped on many PCs today. At this time full speed transceivers are still the most prevalent implementation of the physical layer.

Signal Termination

One of the areas where the specification distinguishes between full speed and high speed is in the proper series termination on the transmission line. For example, when using a full speed (12Mbps) buffer in a USB 2.0 compliant system, it is necessary to place a series resistor on the D+ and D- pins external to the transceiver. This placement is a result of the need to properly match the impedance of the specified transmission line having a differential characteristic impedance (Z_0) of 90Ω and a single ended impedance of 45Ω. To match this load, it requires that the full speed transceiver output impedance must be in the range 28Ω to 44Ω. In order to properly match the impedance of the transmission line the output drive characteristics must fall within the gray shaded regions of Figure 1 and Figure 2. The figures are referenced directly from the USB 2.0 specification.

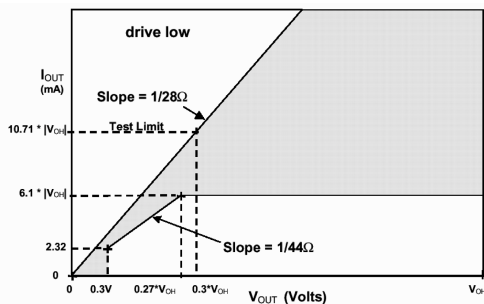


FIGURE 1.
 Full Speed Buffer V/I Characteristics Driving Low
 (page 126 USB 2.0 Specification)

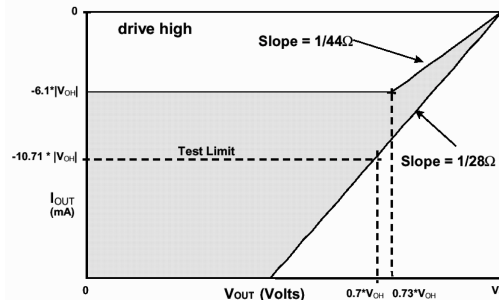


FIGURE 2.
 Full Speed Buffer V/I Characteristics
 (page 126 USB 2.0 Specification)

Signal Termination (Continued)

Because the characteristic output impedance of the signaling pins is actually much smaller than the total required for proper load matching, it is necessary to place external series resistor on these pins. The resistor value can be anything needed in order to ensure the total impedance seen by the transmission line stays within the 28Ω to 44Ω range. (See Figure 3)

This variation in the series termination resistors is due to differences in output drive impedance characteristics of the

buffer which is attributed to the chosen process and design techniques employed. For example, USB1T11A specifies an external series resistor of 24Ω which allows its combined series output impedance to stay within this range while the USB1T1102 suggests 29Ω. By staying within the gray regions of Figure 1 and Figure 2 this will ensure that the specified V_{IH} levels of the receiving transceiver are satisfied and result in a clean eye diagram. See Figure 4 for an example of what a clean eye diagram should look like.

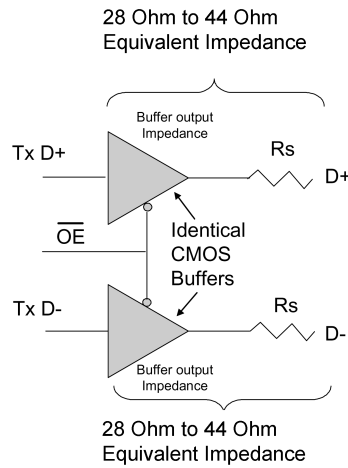


FIGURE 3. Simplified Schematic of Output Buffers and Series Termination

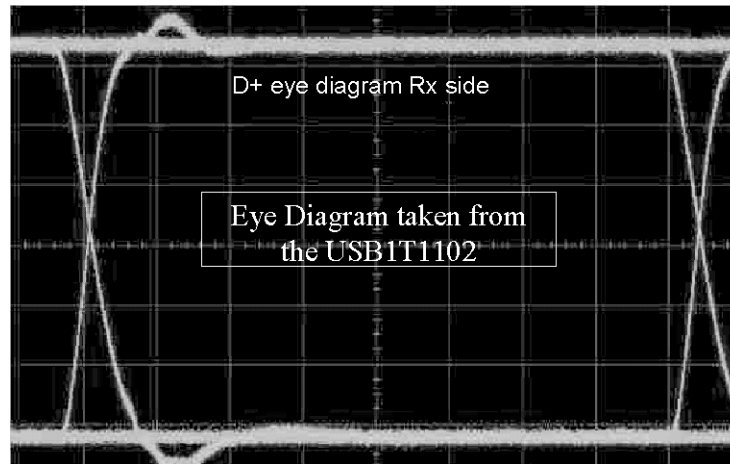


FIGURE 4. Eye Pattern for USB1T1102

Upstream/Downstream Configurations

It is also important to know how to properly configure the transceivers relative to their location in the system. First, it must be determined whether the device is in the upstream or downstream position relative to the host. Simply put, this means that transceivers on the host side are considered to be downstream devices and those on peripheral side are considered to be upstream configured. An easy way to remember this is to ask yourself in what direction, relative to the host, does the transceiver send data to. If the transceiver is on the host side, it sends data downstream away from the host. If the transceiver is on the peripheral side, data is sent upstream back to the host. If a transceiver is on the host side, $15k\Omega \pm 5\%$ pull-down resistors must be connected to both the D+ and D- pins. This is true for low, full, and high speed transmit speeds. With no hub or peripheral attached these pull-down resistors will condition the D+ and D- pins LOW. When both D+ and D- are less than $V_{OL(max)}$ this signals a Single Ended Zero (SE0) state on the Host side which the Host side controlling ASIC monitors, telling it that data transmission is not possible in this condition.

On the upstream facing side there are two different configurations, one for low speed transmission and one for full or high speed transmission. When configuring for full speed data transmission, a $1.5k\Omega \pm 5\%$ pull-up resistor is con-

nected between the D+ line and the 3.3V V_{pu} output. Upon connection of the peripheral to the host through the USB cable, the host side controller is signaled that a Peripheral is present. This is accomplished by the $1.5k\Omega$ pull-up resistor which over comes the $15k\Omega$ pull-down on the host side signaling a "Differential 1". This tells the host to prepare for full or high speed transfer. A "Differential 1" is defined as the state where D+ is greater than $V_{OH(min)}$ and D- is less than $V_{OL(max)}$.

When configuring for low speed data transmission the peripheral is configured to send a "Differential 0". In this case a "Differential 0" is defined as the state where D+ is less than $V_{OL(max)}$ and D- is greater than $V_{OH(min)}$. This is accomplished by placing a $1.5k\Omega \pm 5\%$ pull-up resistor connected between the D- line and 3.3V V_{pu} output. Again many transceivers provide a regulated pull-up voltage for this purpose. When using this configuration as soon as the peripheral is connected to the host, with V_{bus} present, the $1.5k\Omega$ pull-up resistor overcomes the $15k\Omega$ pull-down resistor and signals a "Differential 0" to the host telling it to prepare for low speed data transfer. For a graphical representation of these concepts please refer to Figure 5.

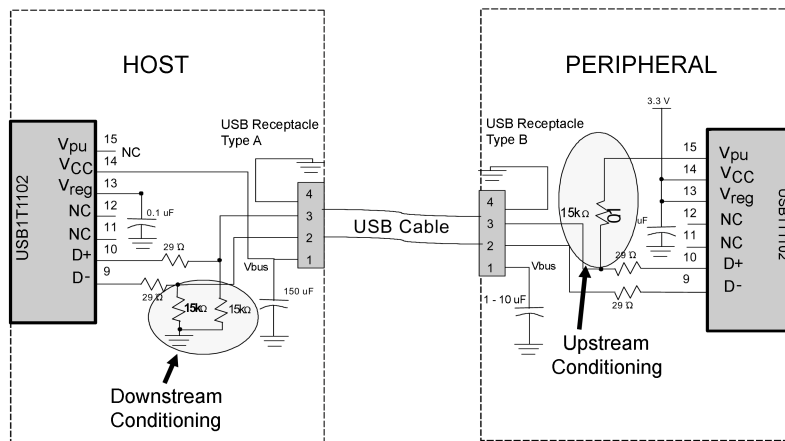


FIGURE 5. Typical Example of a USB Physical Layer using USB1T1102 Full Speed Transceivers

System Power Configuration

In general, there are three different power configurations possible on the physical layer. These are Root Port Hubs, Bus-Powered Hubs, and Self-Powered Hubs. Figure 6 depicts a Root Port Hub powered configuration and is characterized by using the same power supply for both the host and hub. Figure 7 shows a Self Powered Hub configuration which means that the host and hub each have their own separate power supplies. The final configuration is the Bus Powered configuration where the Hub is powered via Vbus.

In all three figures the USB transceivers in the peripherals get power either through Vbus or from the peripheral power supply. Typically, designers will opt for the first option when working with ultra portable devices which are very power consumption conscious and prefer to use Vbus supplied power whenever possible to extend battery life of the device.

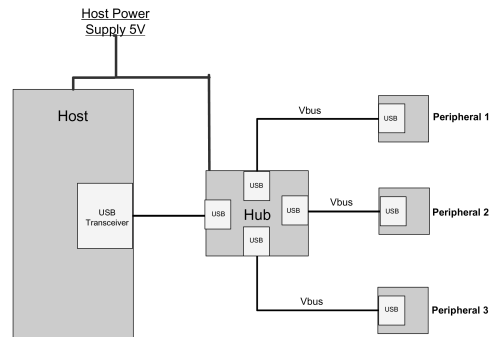


FIGURE 6. Root Port Hub

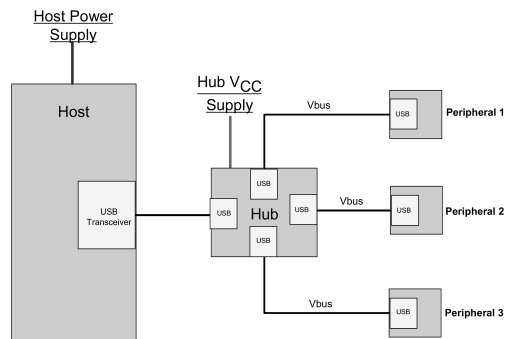


FIGURE 7. Self Powered Hub

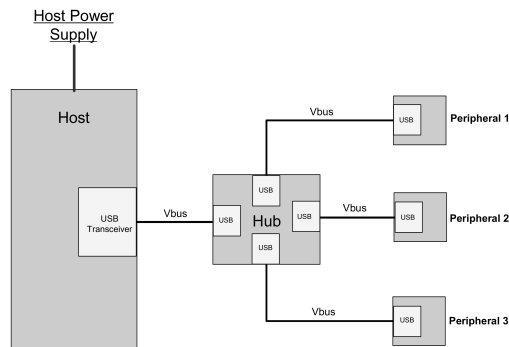


FIGURE 8. Bus Powered Hub

Normal and Bypass Mode Configurations

Because there are multiple powering configurations possible for the physical layer and different power supplies from different sources are often at different voltage levels this requires the transceiver to be adaptable to whatever power supply configuration is chosen. The USB 2.0 specification requires that the signaling on the D+, D- lines be within 0V to 3.3V rails however the host supplied V_{CC} and subsequently V_{bus} is 5V. For this reason newer USB transceivers have internal voltage regulators built-in that translate the 5V V_{bus} down to 3.3V for use in data transmission. This is true for both the upstream and downstream facing transceivers. To accommodate this need the transceivers allow for either a 5V or 3.3V power supply. When using a

5V supply either from V_{bus} the Host or Hub power supply, V_{REG} is supplied with a 3.3V regulated output by the transceiver. When operating from a 5V rail in this manner it is referred to as "Normal Mode". A second option for the physical layer is called "Bypass Mode". This power configuration is possible when there is a 3.3V supply available to the transceiver (many handheld peripheral devices operate in this range and are capable of supplying the transceiver directly). V_{REG} and V_{CC} are then tied together and connected to the 3.3V power supply. Because the voltage regulator is effectively turned off in the configuration this mode is called Bypass Mode. Figure 9 and Figure 10 are examples of both normal and bypass configurations.

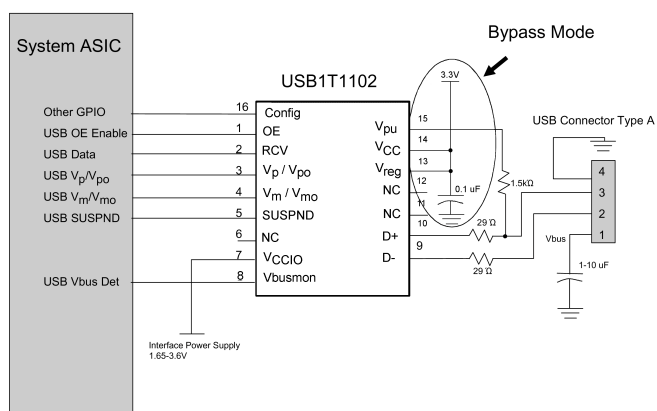


FIGURE 9. Upstream Connection in Bypass Mode with Differential Outputs

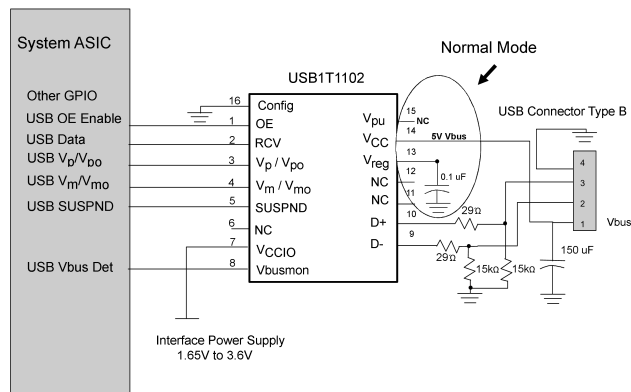


FIGURE 10. Downstream Connection in Normal Mode with Differential Outputs

Interfacing with Mixed Voltage Control Signals

One final consideration to be addressed when implementing the USB physical layer is how to deal with the interface between the higher voltage physical layer device and lower voltage USB controllers. Many USB controllers are no longer independent devices or even part of the transceiver but have been integrated into small line width ASICs. Many of these ASICs operate at very low voltages in the range of 1.8V which causes a potential problem when trying to communicate with the physical layer. If we tried to send a 3.3V level control signal back into 1.8V ASIC this would at the

very least shorten the life of the ASIC and in the worst case cause reverse breakdowns leading to major current consumption and device failure. To overcome this problem physical layer devices allow their control outputs and data I/O pins to be conditioned to whatever voltage is required by the USB controller. This conditioning is accomplished by allowing the controller or system designer to condition the transceiver outputs by placing the required output rail voltage on an input control pin, labeled V_{CCIO} .

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