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Application Note 7531

Implementing A Primary Side Peak-Current-Mode Half-Bridge Converter

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Abstract - Peak-current-mode (PCM) half-bridge push-pull power converters are inherently unstable as a result of volt-seconds circuit asymmetry [1], [2]. A proposed approach [3] is sensitive to circuit asymmetry and overload operation. A new PCM half-bridge converter with transformer isolation is proposed. The proposed converter uses an auxiliary winding and two diodes with a modified current sense to obtain pulse-by-pulse PCM control that is effective under both normal and fault operating modes. Therefore, the possibility of magnetic saturation due to circuit operation asymmetry is eliminated. The auxiliary transformer winding consists of a small gauge wire having the same number of turns as the primary winding. Operation of a 120W design was verified and has been deployed on the space station program.

I. Introduction

The half-bridge push-pull converter is an attractive topology in applications having high bus voltages at intermediate power levels. Important criteria are that the design be amenable to fabrication while remaining economical. An operating limitation of this topology is its inherent instability when PCM feedback is used for control [1], [2], [4], [5] due to charge asymmetry from

- Mismatched switching propagation delays
- Even-order sub-harmonic oscillation of a feedback loop [5]
- Power transformer construction asymmetry
- Differences in C1 and C2 coupling capacitor values

II. Uncompensated Balancing Winding Operation

A voltage balancing winding enhancement was introduced in [3] and is shown in Figure 1. The balancing winding is implemented using a small gauge coupled winding in the power transformer, T_{1b}, having the same number of turns as the primary winding. Although this circuit is a significant topology improvement (a half-bridge push-pull PCM topology cannot be implemented without a balancing winding), an instability mode remains.

Balancing winding T_{1b} is connected between the center points of coupling capacitors C1 and C2, and the junction point of diodes D1 and D2 with polarity shown in Figure 1. The balancing winding conducts to charge the lower voltage capacitor when the opposing transistor from the loop having the higher voltage capacitor conducts. In the

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subsequent discussion, the capacitance of C2 is assumed to be greater than that of C1 such that $V_{C1} > V_{C2}$. Balancing winding current conducts through diode D2 when Q1 turns-on.

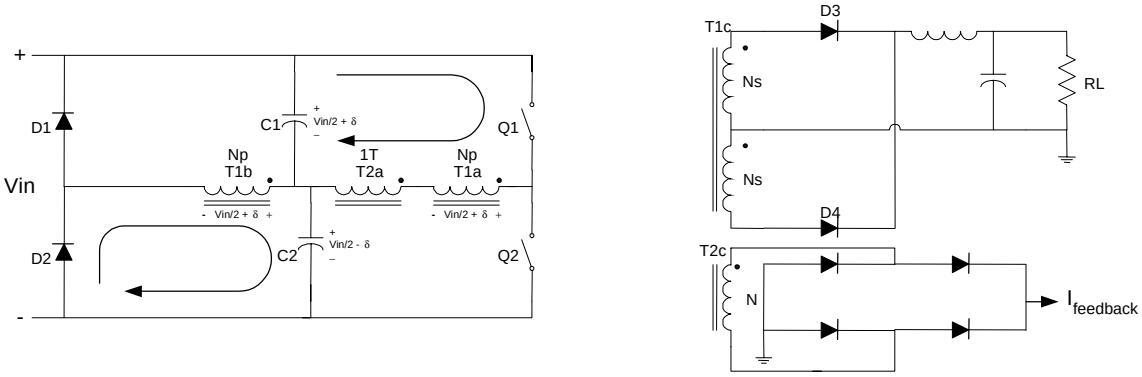

Figure 1 Uncompensated balancing winding

Under normal mode operation, balancing winding conduction ceases before the end of the duty cycle (Figure 2). The signal fed to the current feedback loop by the current transformer winding T_{2c} at the end of the conduction cycle is an accurate representation of the transformed current from T_{2a}. Hence, no modifications to standard feedback loop control are required.

The voltage of storage capacitors C1 and C2 as a function of load, balancing winding leakage inductance and resistance, and transistor $R_{ds(on)}$ have important performance implications.

Selecting C1 and C2 with insufficient capacitance or excessive parasitic voltage drops during conduction hinders the effectiveness of the balancing winding. The maximum capacitor ripple voltage between the beginning and end of the transistor conduction cycle must not exceed the voltage drop of a balancing diode.

If the C1, C2 ripple voltage is excessive under normal mode operation, the balancing winding will conduct at the beginning of each cycle, increasing the possibility that the balancing winding conduction time will exceed the duty cycle duration. The current feedback loop will no longer represent the load current and the current feedback loop transfer function will change.

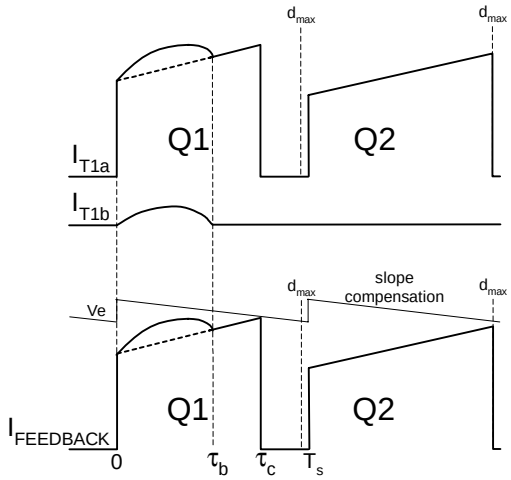

Figure 2 Uncompensated current feedback signal

Equivalent series resistance (ESR) and equivalent series inductance (ESL) introduced by storage capacitors, PCB traces, and transistors also impact the balancing winding conduction time. The balancing winding leakage inductance is dominant over circuit layout ESL, and is dependent on the design of the power transformer.

The balancing winding conducts at Q1 turn-on when $(V_{C1}-V_{C2}) > (V_{D2} + V_{Q1})$. The rate of rise of the balancing winding current is inversely proportional to the leakage inductance per expression (1). A large leakage inductance

can result in the balancing winding having insufficient conduction time available to charge the lower voltage coupling capacitor.

$$\frac{di}{dt} = \frac{V_{T1b} - V_{C2} - V_{d2}}{L} \quad \text{where} \quad V_{T1b} = V_{C1} - V_{Q1} \qquad (1)$$

The rapid response from PCM control protects the switches from excessive current that results from transformer saturation. The shorter conduction cycle is terminated sooner by the detection of magnetic saturation. The longer conduction cycle is limited by the maximum duty cycle (<50%) capability of the controller. Unstable operation will occur as time asymmetry increases [1], [2], [5].

III. Implementation Of The Uncompensated Balancing Winding

The purpose of the charge balancing winding is to equalize the voltage between coupling capacitors C1 and C2, permitting PCM control operation. The charging voltage available to capacitor C2 is the difference between the transformer balancing winding voltage across T_{1b}, the sum of capacitor voltage V_{C2} and the diode voltage drop V_{D2}. Less than a volt would typically be available, resulting in a balancing winding leakage inductance limited di/dt charging rate per expression (1). When $V_{C1} > (V_{in} - V_{C2} - V_d - V_Q)$ and Q1 conducts, the balancing winding conducts current as in Figure 3. T_{2c} provides the feedback current information which includes balancing winding current, the power transformer magnetizing current and output current information.

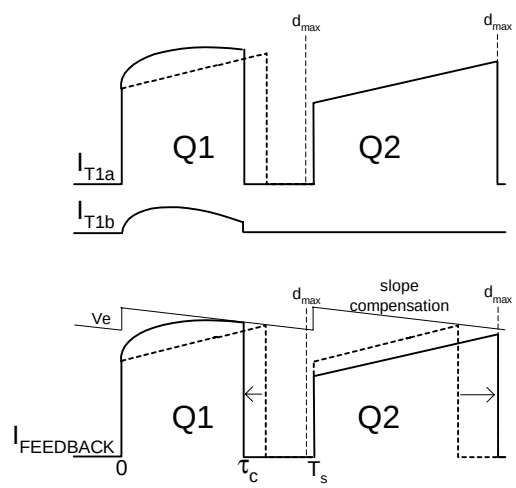

Figure 3 Uncompensated current feedback signal

The balancing winding current I_{T1b} may require a substantial time interval to properly charge the coupling capacitor. The cycle during which the balancing winding conducts may end prematurely. The extra current from the balancing winding is included in the current feedback control signal and may intercept the control signal V_e. If the two signals intercept while the balancing winding is conducting, Q1 will turn-off prematurely preventing C1 and C2 from completing their charge balancing.

If this occurs, the potential difference between capacitors C1 and C2 will increase cycle-by-cycle. Q2 conduction cycle will increase until the controller imposed duty cycle limit d_{max} is reached. The duty cycle time of Q1 is shortened as a result of the control current signal interception with the programmed error signal V_e. Operational instability and transformer magnetic saturation will result.

IV. Implementation Of The One-Turn Compensated Balancing Winding

Figure 4 illustrates a circuit modification for removing the balancing winding current from the controller current sense signal. When $V_{C1} > (V_{in} - V_{C2} - V_{D2} - V_{Q1})$, the balancing winding current conducts as in Figure 4. T_{2a} is coupled to T_{2b}. Current sensed by T_{2b} is subtracted once from that of T_{2a} such that C1, C2 balancing current is not

present in the current sense winding T_{2C}. The feedback loop signal is now an exact representation of the output current, preventing the early cycle termination condition described for the uncompensated circuit.

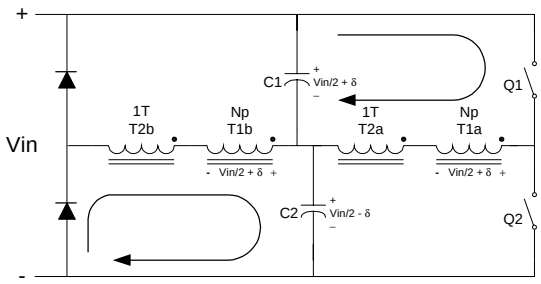

Figure 4 One-turn compensated balancing winding

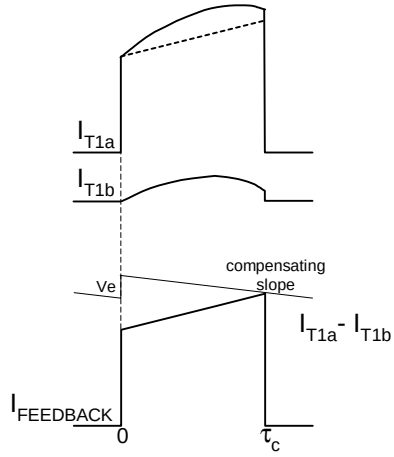

Figure 5 One-turn compensated current feedback signal

The rate of rise of the balancing winding current is limited by the balancing winding leakage inductance per expression (1). During current limit operation, maximum duty cycle is reduced and Q1 may turn-off before the balancing winding has had time to finish charging C2 and while the balancing winding is still conducting (Figure 5). Conduction ends before V_{C2} is balanced with V_{C1}. The condition will deteriorate cycle-by-cycle resulting in operational instability and transformer saturation.

V. Implementation Of The Two-Turn Compensated Balancing Winding

Figure 6 illustrates a further circuit enhancement that ensures stable operation even for short conduction pulse widths associated with overload conditions. A one-turn T_{2a} in series with the primary is coupled to a two-turn T_{2b} in series with the balancing winding. The current in the balancing winding is thus subtracted twice from that being sensed in the primary. As shown in Figure 4, the first subtraction is required to provide the current feedback loop with an accurate representation of the output current, preventing an early termination of the duty cycle during normal operation. A second subtraction is required under current limiting operation to extend the duty cycle while the balancing winding conducts, preventing transformer saturation (Figure 7).

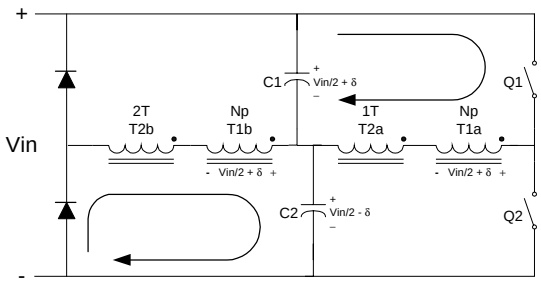

Figure 6 Two-turn compensated balancing winding

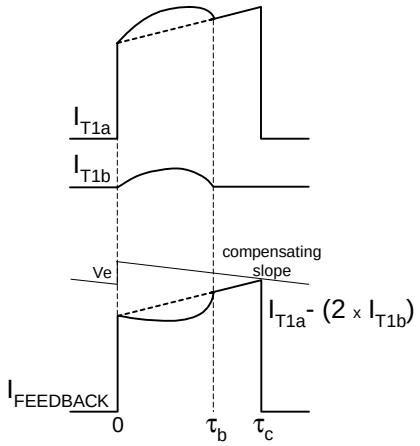

Figure 7 Two-turn compensated current feedback signal

Referencing Figure 7, before the end of the conduction cycle, the balancing winding ceases conduction and the current feedback loop will have an accurate representation of the output current. Under normal operation, the balancing winding current returns to zero before the end of the duty cycle and will not affect the characteristics of the controller feedback loop.

If the balancing winding is conducting current when the duty-cycle would normally terminate, the impact of the second balancing current subtraction is to reduce the current sense signal, extending the duty-cycle of Q1.

During current limit mode, instability is prevented because the balancing winding conduction resonates to zero before Q1 turns-off. Power transformer volt-seconds balance is achieved, preventing operational instability and transformer saturation. The balancing diode will have a slight, but negligible effect in offsetting the centering of the transformer B-H curve.

VI. Simulations And Discussion

Expression (2) provides an analytical representation of the balancing winding current waveform from Figure 6. Expression (3) provides an analytical representation of the coupling capacitor voltage being charged by the balancing winding and the primary current. Circuit parasitics are included.

These expressions are valid during balancing winding current conduction $0 \le t \le \tau_b$, where τ_b is the winding current conduction time.

$$i(t) = K1 \cdot e^{a \cdot t} \cdot \sin(b \cdot t) + K2 \cdot \left(1 - \left(\cos(b \cdot t) - \frac{a}{b} \cdot \sin(b \cdot t)\right) \cdot e^{a \cdot t}\right) + K3 \cdot \left(\frac{2 \cdot a - e^{a \cdot t} \cdot \left(2 \cdot a \cdot \cos(b \cdot t) + \frac{b^2 - a^2}{b} \cdot \sin(b \cdot t)\right)}{a^2 + b^2} + t\right) \qquad (2)$$

where

$$K1 = \frac{V_{in} - V_d - 2 \cdot V_{C2i} - r_1 \cdot I_a}{L \cdot b}$$

$$K2 = \frac{-1}{L \cdot (a^2 + b^2)} \cdot \left(\frac{r_1 \cdot \delta I}{\tau_c} + \frac{2 \cdot Ia}{C1 + C2}\right)$$

$$K3 = \frac{-2 \cdot \delta I}{L \cdot \tau_c \cdot (C1 + C2) \cdot (a^2 + b^2)}$$

$$a = -\left(\frac{r_1 + r_2}{2 \cdot L}\right)$$

$$b = \sqrt{\frac{2}{L \cdot C2} - \left(\frac{r_1 + r_2}{2 \cdot L}\right)}$$

Circuit parameters are defined as:

- r_1 = MOSFET $R_{ds(on)}$ = 0.16
- r_2 = balancing winding resistance = 0.168
- C1 = 8.3µF
- C2 = 8.5µF
- L = balancing winding leakage inductance = 0.73µH
- V_{in} = bus voltage = 120V
- V_d = balancing winding resistance = 0.84V
- V_{C1i} = capacitor voltage before Q1 conduction = 61.2V
- V_{C2i} = capacitor voltage before Q1 conduction = 58.8V
- δI = output ripple current reflected to the primary winding during τ_c = 1.05A
- I_a = initial primary current at transistor turn-on = 4.77A
- τ_c = duration of duty cycle = 4.19µs

$$v_{C2}(t) = \frac{1}{C1 + C2} \cdot \left(Ia \cdot t + \frac{\delta I \cdot t^2}{2 \cdot \tau_c}\right) + \frac{V_{in} - V_d - 2 \cdot V_{C2i} - r_1 \cdot I_a}{b \cdot L \cdot C2} \cdot \left(\frac{e^{at}}{a^2 + b^2} \cdot (a \cdot \sin(b \cdot t) - b \cdot \cos(b \cdot t))\right) - \frac{\frac{r_1 \cdot \delta I}{\tau_c} + \frac{2 \cdot I_a}{C1 + C2}}{L \cdot C2 \cdot (a^2 + b^2)} \cdot \left(t - \frac{e^{at}}{a^2 + b^2} \cdot (a \cdot \cos(b \cdot t) + b \cdot \sin(b \cdot t)) + \frac{a}{b} \cdot \frac{e^{at}}{a^2 + b^2} \cdot (a \cdot \sin(b \cdot t) - b \cos(b \cdot t))\right) -$$

$$\frac{2 \cdot \delta I}{L \cdot C2 \cdot (C1 + C2) \cdot \tau_c \cdot (a^2 + b^2)} \cdot \left(\frac{2 \cdot a \cdot t}{a^2 + b^2} + \frac{t^2}{2} - \frac{2 \cdot a \cdot e^{at}}{(a^2 + b^2)^2} \cdot (a \cdot \cos(b \cdot t) + b \cdot \sin(b \cdot t)) + \frac{(a^2 - b^2) \cdot e^{at}}{b \cdot (a^2 + b^2)^2} \cdot (a \cdot \sin(b \cdot t) - b \cos(b \cdot t))\right) + Z \qquad (3)$$

where

$$Z = \frac{V_{in} - V_d - 2 \cdot V_{C2i} - r_1 \cdot I_a}{L \cdot C2 \cdot (a^2 + b^2)} + V_{c2}i + \frac{2}{L \cdot C2 \cdot (a^2 + b^2)^2} \cdot \left(\frac{\delta I \cdot (b^2 - 3 \cdot a^2)}{(C1 + C2) \cdot (a^2 + b^2) \cdot \tau_c}\right) - a \cdot \left(\frac{r_1 \cdot \delta I}{\tau_c} + \frac{2 \cdot I_a}{C1 + C2}\right)$$

Circuit parasitics have a dampening effect on the balancing winding current waveform. The effect of these parasitic elements is illustrated in Figures 8, 9, 10 and 11.

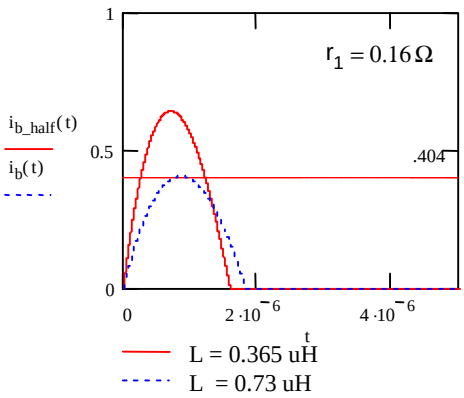

Figure 8 Influence of leakage inductance on balancing winding current

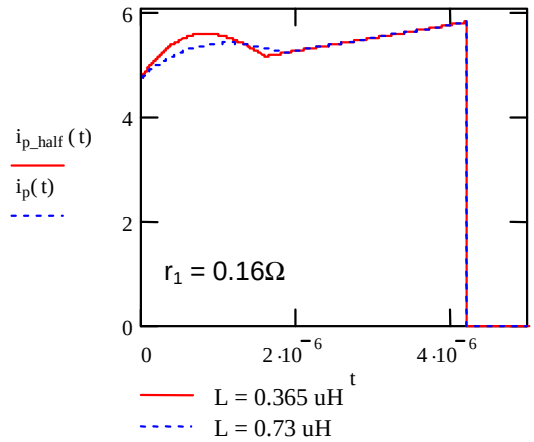

Figure 9 Influence of leakage inductance on primary winding current

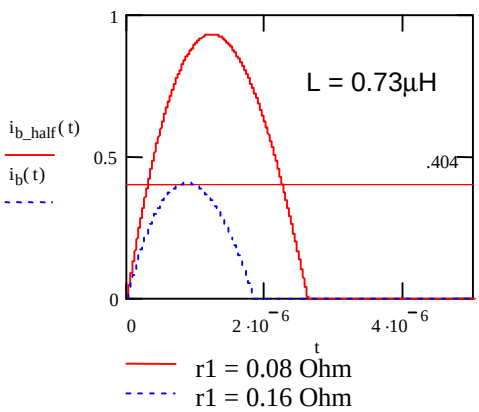

Figure 10 Influence of transistor $R_{ds(on)}$ on balancing winding current

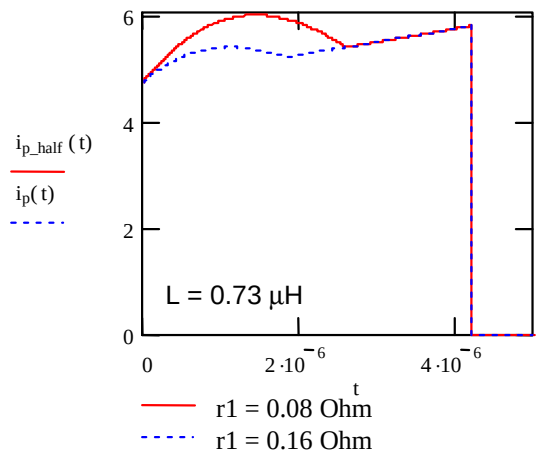

Figure 11 Influence of transistor $R_{ds(on)}$ on primary winding current

A larger leakage inductance results in a balancing winding current having a lower natural frequency and amplitude. The effect on the capacitor charge is a reduction of available energy in the pulse to balance the coupling capacitor. A larger number of pulses are required to restore balance to the capacitor.

A larger circuit resistance (from the transistor, the transformer winding and board traces) results in balancing winding current of lower amplitude and higher natural frequency. Available charging energy to the coupling capacitor is reduced.

The voltage unbalance between C1 and C2 (2.4V) in these simulations is large and was selected for purposes of analysis. Under operation, the balancing winding would restore the balance within a few conduction cycles.

Verification of expressions (2) and (3) could not be performed in circuit for the large voltage imbalance used in this analysis. Instead, validation of these expressions was reached via a Spice implementation of the circuit from Figure 6. Simulation results are shown in Figure 12.

VII. Test Results

Correlation between the numerical analysis and simulation results are very good. The numerical analysis provided a peak balancing winding current of 404 mA versus 406 mA from the Spice simulation, a difference of 0.5%.

This design has been verified in a 120W power supply in the space station program. The power supply has been deployed and is in service.

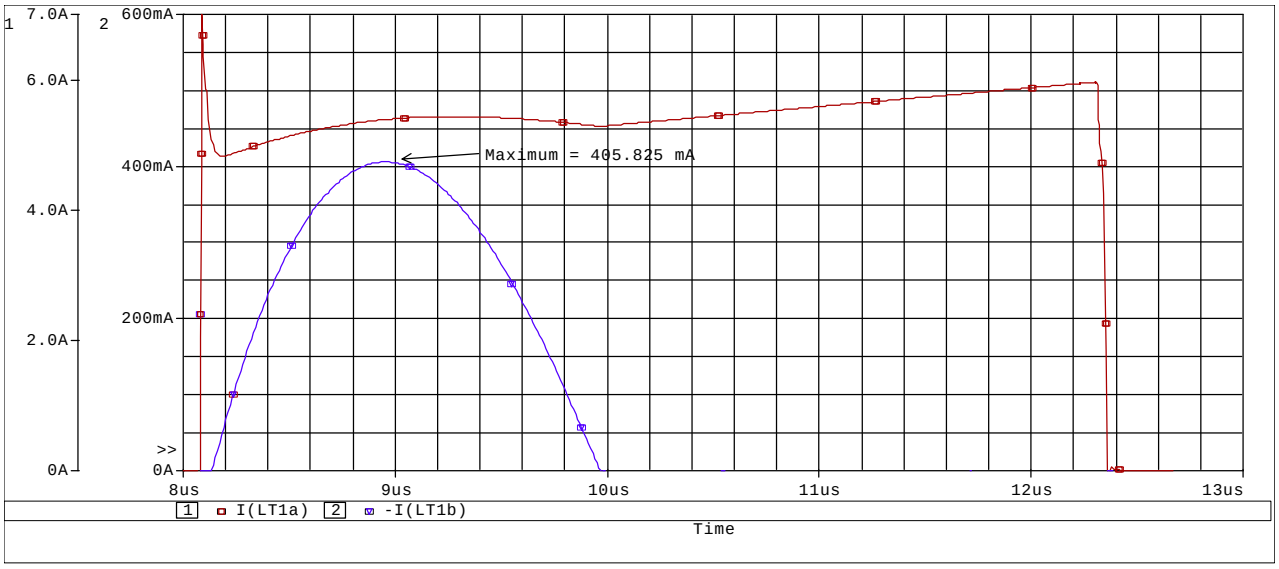

Figure 12 Spice simulation results

VIII. Conclusion

An economical and easily implemented method for designing a PCM half-bridge push-pull power converter with transformer isolation has been described. This design has proven itself to be both rugged and reliable, eliminating the instance of transformer saturation under both normal and fault operating modes.

Excellent correlation between the analytical expressions and the Spice simulation was achieved.

IX. Acknowledgement

The authors wish to thank EMS Technologies Canada Limited for their support in preparing this paper.

Thanks are also extended to Ron H. Randall for his editorial assistance in the preparation of this document.

X. References

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[5] Unitrode Application Note U-97; "Modeling, Analysis And Compensation Of The Current-Mode Converter".

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