AN-7730
FL7730 Design Tool Flow

Overview
This document is intended to provide in-depth guidance to using the Fairchild Design Tool for FL7730. Use the Design Tool with the product datasheet.

Figure 1. Design Flow
Step 1 — Enter Input Output Specification

Input Output Specification

Blue box is input from user. Red box is calculated output.

<table>
<thead>
<tr>
<th>Input Spec</th>
<th>Min. Vin</th>
<th>90</th>
<th>Vac</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Max. Vin</td>
<td>140</td>
<td>Vac</td>
</tr>
</tbody>
</table>

| Output Spec | Vout | 22  | V   |
|             | Max. Vout | 28  | V   |
|             | Iout | 380 | mA  |
|             | Pout | 8.36| W   |

Max. Vout is OVP level.

Step 2 — Transformer Design

Transformer Design

Max. duty is generally between 20%~50%. High max. duty = · Low conduction loss. Suitable for low-line. Low max. duty = · More Bmax margin. Suitable for high-line.

Max. Ton should be less than 10us.

This switching frequency is the operating frequency at the rated Vout condition. The switching frequency should be less than 65kHz.

Max. Vcs is max. peak CS voltage. Enter Max. Vcs less than 0.67V because pulse by pulse CS voltage limit is 0.67V. Higher Nps makes higher max. Vcs in the primary side CC regulation. So, when max. Vcs is highly set, Nps becomes higher.

Enter Np over Np min. If Np is too big to fit in transformer window, reduce Max. Duty.

Make transformer according to the above spec. Then, enter Lk (Leakage inductance) after measuring.

Step 3 — Snubber Design

Snubber Design

Vsn is snubber voltage. Vsn is generally set as 2~2.5 times Nps·Vo.

ΔVsn is generally set as 5% ripple of Vsn.
Step 4 — Control Circuit Design

- **Rcc** is line CC compensation resistor. When **Iout** becomes higher at higher input voltage, increase **Rcc**. **Rcc** should be limited less than 500ohm. Large **Rcc** can make CS noise, inducing **Vcs** peak detection error.

<table>
<thead>
<tr>
<th>Control Circuit Design</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Rsense</strong></td>
<td>0.593767 ohm</td>
</tr>
<tr>
<td><strong>Rcc</strong></td>
<td>100 ohm</td>
</tr>
<tr>
<td><strong>Vin.bnk</strong></td>
<td>50 V</td>
</tr>
<tr>
<td><strong>Vf</strong></td>
<td>0.5 V</td>
</tr>
<tr>
<td><strong>Rsv1</strong></td>
<td>165.2367 kohm</td>
</tr>
<tr>
<td><strong>Rsv2</strong></td>
<td>19.75502 kohm</td>
</tr>
<tr>
<td><strong>CV</strong></td>
<td>10 pF</td>
</tr>
<tr>
<td><strong>Ccomi</strong></td>
<td>1 uF</td>
</tr>
<tr>
<td><strong>Cvdd</strong></td>
<td>33 uF</td>
</tr>
<tr>
<td><strong>Dvdd-Vmax</strong></td>
<td>73.95584 V</td>
</tr>
<tr>
<td><strong>Rstr</strong></td>
<td>155.8442 kohm</td>
</tr>
</tbody>
</table>

- **Vin.bnk** is COMI/VS blanking level. COMI blanking: Error amp. input is fixed, working as open loop. VS blanking: VS voltage detection is disabled. **Vin.bnk** is generally set as 30–70V.

- **Vf** is secondary diode forward voltage.

- **Cvs** is VS filter capacitor, generally set as 10–30pF.

- **COMI** capacitor is generally 0.68–3.3uF. Check output voltage overshoot at startup in max. **Vin** condition. If output voltage overshoot is too big, increase **Ccomi**.

- **Vdd** capacitor is generally in 10–47uF. If **Vdd** drops too close to **Vdd-off** at startup, increase **Cvdd**.

Step 5 — Power Device Design

<table>
<thead>
<tr>
<th>Power Device Design</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MOSFET Vmax</strong></td>
<td>397.9899 V</td>
</tr>
<tr>
<td><strong>MOSFET Ipk</strong></td>
<td>0.842082 A</td>
</tr>
<tr>
<td><strong>Diode Vmax</strong></td>
<td>89.4245 V</td>
</tr>
<tr>
<td><strong>Diode Ipk</strong></td>
<td>2.714286 A</td>
</tr>
</tbody>
</table>

- **Vmax** is MOSFET drain-source maximum voltage. **Ipk** is MOSFET peak current.

- **Vmax** is maximum reverse voltage of secondary diode. **Ipk** is peak current of secondary diode.
Step 6 — DIM Detection Circuit Design

<table>
<thead>
<tr>
<th>DIM Detection Circuit Design</th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ZDdim</td>
<td>11V</td>
<td></td>
</tr>
<tr>
<td>Rdim1</td>
<td>1Mohm</td>
<td></td>
</tr>
<tr>
<td>Rdim2</td>
<td>75kohm</td>
<td></td>
</tr>
<tr>
<td>Rdim3</td>
<td>62kohm</td>
<td></td>
</tr>
<tr>
<td>Cdim</td>
<td>3.3µF</td>
<td></td>
</tr>
</tbody>
</table>

Zener voltage of ZDdim is generally in 10~40V.
Rdim1 is generally around 1Mohm.
If Rdim1 is too small,
- efficiency is reduced.
- Dim pin voltage is changed a lot when line voltage changes.
If Rdim1 is too big,
- ZDdim biasing current becomes too small, inducing error in dimming angle detection.

TRIAC dimmers have different max. dimming angle.
So, Rdim2/3 can not be calculated and found by testing with dimmers.
Rdim2/3 are tens to hundreds kohm.
Rdim2/3 determine dimming control range.
For wider dimming control range, reduce Rdim2 and Rdim3.
(But, wider dimming control makes higher flicker possibility specially in high-line and low output power condition.).

Cdim is 0.1~5µF as a filter to supply DC voltage to Dim pin.
If Cdim is too big, Dim pin voltage rises slowly at startup and it can affect powering speed.

Step 7 — Passive Bleeder Design

<table>
<thead>
<tr>
<th>Passive Bleeder Design</th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Cbleeder</td>
<td>330nF</td>
<td></td>
</tr>
<tr>
<td>Rbleeder</td>
<td>0.5kohm</td>
<td></td>
</tr>
</tbody>
</table>

Cbleeder is generally 47~470nF.
If Cbleeder is increased,
- Flicker is relieved.
- Efficiency and PF become worse.

Rbleeder is determined after selecting Cbleeder.
Rbleeder is generally 0.1~10kohm.
Too big Rbleeder limits bleeder current, which makes flicker.
Too small Rbleeder induces input current ringing at dimmer firing, which also can make flicker.

So, change Rbleeder by checking input current at firing.
Find the min. Rbleeder to satisfy below.
- input current at firing is higher enough than dimmer holding current.
- there is no mis-fire right after firing.
The min. Rbleeder is proper value for no flicker and high efficiency.
Step 8 — Active Damper Design

R\text{damp} is generally 10–1kohm. R\text{damp} is to limit input spike current at fire and remove flicker. Large R\text{damp} can considerably reduce spike current and remove flicker, but it will reduce efficiency.

So, find min. R\text{damp} to satisfy below without active damping circuit.
- Input spike current at 90° dimming angle is less than customer spec.
- There is no flicker caused by R\text{damp} current ringing.
  (Check input current and R\text{damp} current at the same time. Then, you can find if input current ringing is affected by R\text{damp} current.)

Check the R\text{damp} temperature after finding the min. R\text{damp}.
If the temperature is too high and efficiency is too low, active damper is necessary and go to active damper design.

Check R\text{damp} voltage at 90° dimming angle firing. That is SW\text{damp} max voltage.
Tip! SW\text{damp} with low threshold voltage can reduce power loss.
  (Because R\text{damp} voltage is regulated as threshold voltage.)

D\text{delay} max. voltage is same as SW\text{damp} max. voltage.
C\text{delay} is generally around 100nF.
R\text{delay} is tens to hundreds kohm. Large R\text{delay} lengthens delay time between dimmer fire and SW\text{damp} turn-on.

Find the min. R\text{delay} to satisfy below.
- At 90° dimming angle, SW\text{damp} should be turned on after input current is dampened by R\text{damp}.
  (Check if input current ringing is finished before SW\text{damp} turns on.)
The min. R\text{delay} is proper value for high efficiency.
Related Resources

Locate the Design Tool at:

http://www.fairchildsemi.com/design_tools/led-driver-design-tool/

Consult the product datasheet at:

FL7730 — Dimmable Single-Stage PFC PSR Offline LED Driver

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