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Design Guideline of Single-Stage Flyback AC-DC Converter Using FAN7530 for LED Lighting

Summary

This application note describes the single-stage power factor correction (PFC) and presents the design guidelines of a 75W universal-input, single-stage PFC for LED lighting applications. Flyback converter topology controlled by the critical conduction mode control IC, FAN7530 is applied and several functions; such as CV/CC mode feedback circuits, cycle-by-cycle current limit, soft-starting function, and so on, are considered for LED lighting applications.

Introduction

Despite large output voltage ripple, single-stage AC-DC conversion is a more attractive solution than two-stage conversion from the standpoint of the cost and power density. Especially in applications like battery chargers, Plasma Display Panel (PDP)-sustaining power supplies, and LED lighting; low frequency, 100Hz or 120Hz, large output voltage ripple is inconsequential.

Single-stage AC-DC converter directly converts AC input voltage to the DC output voltage without a pre-regulator, as shown in Figure 1.

This application note presents a 75W single-stage AC-DC converter for LED lighting. As a power-conversion topology, flyback converter is normally chosen because it doesn’t need an inductive output filter; the main transformer works as an inductive filter itself.

Figure 2 shows the circuit diagram of a flyback AC-DC converter. FAN7530 is used as a controller and both CV (constant voltage) and CC (constant current) mode feedback circuits are applied to prevent overload and over-voltage conditions. In LED lighting, the output is always full-load condition and the forward voltage drop of LED decreases if the junction temperature of LED increases. Therefore the output should be controlled by CC mode in the normal state while CV mode only works as over voltage protection.

Figure 3 shows the block diagram of FAN7530. Its major features are:

- Fixed On Time CRM PFC Controller
- Zero Current Detector (ZCS) & Valley Switching
- MOSFET Over-Current Protection
- Low Startup (40μA) and Operating Current (1.5mA)
- Totem Pole Output with High State Clamp
- +500/-800mA Peak Gate Drive Current

FAN7530 is a voltage-mode CRM PFC controller; the turn-on time of switch is fixed while the turn-off time is varied during the steady state. Therefore, the switching frequency varies in accordance with the input voltage variation shown in Figure 4.
Vin / Iin

Average input current

Vin

Figure 4. Switching Frequency Variation

Figure 5. Theoretical Waveforms

Figure 5 illustrates the theoretical waveforms of the primary-side switch current, the secondary-side diode current, and gating signal. MOSFET Q turns on and Fast Recovery Diode (FRD) Do turns off under zero-current condition, while Q turns off and Do turns on under the hard-switching condition.

Design Example

A design guideline of 75W single-stage flyback AC-DC converter using FAN7530 is presented. The applied system parameters are shown in Table 1.

Table 1. System Parameters

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<th>Parameter</th>
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1. Flyback Transformer Design

In flyback converter, the transformer is easily saturated because the transformer is only utilized in the first quadrant of B-H loop. Moreover, if it works under the critical conduction mode, the peak current is much higher than that of the continuous conduction mode. Therefore, air-gap should be inserted to prevent saturation of the transformer.

A proper turn ratio, N1/N2, should also be considered in a flyback single-stage AC-DC converter because the maximum voltage rating of the MOSFET and Fast Recovery Diode (FRD) strongly relates to the turn ratio of transformer. There is a trade-off relationship between the drain-to-source voltage rating, V_{ds}, of MOSFET and the reverse voltage rating, V_R, of the FRD in accordance with the turn ratio of the transformer. A larger turn ratio (N1/N2) requires a higher V_R of FRD while V_{ds} of MOSFET is decreased. In contrast, a lower turn ratio causes a higher voltage stress on the MOSFET, while V_R of the FRD is decreased. Figure 6 shows the trade-off relationship between V_{ds} of the MOSFET and V_R of the FRD.

From $P_o = \eta V_o I_o$, the maximum line current $I_{in(max)} = P_o / \eta V_{in(max)}$. If switching frequency $f_s$ is much higher than the AC line frequency, $f_{ac}$, the input current can be assumed to be constant during one switching period.

To define the magnetizing inductance of transformer, the largest period must be defined. The largest switching period occurs at the peak of input current, $I_{in(max)}$, when the minimum input voltage is applied. It can be defined as:

\[ I_{(max)_(in)_pk} = \frac{1}{T_s} \int_0^{T_s} I_{Q_(max)_pk} dt \frac{D}{2} \]

where $D = D_{Q_(max)_pk} \times I_{in(max)_pk} = \sqrt{2} I_{in(max)_pk}$, and $V_{in(min)_pk} = \sqrt{2} V_{in(min)}$, respectively.

The transformer primary-side voltage, $V_T$, is defined as:

\[ V_T = L_m \frac{\Delta I}{\Delta T} = L_m \frac{I_{Q_(max)_pk} f_s \cdot \Delta I}{D_{Q_(max)_pk}} \]

Therefore, the magnetizing inductance is calculated by:

\[ L_m = \frac{D_{Q_(max)_pk} \cdot V_{in(min)_pk}}{2 \times I_{in(max)_pk} f_s} = 0.6 \times \frac{V_{in(min)_pk}}{2 \times 1.04 \times 50 \times 10^{-3}} = 294.8 \mu H \]

From Equation (4) and Table 1, the calculated magnetizing inductance is 294μH.

There are several methods defining the turn number for the desirable inductance, but using the AL-value is the most...
common and the easiest. The turn number can be obtained with AL-value as:

\[ N = \sqrt{\frac{L}{AL \text{- value}}} \]  
\[ (5) \]

However, if air-gap is inserted into the magnetic core, a designer should find the AL-value. To obtain AL-value, wind several turns into a bobbin and measure the inductance, then calculate AL-value with the equation:

\[ AL \text{- value} = \frac{L}{N^2} \]  
\[ (6) \]

Once the AL-value is obtained, calculate the turn number using Equation (6).

Applying coil dummy EER3435 with 0.33mm of air gap for the transformer and 14.9\(\mu\)H is measured when 10 turns are wound into the core and 0.149\(\times10^{-6}\) of AL-value is obtained. Therefore, the calculated primary-side turn number is 44.5 from Equation (6) and finally determines 44 as the primary-side turn number. (The actual inductance is measured as 330\(\mu\)H.)

The secondary-side turn number is obtained as 17 turns by following equation:

\[ N_2 = \frac{\pi N_1 V_{in(max)} (1 - D_{max})}{2\sqrt{2} D_{max} V_{in(min)}} = \frac{\pi \times 44 \times 45 (1 - 0.6)}{2\sqrt{2} \times 0.6 \times 85} = 17 \]
\[ (7) \]

### 2. MOSFET and FRD

The voltage stress of MOSFET is calculated as:

\[ V_{ds(max)} = V_{in(max)_{pk}} + V_{sn} \]  
\[ (8) \]

where \(V_{sn}\) is the maximum capacitor voltage of the snubber circuit; \(V_f\) is the flyback voltage; and \(V_{Lk}\) is the ringing voltage at the leakage inductance of the transformer. \(V_f\) is derived by \(N_1 V_{in}/N_2\) and \(V_{Lk}\) is normally estimated as 1.5 times the flyback voltage, \(V_f\). Therefore, the maximum voltage of MOSFET is obtained as:

\[ V_{ds(max)} = \sqrt{2} V_{in(max)} + 2.5 n V_c = \sqrt{2} \times 265 \times 2.5 + 44 \times 17 = 665.94V \]
\[ (9) \]

The maximum rms current and the peak current are:

\[ I_{in(max)} = \frac{P_o}{\eta V_{in(min)}} = \frac{75}{0.85 \times 85} = 1.04A \]
\[ (10) \]

and

\[ I_{(max)_{pk}} = \frac{2\sqrt{2} P_o}{\eta D_{in(max)_{pk}} V_{in(min)}} = \frac{2\sqrt{2} \times 75}{0.85 \times 0.6 \times 85} = 4.89A \]
\[ (11) \]

respectively.

Therefore, an N-Channel enhancement-mode MOSFET, FQFP8N80C (800V, 8A, \(R_{DS,ON} = 1.55\Omega\)), is chosen in consideration of the margins.

The maximum reverse voltage and the forward peak current of the FRD are:

\[ V_{f(max)} = V_{f_{in(max)_{pk}}} + \frac{N_2}{N_1} V_{f_{in(max)_{pk}}} \]
\[ = 50 + \frac{17}{44} \times \sqrt{2} \times 265 = 195V \]
\[ (12) \]

\[ I_{f_{pk}} = \frac{2}{(1 - D_{in(max)_{pk}})} I_f = \frac{2}{(1 - 0.6)} \times \frac{75}{45} = 8.33 A \]
\[ (13) \]

respectively. Therefore, the Ultra-Fast Rectifier Diode (UFRD), F06UP20S (200V, 6A, \(V_f = 1.15V\)), is finally chosen in consideration of the margins.

### 3. Snubber Circuit Design

In flyback converter, the resonant between \(L_{leak}\) and \(C_{oss}\) causes an excessively high voltage surge that causes damage to the MOSFET during turn-off. This voltage surge must be suppressed and a snubber circuit is therefore necessary to prevent MOSFET failures.

The clamping voltage by snubber is:

\[ V_{cl} = V_f + L_{leak} \frac{\Delta i}{\Delta t} \]
\[ (14) \]

Therefore:

\[ i_f = \frac{L_{leak} \cdot I_{Dsn_{pk}}}{V_{in} - V_f} \]
\[ (15) \]

The maximum power dissipation of the snubber circuit is determined by:

\[ P_{sn} = \frac{1}{T_s} \int_0^{T_s} V_{sn} I_{Dsn_{pk}} t dt = \frac{1}{2} L_{leak} I_{Dsn_{pk}}^2 \frac{V_{in} - V_f}{V_f} f_s \]
\[ (16) \]
The maximum power dissipation is:

\[
P_{\text{max}} = \frac{1}{2} L_{\text{ind}} I_{\text{Dson, pk}}^2 \frac{V_m}{V_s} - \frac{f_{\text{sw}}}{V_{\text{in, max}}} V_m^2 \frac{R_m}{R_{\text{sn}}} \tag{17}
\]

where \( V_m = V_f + V_{Lr} \).

Therefore, the resistance, \( R_{\text{sn}} \), is determined by:

\[
R_{\text{sn}} = \frac{V_m^2}{2 L_{\text{ind}} I_{\text{Dson, pk}}^2 \frac{V_m}{V_s} - \frac{f_{\text{sw}}}{V_{\text{in, max}}} V_m^2 \frac{R_m}{R_{\text{sn}}}} \tag{18}
\]

The maximum ripple voltage of the snubber circuit is obtained by:

\[
\Delta V_{\text{sn}} = \frac{V_m}{C_{\text{sn}} R_{\text{sn}} f_{\text{sw}} V_{\text{in, max}}} \tag{19}
\]

The larger snubber capacitor results, the lower voltage ripple, but the power dissipation increases. Consequently, selecting the proper value is important. In general, it is reasonable to determine that the surge voltage of snubber circuit, \( V_{\text{sn}} \), is two to three (2~3) times the flyback voltage, \( V_f \), and the ripple voltage, \( \Delta V_{\text{sn}} \), is 50V. In this application note, the snubber voltage is 2.5 times of the flyback voltage. Thus, the snubber resistor and capacitor are determined by the following equations:

\[
I_{\text{Dson, pk}} = \frac{2 \sqrt{2} P_{\text{out}}}{\eta D_{\text{min}} V_{\text{in}}} = \frac{2 \sqrt{2} \times 75}{0.85 \times 0.33 \times 265} = 2.854 \text{A}
\]

\[
V_m = V_f + V_{Lk} = 2.5V_f + 2.5 \times 44 \times 45 = 291.17V \tag{21}
\]

\[
t_s = \frac{L_{\text{ind}} I_{\text{Dson, pk}}}{V_m - V_f} = \frac{15 \times 10^{-6} \times 2.85}{291.17 - 44 \times 45} = 245.03n\text{sec} \tag{22}
\]

\[
f_{\text{sw}} = \frac{V_m}{I_{\text{Dson, pk}}} = \frac{E_{\text{ind, measured}} I_{\text{Dson, pk}}}{V_m} = \frac{0.33 \times 291.17}{330 \times 10^{-6} \times 2.85 \times 291.17} = 102.03kHz \tag{23}
\]

\[
R_{\text{sn}} = \frac{1}{2} \times 15 \mu \times 2.85^2 \times \frac{291.17}{291.17 - (44/17)45} = 8.164\Omega \tag{24}
\]

\[
C_{\text{sn}} = \frac{\Delta V_{\text{sn}} R_{\text{sn}} f_{\text{sw}} V_{\text{in, max}}}{291.17} = \frac{291.17}{50 \times 8.16k \times 102.03k} = 6.99nF \tag{25}
\]

where the minimum duty ratio is obtained as:

\[
D_{\text{min}} = \frac{N_i}{N_f} \frac{V_i}{V_{\text{in, max}}} + V_o = \frac{45}{44 \times \left( \frac{2 \sqrt{2}}{\pi} \times 265 \right) + 45} = 0.33 \tag{26}
\]

Even though the calculated \( R_{\text{sn}} \) is 8.16k\( \Omega \), the actual resistance value should be increased because large power dissipation in the snubber circuit is expected due to small resistance. In practice, it is reasonable to choose the resistance about two times of the calculated value.

4. Sensing Resistor

The CS pin of FAN7530 limits the peak current and protects the MOSFET during transient state or over load condition. Normally, it is reasonable to limit to 1.5 times the switching peak current. The limiting level of switching peak current and the sensing resistor are obtained as:

\[
I_{\text{Q, Limit}} = 1.5 I_{(\text{max}) \text{, pk}} = 1.5 \times \frac{2}{D_{\text{max}}} \left( \sqrt{2} \frac{P_{\text{out}}}{\eta f_{\text{sw}}(\text{min})} \right) \tag{27}
\]

\[
= 1.5 \times \frac{2}{0.6} \left( \sqrt{2} \frac{75}{0.85 \times 85} \right) = 7.44 \text{A} \tag{28}
\]

R_s \leq \frac{0.8}{7.4} = 0.11\Omega

5. Soft-starting Circuit

Since the FAN7530 is designed for a non-isolated boost PFC circuit, some circuits are added externally. The internal disable amplifier can be used as soft-start function when FAN7530 is applied to non-isolated PFC circuit. However, the disable amplifier cannot participate in the operation if it is applied to isolated single stage PFC circuit because the initial voltage at Pin 1 is zero and FAN7530 cannot start. To exclude the disable amplifier from operation, over 0.5V of voltage must be applied through a blocking diode, as shown in Figure 9(a).

The initial \( V_{FB} \) is approximately defined as:

\[
V_{FB\_\text{initial}} = \frac{R_{FB}}{R_{FB} + R_s} V_{CC} \tag{29}
\]

To prevent MOSFET failure due to the initial excessive switching current, an external soft-start function is necessary. The circuit shown in Figure 9(b) makes the output voltage of E/A increase slowly and, consequently,
the converter can be smoothly started in accordance with the gradual increase of the on time.

6. Voltage and Current Feedback

Power supplies for LED lighting must be controlled by constant current (CC) mode as well as a constant voltage (CV) mode. Because the forward voltage drop of LED varies with the junction temperature and the current also increases greatly consequently, devices can be damaged.

Figure 10 shows an example of a CC and CV mode feedback circuit. During normal operation, CC mode is dominant and CV mode only acts as OVP for abnormal modes.

Experimental Results

To verify the validity of the design guideline in this application note, a prototype test set-up was built and tested. The design parameter and component values are shown in the appendix.

Figure 11 shows the input voltage and current at 110V AC input and 220V AC input conditions. The power factors at 110V AC and 220V AC condition are measured as 0.997 and 0.955, respectively.

Figure 12 shows the waveforms of the switching voltage and current, which shows the switching current waveforms following the shape of the input voltage well. The switch is turned on at zero current condition.
Figure 13. Drain-Source Voltage and Switching Current at 265VAC Input Condition

Figure 13 shows the waveforms of the drain-source voltage and current of 265V of input line voltage, the maximum input voltage, is applied. The voltage ripple of snubber circuit is measured at 54V and the maximum voltage stress is 688V. Since the maximum voltage is 688V, 800V rating MOSFET is needed for wide input voltage range.

The efficiency characteristics according to the load variation for 110 V\textsubscript{ac} and 220 V\textsubscript{ac} of the input conditions are plotted in Figure 14. In the case of 110V\textsubscript{ac} input, the maximum efficiency is measured as 85.17\% at 45W load condition.

Figure 14. Efficiency Comparison

Figure 15. Output V-I Characteristic

In the case of 220V\textsubscript{ac} input, the maximum efficiency is measured as 85.95\% at full-load condition 75W.

In LED lighting, LED strings are driven by the rating current and the power supply should be operated under the full-load condition. Therefore, the power supply is controlled by constant current during normal condition. Figure 15 shows the V-I characteristics of the prototype experimental set-up. The result verifies that the output is driven well by the constant current control for whole input voltage condition.
Figure 16. Schematic
### Part List

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<th>Component</th>
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<th>Value/Part Number</th>
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Related Datasheets

FAN7527 — Boundary Mode PFC Control IC
FAN7528 — Dual-Output Critical Conduction Mode PFC Controller
FAN7529 — Critical Conduction Mode PFC Controller
FAN7530 — Critical Conduction Mode PFC Controller

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