**AN-9750**

**High-Power Factor Flyback Converter for LED Driver with FL7732 PSR Controller**

**Introduction**

This highly integrated PWM controller, FL7732, provides several features to enhance the performance of low-power flyback converters. The proprietary topology enables simplified circuit design for LED lighting applications. By using single-stage topology with primary-side regulation, a LED lighting board can be implemented with few external components and minimized cost, without requiring an input bulk capacitor and feedback circuitry. To implement high power factor and low THD, constant on-time control utilizes an external capacitor connected at the COMI pins.

Precise constant-current control regulates accurate output current across changes in input voltage and output voltage. The operating frequency is proportionally changed by the output voltage to guarantee DCM operation with higher efficiency and simple design. FL7732 provides protection functions such as open-LED, short-LED and over-temperature protection. The current-limit level is automatically reduced to minimize the output current and protect external components in short-LED condition.

This application note presents practical design consideration for an LED driver employing Fairchild Semiconductor PWM PSR controller FL7732. It includes designing the transformer, selecting the components, and implementing constant current regulation. The step-by-step design procedure helps engineers design a power supply. The design procedure is verified through an experimental prototype converter. Figure 1 shows the typical application circuit of primary-side controlled flyback converter using FL7732 created in the design example.

![Typical Application Circuit](image)

**Figure 1. Typical Application Circuit**
Basic Operation

Generally, Discontinuous Conduction Mode (DCM) operation is preferred for primary-side regulation because it allows better output regulation. The operation principles of DCM flyback converter are as follows:

Mode I

During the MOSFET turn-on time \((t_{ON})\), input voltage \((V_{IN,\text{pk}})\) is applied across the primary-side inductor \((L_m)\). Then, drain current \((I_{DS})\) of the MOSFET increases linearly from zero to the peak value \((I_{pk})\), as shown in Figure 2. During this time, the energy is drawn from the input and stored in the inductor.

Mode II

When the MOSFET \((Q)\) is turned off, the energy stored in the inductor forces the rectifier diode \((D)\) to be turned on. While the diode is conducting, output voltage \((V_{OUT})\), together with diode forward-voltage drop \((V_{FD})\), is applied across the secondary-side inductor and diode current \((I_{D})\) decreases linearly from the peak value \((I_{pk} \cdot N_P/N_S)\) to zero. At the end of inductor current discharge time \((t_{DIS})\), all energy stored in the inductor has been delivered to the output.

Mode III

When the diode current reaches zero, the transformer auxiliary winding voltage begins to oscillate by the resonance between the primary-side inductor \((L_m)\) and the effective capacitor loaded across MOSFET \((Q)\).
Constant Current Regulation

The output current ($I_o$) can be estimated by using the peak drain current ($I_{pk}$) of MOSFET and discharging time ($t_{DIS}$) of inductor current because output current ($I_o$) is same as the average of the diode current ($I_D$) in steady state. The output current estimator identifies the peak value of the drain current with a peak-detection circuit and calculates the output current using the inductor discharging time and switching period ($t_S$). This output information is compared with an internal precise reference to generate error voltage ($V_{COMI}$), which determines the duty cycle of the MOSFET in Constant Current Mode. With Fairchild’s innovative TRUECURRENT® technique, the constant output current can be precisely controlled.

\[
I_o = \frac{1}{2} \cdot \frac{t_{DIS}}{t_s} \cdot \frac{V_{CS}}{N_P} \cdot \frac{1}{N_S} \cdot \frac{1}{R_{SENSE}}
\]

(1)

TRUECURRENT® calculation makes a precise output current prediction.

Output voltage is detected by the auxiliary winding and resistive divider connected to the VS pin, as shown in Figure 7.

Figure 8. Linear Frequency Control

When output voltage decreases, secondary diode conduction time is increased and the linear frequency control lengthens the switching period, which retains DCM operation in the wide output voltage range, as shown in Figure 8. The frequency control also lowers primary rms current with better power efficiency in full-load condition.

Figure 9. Primary and Secondary Current

BCM Control

As mentioned above, DCM should be guaranteed for high power factor in flyback topology. To maintain DCM in the wide range of output voltage, frequency is linearly changed by the output voltage in linear frequency control.

Figure 6. Detection for TRUECURRENT® Calculation

Figure 7. TRUECURRENT® Calculation Principle

Linear Frequency Control

As mentioned above, DCM should be guaranteed for high power factor in flyback topology. To maintain DCM in the wide range of output voltage, frequency is linearly changed by the output voltage in linear frequency control.
Protections
The FL7732 have several self-protection functions, such as over-voltage protection, over-temperature protection, and pulse-by-pulse current limit. All the protections are implemented as Auto-Restart Mode.

Open-LED Protection
FL7732 protects external components, such as diode and capacitor at secondary side, in open-LED condition. During switch-off, the \( V_{DD} \) capacitor is charged up to the auxiliary winding voltage, which is applied as the reflected output voltage. Because the \( V_{DD} \) voltage has output voltage information, the internal voltage comparator at the \( V_{DD} \) pin can trigger output over-voltage protection (OVP), as shown in Figure 9. When at least one LED is open-circuited, output load impedance becomes very high and output capacitor is quickly charged up to \( V_{OVP} \times N_S/N_A \). Then switching is shut down and the \( V_{DD} \) block goes into “Hiccup Mode” until the open-LED condition is removed, as shown in Figure 10.

Short-LED Protection (OCP)
In case of short-LED condition, the switching MOSFET and secondary diode are usually stressed by the high powering current. However, FL7732 changes the OCP level in the short LED condition. When \( V_S \) voltage is lower than 0.4 V, OCP level changes to 0.2 V from 0.7 V, as shown in Figure 12 so that powering is limited and external components current stress is relieved.

Under Voltage Lockout (UVLO)
The turn-on and turn-off thresholds are fixed internally at 16 V and 7.5 V, respectively. During startup, the \( V_{DD} \) capacitor must be charged to 16 V. The \( V_{DD} \) capacitor continues to supply \( V_{DD} \) until power can be delivered from the auxiliary winding of the main transformer. \( V_{DD} \) is not allowed to drop below 7.5 V during this startup process. This UVLO hysteresis window ensures that \( V_{DD} \) capacitor properly supplies \( V_{DD} \) during startup.

Figure 11. Waveforms at Open-LED Condition
Figure 12. Internal OCP Block
Figure 13 shows operational waveforms at short-LED condition. Output voltage is quickly lowered to 0 V right after the LED-short event. Then, the reflected auxiliary voltage is also 0 V making \( V_S \) voltage less than 0.4 V. 0.2 V OCP level limits primary-side current and \( V_{DD} \) hiccups up and down in between UVLO hysteresis.
Over-Voltage Protection (OVP)
The OVP prevents damage in over-voltage conditions. If the $V_{DD}$ voltage exceeds 23 V at open-loop feedback condition, the OVP is triggered and the PWM switching is disabled. At open-LED condition, $V_{DD}$ reaches $V_{DD\_OVP}$. Then, auto-restart sequence causes a delay, limiting output voltage.

Over-Temperature Protection (OTP)
The built-in temperature-sensing circuit shuts down PWM output if the junction temperature exceeds 150°C. There is hysteresis of 10°C.

At short-LED condition, $V_S$ is low due to low output voltage. Then, OCP level is changed to 0.2 V to reduce output current.
Design Procedure

In this section, a design procedure of a single-stage flyback using FL7732 is presented using the schematic of Figure 1 as a reference. An offline LED driver with 16.8 W (24 V/0.7 A) output has been selected as a design example. The design specifications are as follows:

- Input voltage range: 90 ~ 264 VAC and 50 ~ 60 Hz
- Nominal output voltage and current: 24 V/0.7 A
- Minimum efficiency: 87%
- Maximum switching frequency: 65 kHz

Step 1. Inductor Selection (Lm)

FL7732 operates with constant turn-on and turn-off time, as shown Figure 14. When MOSFET turn-on time (tON) and switching period (tS) are constant, IIN is proportional to VIN and can implement high power factor.

The single-stage flyback using FL7732 is assumed to operate in DCM due to constant tON and tS. Input voltage is applied across the magnetizing inductance (Lm) during tON, charging the magnetic energy in Lm. Therefore, the maximum peak switch current (ISW.pk) of MOSFET occurs at peak point of line voltage, as shown Figure 14. The peak input current (IIN.pk) is also shown at the peak input voltage of one line cycle. Once the maximum tON is decided, ISW.pk of MOSFET is obtained at the minimum line input voltage and full-load condition as:

\[ I_{SW.pk} = \frac{t_{ON} \cdot V_{IN.min.pk}}{L_m} \]  

where V_{IN.min.pk} and tON are the peak input voltage and the maximum turn-on time at the minimum line input voltage, respectively.

Using equation (2), the peak input current is obtained by:

\[ I_{IN.pk} = \frac{1}{2} \cdot (t_{ON}) \cdot \left( \frac{V_{IN.min.pk} \cdot t_{ON}}{L_m} \right) \cdot f_s \]  

then I_{IN.pk} and V_{IN.min.pk} can be expressed as:

\[ I_{IN.pk} = \sqrt{2} \cdot I_{IN.rms} \]  
\[ V_{IN.min.pk} = \sqrt{2} \cdot V_{IN.rms} \]  

where the I_{IN.rms} and V_{IN.rms} are rms line input current and voltage, respectively.

\[ t_{ON} \] is required to calculate reasonable Lm value. With Equation (2) ~ (5), the turn-on time, tON is obtained as:

\[ t_{ON}^2 = \frac{2L_m \cdot I_{IN.rms}}{V_{IN.rms} \cdot f_s} \]

The input power is given as:

\[ P_{IN} = I_{IN.rms} \cdot \frac{P_O}{\eta} \]

With Equation (6) and (7), the Lm value is obtained as:

\[ L_m = \frac{\eta \cdot (V_{IN.rms})^2 \cdot f_s \cdot t_{ON}^2}{2P_O} \]

(Design Example) Since the minimum input voltage is 90VAC, the maximum tON occurs at full-load condition. Assuming the maximum tON is 7.4 µs at 65 kHz of the maximum frequency, the magnetizing inductance is obtained as:

\[ L_m = \frac{0.87 \times 90^2 \times 65 \times 10^3 \times (7.4 \times 10^{-6})^2}{2 \times 16.8} = 743 \mu H \]

The maximum peak current of MOSFET at nominal output power is calculated as:

\[ I_{SW.pk} = \frac{7.4 \times 10^{-6} \times \sqrt{2} \times 90}{743 \times 10^{-6}} = 1.26 A \]

Step 2. Sensing Resistor and nPS Selection

Since FL7732 adopts TRUECURRENT® Calculation method to regulate constant output current (Io), as defined in equation (1). The output current is proportional to turn ratio nPS between the primary and secondary windings of the transformer and inversely proportional to sensing resistor (Rs). The FL7732 also implements cycle-by-cycle current limitation by detecting VC5 to protect system from output short or overload. Therefore, VC5 level to handle rated system power without the current limitation should be considered. It is typical to set the cycle-by-cycle limit level.
(typical: 0.67 V) at 20~30% higher than CS peak voltage (V_{CS, pk}) at full-load condition. MOSFET peak current (I_{SW, pk}) is converted into V_{CS, pk} as:

\[ V_{CS, pk} = I_{SW, pk} \cdot R_S \]  

(9)

According to Equation (1), the transformer turn ratio is determined by the sensing resistor and nominal output current as:

\[ n_p = 10.5 \times I_O \times R_S \]  

where 10.5 is a constant.

\[ \frac{1}{2} \cdot \frac{t_{DS}}{t_s} \cdot V_{CS} = \frac{1}{10.5} \]  

(11)

(Design Example) Once V_{CS, pk} is set as 0.5 V, the sensing resistor value is obtained as:

\[ R_S = \frac{V_{CS, pk}}{I_{SW, pk}} = \frac{0.5}{1.26} = 0.396 \]  

\[ n_p = 10.5 \times 0.7 \times 0.396 = 2.91 \]

**Step 3. n_{AS} Selection**

When V_{DD} voltage is 23 V, FL7732 stops switching operation due to over-voltage protection (OVP). So n_{AS} can be determined as follows:

\[ n_{AS} = \frac{V_{DD, OVP}}{V_{O, OVP}} = \frac{23}{V_{O, OVP}} \]  

where \((n_{AS} = N_v / N_s)\) is the turns ratio of secondary to auxiliary of transformer. Therefore, V_{O, OVP} can be set by changing the n_{AS} value.

(Design Example) Once output over-voltage level is set as 30 V, n_{AS} is obtained as:

\[ n_{AS} = \frac{23}{30} = 0.77 \]

**Step 4. Resistor Selection (R_{VS1} and R_{VS2})**

The first consideration for R_{VS1} and R_{VS2} selection is that V_s is 2.35 V at the end of diode current conduction time to operate at maximum switching frequency at rated power. The second consideration is V_s blanking, as explained below. The output voltage is detected by auxiliary winding and a resistive divider connected to the VS pin, as shown in Figure 7. However, in a single-stage flyback without DC link capacitor, auxiliary winding voltage cannot be clamped to reflected output voltage due to the small L_m current, which induces V_s voltage sensing error. Then, frequency decreases rapidly at the zero-crossing point of line voltage, which can cause flicker. To maintain constant frequency over the whole sinusoidal line voltage, FL7732 has V_s blanking to disable sampling of V_s voltage at less than a particular line voltage by sensing the auxiliary winding.

Considering the maximum switching frequency at rated power and V_s blanking level, R_{VS1} and R_{VS2} are obtained as:

\[ R_{VS} = \frac{(V_O + V_F)n_{AS} - V_{VS, \text{max}}}{V_{VS, \text{max}}} \]  

(13)

\[ R_{VS1} = R_{VS} \cdot R_{VS2} \]  

(14)

where V_{VS, max} is the V_s value to set the maximum switching frequency for constant output current in rated power and V_F is secondary diode forward voltage.

\[ R_{VS2} = \frac{1}{I_{VS, \text{blank}} \times (V_{VS, \text{blank}} + V_{IN, \text{blank}} \cdot n_{AP})} \]  

(15)

where V_{IN, blank} and n_{AP} are the blanking level of input voltage and the turn ratio of auxiliary to primary, respectively. The n_{AP} can be calculated as the ratio of n_{AS} to n_{PS}. I_{VS, blank} and V_{VS, blank} are decided internally at 1 µA and 0.545 V.

(Design Example) The voltage divider network is determined as:

\[ R_{VS} = \frac{(24 + 0.7) \times 0.77 - 2.35}{2.35} = 7.06 \]

Once V_{IN, blank} level is set to 50 V, R_{VS2} is obtained as.

\[ R_{VS2} = \frac{1}{100 \times 10^{-6} \times (0.545 + \frac{0.77}{2.91})} \]

\[ = 24.86 \text{k} \Omega \]

Then R_{VS1} is determined to be 175.5 kΩ.

It is recommended to place a bypass capacitor of 10 ~ 30 pF closely between the VS pin and the GND pin to bypass the switching noise and keep the accuracy of the V_s sensing for CC regulation. The value of the capacitor affects constant-current regulation. If a high value of V_s capacitor is selected, the discharge time t_{DIS} becomes longer and the output current is lower, compared to small V_s capacitor.
Step 5. Design the Transformer

The number of primary turns is determined by Faraday’s law. \( N_{p,\min} \) is fixed by the peak value of the minimum line input voltage across the primary winding and the maximum on time. The minimum number of turns for the transformer primary side to avoid the core saturation is given by:

\[
N_{p,\min} = \frac{V_{IN,\min, pk} \cdot I_{ON}}{B_{sat} \cdot A_e}
\]

(16)

where \( A_e \) is the cross-sectional area of the core in \( m^2 \) and \( B_{sat} \) is the saturation flux density in Tesla.

Since the saturation flux density decreases as the temperature rises, the high-temperature characteristics should be considered when it is used in an enclosed case.

**Design Example** An RM8 core is selected for the transformer and the minimum number of turns for the transformer primary side to avoid the core saturation is given by:

\[
N_{p,\min} = \sqrt{2} \cdot 90 \times 7.4 \times 10^{-6} = 54.5 T
\]

Considering the tolerance of the transformer and high ambient temperature, \( N_p \) should be selected with a margin about 5% ~ 10% to avoid core saturation:

\[
N_p = 54.5 \times 1.1 = 59.95 T
\]

Once the turn number of the primary side \( (N_p) \) is determined as 60 T, the turn number of the secondary side \( (N_S) \) is obtained by:

\[
N_S = 60 \div 2.91 = 20.5 T
\]

Once the turn number of the secondary side \( (N_S) \) is determined as 20 T, the auxiliary winding turns \( (N_A) \) is obtained by:

\[
N_A = 20 \times 0.77 = 15.4 T
\]

\( N_A \) is determined to be 15 T.

**Step 6. Calculate the Voltage and Current of the Switching Devices**

**Primary-Side MOSFET:** The voltage stress of the MOSFET was discussed when determining the transformer turns ratio. Assuming the drain voltage overshoot is the same as the reflected output voltage, the maximum drain voltage is given as:

\[
V_D = V_o + \frac{N_S}{N_p} V_{in,max, pk}
\]

(19)

\[
I_{D,\text{rms}} \approx I_{SW,\text{rms}} \times \sqrt{2 \cdot V_{RO} \cdot \frac{N_p}{N_S}}
\]

(20)

**Secondary-Side Diode:** The maximum reverse voltage and rms current of the rectifier diode are obtained as:

\[
V_D = 24 + \frac{20}{60} \times 374 = 148.7 V
\]

\[
I_{D,\text{rms}} \approx 0.357 \times \sqrt{\frac{127}{2 \times 74.1} \frac{60}{20}} = 0.991 A
\]

**Design Example** The diode voltage and current are obtained as:

\[
V_D = 24 + \frac{20}{60} \times 374 = 148.7 V
\]

\[
I_{D,\text{rms}} \approx 0.357 \times \sqrt{\frac{127}{2 \times 74.1} \frac{60}{20}} = 0.991 A
\]
Step 7. Design RCD Snubber in Primary Side

When the power MOSFET is turned off, there is a high-voltage spike on the drain due to the transformer leakage inductance. This excessive voltage on the MOSFET may lead to an avalanche breakdown and eventually failure of the device. Therefore, it is necessary to use an additional network to clamp the voltage. The RCD snubber circuit and its waveform are shown in Figure 16 and Figure 17, respectively. The RCD snubber network absorbs the current in the leakage inductance by turning on the snubber diode ($D_{SN}$) once the MOSFET drain voltage exceeds the cathode voltage of snubber diode. In the analysis of snubber network, it is assumed that the snubber capacitor is large enough that its voltage does not change significantly during one switching cycle. The snubber capacitor should be ceramic or a material that offers low ESR. Electrolytic or tantalum capacitors are unacceptable for these reasons.

Snubber capacitor voltage at full-load condition is given as:

$$V_{SN} = V_{RO} + V_{OS} \tag{21}$$

The power dissipated in the snubber network is obtained as:

$$P_{SN} = \frac{1}{2} \frac{V_{SN}}{R_{SN}} \cdot I_{PK}^2 \cdot \frac{V_{SN}}{V_{SN} - V_{RO}} \cdot f_s \tag{22}$$

where $L_{lk}$ is leakage inductance, $V_{SN}$ is the snubber capacitor voltage at full load, and $R_{SN}$ is the snubber resistor.

The leakage inductance is measured at the switching frequency on the primary winding with all other windings shorted. Then, the snubber resistor with proper rated wattage should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained as:

$$\Delta V_{SN} = \frac{V_{SN}}{C_{SN} \cdot R_{SN} \cdot f_s} \tag{23}$$

In general, 5 ~ 20% ripple of the selected capacitor voltage is reasonable. In this snubber design, neither the lossy discharge of the inductor nor stray capacitance is considered.

(Design Example) Since the voltage overshoot of drain voltage has been determined to be the same as the reflected output voltage, the snubber voltage is:

$$V_{SN} = V_{RO} + V_{OS} = 150V$$

The leakage inductance is measured as 10 $\mu$H. Then the loss in snubber networking is given as:

$$P_{SN} = \frac{1}{2} \times 10 \times 10^{-6} \times 1.26^2 \times \frac{150}{150 - 75} \times 65 \times 10^3$$

$$= 1.03W$$

$$R_{SN} = \frac{150^2}{1.03} = 21.84k\Omega$$

To allow 7% ripple on the snubber voltage (150 V):

$$C_{SN} = \frac{150}{0.07 \times 150 \times 21.84 \times 10^3 \times 65 \times 10^3} = 10.06nF$$
Lab Notes

1. Before modifying or soldering/desoldering the power supply, discharge the primary capacitors through the external bleeding resistor. Otherwise, the PWM IC may be destroyed by external high-voltage during the process. This device is sensitive to electrostatic discharge (ESD). To improve the yield, the production line should be ESD protected as required by ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1 standards.

2. In case of LED-short condition, $V_{DD}$ voltage charged at $V_{DD}$ capacitor should touch $V_{DD}$ off level rapidly to stop switching. Therefore, $V_{DD}$ capacitor value is recommended under 22 µF.
Schematic of Design example

Figure 18 shows the schematic of the 16.8 W LED driver design example. RM8 core is used for the transformer. Figure 19 shows the transformer information.

![Figure 18. Schematic of the FL7732 17 W Design Example](image)

![Figure 19. Transformer Winding Structure](image)

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<th>Wire</th>
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Related Datasheets

FL7732 — Single-Stage PFC Primary-Side-Regulation Offline LED Driver

Reference Designs— http://www.fairchildsemi.com/referencedesign/

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LIFE SUPPORT POLICY
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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.