FAN5234
Dual Mobile-Friendly PWM / PFM Controller

Features
- Wide Input Voltage Range for Mobile Systems: 2V to 24V
- Excellent Dynamic Response with Voltage Feedback and Average-Current-Mode Control
- Lossless Current Sensing on Low-Side MOSFET or Precision Over-Current via Sense Resistor
- \( V_{CC} \) Under-Voltage Lockout
- Power-Good Signal
- Light-Load Hysteretic Mode Maximizes Efficiency
- 300KHz or 600KHz Operation
- TSSOP16 Package

Applications
- Mobile PC Regulator
- Handheld PC Power

Related Resources
- Application Note — AN-6002 Component Calculations and Simulation Tools for FAN5234 or FAN5236
- Application Note — AN-1029 Maximum Power Enhancement Techniques for SO-8 Power MOSFET

Description
The FAN5234 PWM controller provides high efficiency and regulation with an adjustable output from 0.9V to 5.5V required to power I/O, chip-sets, memory banks, or peripherals in high-performance notebook computers, PDAs, and internet appliances. Synchronous rectification and hysteretic operation at light loads contribute to a high efficiency over a wide range of loads. The Hysteretic Mode of operation can be disabled if PWM Mode is desired for all load levels. Efficiency is further enhanced by using the MOSFET's \( R_{DS(on)} \) as a current-sense component.

Feed-forward ramp modulation, average current mode control, and internal feedback compensation provide fast response to load transients. The FAN5234 monitors these outputs and generates a PGGOOD (power-good) signal when the soft-start is completed and the output is within ±10% of its set point. A built-in over-voltage protection prevents the output voltage from going above 120% of the set point. Normal operation is automatically restored when the over-voltage conditions cease. Under-voltage protection latches the chip off when the output drops below 75% of its set value after the soft-start sequence is completed. An adjustable over-current function monitors the output current by sensing the voltage drop across the lower MOSFET.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Operating Temperature Range</th>
<th>Package</th>
<th>Packing Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAN5234MTCX</td>
<td>-10 to +85°C</td>
<td>16-Lead, Thin-Shrink Small-Outline Package (TSSOP)</td>
<td>Tape and Reel</td>
</tr>
</tbody>
</table>
Typical Application

VIN (BATTERY) = 2 to 24V

Figure 1. 1.18V Output Regulator

Block Diagram

Figure 2. Block Diagram
Pin Configuration

Figure 3. Pin Configuration

Pin Definitions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VIN</td>
<td><strong>Input Voltage.</strong> Connect to main input power source (battery), also used to program operating frequency for low input voltage operation (see Table 1).</td>
</tr>
<tr>
<td>2</td>
<td>PGOOD</td>
<td><strong>Power-Good Flag.</strong> An open-drain output that pulls LOW when $V_{SEN}$ is outside of a ±10% range of the 0.9V reference.</td>
</tr>
<tr>
<td>3</td>
<td>EN</td>
<td><strong>Enable.</strong> Enables operation when pulled to logic HIGH. Toggling EN resets the regulator after a latched fault condition. This is a CMOS input whose state is indeterminate if left open.</td>
</tr>
<tr>
<td>4</td>
<td>ILIM</td>
<td><strong>Current Limit.</strong> A resistor from this pin to GND sets the current limit.</td>
</tr>
<tr>
<td>5</td>
<td>VOUT</td>
<td><strong>Output Voltage.</strong> Connect to output voltage. Used for regulation to ensure a smooth transition during mode changes. When $V_{OUT}$ is expected to exceed $V_{CC}$, tie this pin to $V_{CC}$.</td>
</tr>
<tr>
<td>6</td>
<td>VSEN</td>
<td><strong>Output Voltage Sense.</strong> The feedback from the output. Used for regulation as well as power-good, under-voltage, and over-voltage protection monitoring.</td>
</tr>
<tr>
<td>7</td>
<td>SS</td>
<td><strong>Soft-Start.</strong> A capacitor from this pin to GND programs the slew rate of the converter during initialization, when this pin is charged with a 5µA current source.</td>
</tr>
<tr>
<td>8</td>
<td>AGND</td>
<td><strong>Analog Ground.</strong> This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.</td>
</tr>
<tr>
<td>9</td>
<td>PGND</td>
<td><strong>Power Ground.</strong> The return for the low-side MOSFET driver output. Connect to the gate of the low-side MOSFET.</td>
</tr>
<tr>
<td>10</td>
<td>LDRV</td>
<td><strong>Low-Side Drive.</strong> The low-side (lower) MOSFET driver output. Connect to the gate of the low-side MOSFET.</td>
</tr>
<tr>
<td>11</td>
<td>VCC</td>
<td><strong>Supply Voltage.</strong> This pin powers the chip as well as the LDRV buffers. The IC starts to operate when voltage on this pin exceeds 4.6V (UVLO rising) and shuts down when it drops below 4.3V (UVLO falling).</td>
</tr>
<tr>
<td>12</td>
<td>ISNS</td>
<td><strong>Current-Sense Input.</strong> Monitors the voltage drop across the lower MOSFET or external sense resistor for current feedback.</td>
</tr>
<tr>
<td>13</td>
<td>SW</td>
<td><strong>Switching Node.</strong> Return for the high-side MOSFET driver and a current-sense input. Connect to source of high-side MOSFET and low-side MOSFET drain.</td>
</tr>
<tr>
<td>14</td>
<td>HDRV</td>
<td><strong>High-Side Drive.</strong> High-side (upper) MOSFET driver output. Connect to the gate of the high-side MOSFET.</td>
</tr>
<tr>
<td>15</td>
<td>BOOT</td>
<td><strong>BOOT.</strong> Positive supply for the upper MOSFET driver. Connect as shown in Figure 2.</td>
</tr>
<tr>
<td>16</td>
<td>FPWM</td>
<td><strong>Forced PWM Mode.</strong> When logic HIGH, inhibits the regulation from entering Hysteretic Mode.</td>
</tr>
</tbody>
</table>
## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>$V_{CC}$ Supply Voltage</td>
<td>6.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>$V_{IN}$ Supply Voltage</td>
<td>27</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>BOOT, SW, ISNS, HDRV Pins</td>
<td></td>
<td>33</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>BOOT to SW Pins</td>
<td></td>
<td>6.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>All Other Pins</td>
<td></td>
<td>-0.3</td>
<td>$V_{CC}+0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Junction Temperature</td>
<td>-10</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage Temperature</td>
<td>-65</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_L$</td>
<td>Lead Soldering Temperature, 10 Seconds</td>
<td></td>
<td>+300</td>
<td>°C</td>
</tr>
</tbody>
</table>

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>$V_{CC}$ Supply Voltage</td>
<td>4.75</td>
<td>5.00</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>$V_{IN}$ Supply Voltage</td>
<td></td>
<td>24</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$T_A$</td>
<td>Ambient Temperature</td>
<td>-10</td>
<td></td>
<td>+85</td>
<td>°C</td>
</tr>
<tr>
<td>$\Theta_{JA}$</td>
<td>Thermal Resistance, Junction to Ambient</td>
<td></td>
<td></td>
<td>112</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
## Electrical Characteristics

Recommended operating conditions, unless otherwise noted.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{VCC}$</td>
<td>$V_{CC}$ Current</td>
<td>LDRV, HDRV Open; $V_{SEN}$ Forced Above Regulation Point</td>
<td>850</td>
<td>1300</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Shutdown (EN-0)</td>
<td>5</td>
<td>15</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{SINK}$</td>
<td>$V_{IN}$ Current, Sinking</td>
<td>$V_{IN}$ Pin = Input Voltage Source</td>
<td>10</td>
<td>20</td>
<td>30</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{SOURCE}$</td>
<td>$V_{IN}$ Current, Sourcing</td>
<td>$V_{IN}$ Pin = GND</td>
<td>7</td>
<td>15</td>
<td>20</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{SSD}$</td>
<td>$V_{IN}$ Current, Shutdown</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$V_{UVLO}$</td>
<td>UVLO Threshold</td>
<td>Rising $V_{CC}$</td>
<td>4.30</td>
<td>4.55</td>
<td>4.75</td>
<td>$V$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling</td>
<td>4.10</td>
<td>4.27</td>
<td>4.50</td>
<td>$V$</td>
</tr>
<tr>
<td>$V_{UVLOH}$</td>
<td>UVLO Hysteresis</td>
<td></td>
<td>0.1</td>
<td></td>
<td>0.5</td>
<td>$V$</td>
</tr>
</tbody>
</table>

### Oscillator

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{osc}$</td>
<td>Frequency</td>
<td>$V_{IN} &gt; 5V$</td>
<td>255</td>
<td>300</td>
<td>345</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 0V$</td>
<td>510</td>
<td>600</td>
<td>690</td>
</tr>
<tr>
<td>$V_{PP}$</td>
<td>Ramp Amplitude</td>
<td>$V_{IN} = 16V$</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} &gt; 5V$</td>
<td>1.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{RAMP}$</td>
<td>Ramp Offset</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$G$</td>
<td>Ramp / $V_{IN}$ Gain</td>
<td>$V_{IN} \geq 3V$</td>
<td>125</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$1V &lt; V_{IN} &lt; 3V$</td>
<td>250</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Reference and Soft-Start

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{REF}$</td>
<td>Internal Reference Voltage</td>
<td></td>
<td>0.891</td>
<td>0.900</td>
<td>0.909</td>
</tr>
<tr>
<td>$I_{SS}$</td>
<td>Soft-Start Current</td>
<td>At Startup</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>Soft-Start Complete Threshold</td>
<td></td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### PWM Converter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{OUT}$</td>
<td>Load Regulation</td>
<td>$I_{OUT}$ from 0 to 3A, $V_{IN}$ from 2 to 24V</td>
<td>-1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SEN}$</td>
<td>$V_{SEN}$ Bias Current</td>
<td>$V_{IN}$ from 2 to 24V</td>
<td>50</td>
<td>80</td>
<td>150</td>
</tr>
<tr>
<td>$VOUT$</td>
<td>VOUT Pin Input Impedance</td>
<td></td>
<td>40</td>
<td>55</td>
<td>65</td>
</tr>
<tr>
<td>$UVLO_{TSD}$</td>
<td>Under-Voltage Shutdown</td>
<td>% of Set Point, 2$\mu$s Noise Filter</td>
<td>70</td>
<td>75</td>
<td>80</td>
</tr>
<tr>
<td>$I_{SNS}$</td>
<td>Over-Current Threshold</td>
<td>$R_{LIM} = 68.5K\Omega$, Figure 6</td>
<td>115</td>
<td>144</td>
<td>172</td>
</tr>
<tr>
<td>$UVLO$</td>
<td>Over-Voltage Threshold</td>
<td>% of Set Point, 2$\mu$s Noise Filter</td>
<td>113</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Output Drivers

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDRV</td>
<td>Output Resistance</td>
<td>Sourcing</td>
<td>8.0</td>
<td>15.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking</td>
<td>3.2</td>
<td>4.0</td>
<td></td>
</tr>
<tr>
<td>LDRV</td>
<td>Output Resistance</td>
<td>Sourcing</td>
<td>8.0</td>
<td>15.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking</td>
<td>1.5</td>
<td>2.4</td>
<td></td>
</tr>
</tbody>
</table>

*Continued on following page…*
### Electrical Characteristics (Continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Power-Good Output and Control Pins</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lower Threshold</td>
<td>% of Set Point, 2µs Noise Filter</td>
<td>86</td>
<td>92</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Upper Threshold</td>
<td>% of Set Point, 2µs Noise Filter</td>
<td>110</td>
<td>115</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>PGOOD Output Low</td>
<td>$I_{PGOOD} = 4mA$</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Leakage Current</td>
<td>$V_{PULLUP} = 5V$</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Soft-Start Voltage, PGOOD Enabled</td>
<td></td>
<td>1.5</td>
<td></td>
<td></td>
<td></td>
<td>% $V_{REF2}$</td>
</tr>
<tr>
<td></td>
<td>EN, FPWM Inputs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>
Functional Description

Overview
The FAN5234 is a PWM controller intended for low-voltage power applications in notebook, desktop, and sub-notebook PCs. The output voltage of the controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

The synchronous buck converter can operate from an unregulated DC source (such as a notebook battery), with voltage ranging from 2V to 24V, or from a regulated system rail. In either case, the IC is biased from a +5V source. The PWM modulator uses an average-current-mode control with input voltage feed-forward for simplified feedback loop compensation and improved line regulation. The controller includes integrated feedback loop compensation that dramatically reduces the number of external components.

Depending on the load level, the converter can operate in fixed-frequency PWM Mode or in Hysteretic Mode. Switch-over from PWM to Hysteretic Mode improves the converters’ efficiency at light loads and prolongs battery run time. In Hysteretic Mode, a comparator is synchronized to the main clock to allow seamless transition between the operational modes and reduced channel-to-channel interaction.

The Hysteretic Mode of operation can be inhibited independently using the FPWM pin if variable frequency operation is not desired.

Oscillator

Table 1. Converter Operating Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>fSW</th>
<th>Converter Power</th>
<th>VIN Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery</td>
<td>300</td>
<td>2 to 24V</td>
<td>Battery (&gt;5V)</td>
</tr>
<tr>
<td>Fixed 300</td>
<td>300</td>
<td>&lt;5.5V Fixed</td>
<td>100KΩ to GND</td>
</tr>
<tr>
<td>Fixed 600</td>
<td>600</td>
<td>&lt;5.5V Fixed</td>
<td>GND</td>
</tr>
</tbody>
</table>

When V_IN is from the battery, the oscillator ramp amplitude is proportional to V_IN, providing voltage feed-forward control for improved loop response. When in either of the fixed modes, oscillator ramp amplitude is fixed. The operating frequency is determined according to the connection on the VIN pin (see Table 1).

Initialization and Soft Start

Assuming EN is HIGH, FAN5234 is initialized when V_CC exceeds the rising UVLO threshold. Should V_CC drop below the UVLO threshold, an internal power-on reset function disables the chip.

The voltage at the positive input of the error amplifier is limited by the voltage at the SS pin, which is charged with 5mA current source. Once C_SS has charged to V_REF (0.9V), the output voltage is in regulation. The time it takes SS to reach 0.9V is:

\[ t_{0.9} = \frac{0.9V \times C_{SS}}{5} \]  

where \( t_{0.9} \) is in seconds if C_SS is in \( \mu \)F.

When SS reaches 1.5V, the power-good outputs are enabled and Hysteretic Mode is allowed. The converter is forced into PWM Mode during soft-start.

Operation Mode Control

The mode-control circuit changes the converter’s mode from PWM to Hysteretic and vice versa based on the voltage polarity of the SW node when the lower MOSFET is conducting and the converters operate in fixed-frequency PWM Mode, as shown in Figure 4. This mode achieves high efficiency at nominal load. When the load current decreases to the point where the inductor current flows through the lower MOSFET in the “reverse” direction, the SW node becomes positive and the mode is changed to Hysteretic, which achieves higher efficiency at low currents by decreasing the effective switching frequency.

To prevent accidental mode change or "mode chatter," the transition from PWM to Hysteretic Mode occurs when the SW node is positive for eight consecutive clock cycles (see Figure 4). The polarity of the SW node is sampled at the end of the lower MOSFET conduction time. At the transition between PWM and Hysteretic Mode, both the upper and lower MOSFETs are turned off. The SW node "rings" based on the output inductor and the parasitic capacitance on the SW node and settles out at the value of the output voltage.

The boundary value of inductor current, where current becomes discontinuous, is estimated by the following:

\[ I_{LOAD(DIS)} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{2f_{SW}L_{OUT}V_{IN}} \]  

Hysteretic Mode

Conversely, the transition from Hysteretic Mode to PWM Mode occurs when the SW node is negative for eight consecutive cycles.

A sudden increase in the output current causes a change from Hysteretic to PWM Mode. This load increase causes an instantaneous decrease in the output voltage due to the voltage drop on the output capacitor ESR. If the load causes the output voltage (as presented at V_{SEN}) to drop below the hysteretic regulation level (20mV below V_{REF}), the mode is changed to PWM on the next clock cycle.

In Hysteretic Mode, the PWM comparator and the error amplifier that provide control in PWM Mode are inhibited and the hysteretic comparator is activated. In Hysteretic Mode the low-side MOSFET is operated as a synchronous rectifier, where the voltage across (V_{DS(on)}) is monitored and it is switched off when V_{DS(on)} goes positive (current flowing back from the load), allowing the diode to block reverse conduction.
The hysteretic comparator causes HDRV turn-on when the output voltage (at \( V_{\text{SEN}} \)) falls below the lower threshold (10mV below \( V_{\text{REF}} \)) and terminates the PFM signal when \( V_{\text{SEN}} \) rises over the higher threshold (5mV above \( V_{\text{REF}} \)).

The switching frequency is primarily a function of:

- Spread between the two hysteretic thresholds
- \( I_{\text{LOAD}} \)
- Output inductor and capacitor ESR

A transition back to PWM Continuous Conduction Mode or (CCM) occurs when the inductor current rises sufficiently to stay positive for eight consecutive cycles. This occurs when:

\[
I_{\text{LOAD(CCM)}} = \left( \frac{\Delta V_{\text{HYSTERESIS}}}{2 \times \text{ESR}} \right)
\]

where \( \Delta V_{\text{HYSTERESIS}} = 15\text{mV} \) and ESR is the equivalent series resistance of \( C_{\text{OUT}} \).

Due to different control mechanisms, the value of the load current where transition into PWM operation takes place is typically higher compared to the load level at which transition into Hysteretic Mode occurs. Hysteretic Mode can be disabled by setting the FPWM pin HIGH.

### Current Processing

The following discussion refers to Figure 6.

The current through \( R_{\text{SENSE}} \) resistor (\( I_{\text{NSNS}} \)) is sampled shortly after Q2 is turned on. That current is held and summed with the output of the error amplifier. This effectively creates a current-mode control loop. The resistor connected to the ISNS pin (\( R_{\text{SENSE}} \)) sets the gain in the current feedback loop. Equation 4 estimates the recommended value of \( R_{\text{SENSE}} \) as a function of the maximum load current (\( I_{\text{LOAD(MAX)}} \)) and the value of the MOSFET \( R_{\text{DS(ON)}} \). \( R_{\text{SENSE}} \) must be kept higher than 700\( \Omega \) even if the number calculated comes out less than 700\( \Omega \):

\[
R_{\text{SENSE}} = \left( \frac{I_{\text{LOAD(MAX)}} \times R_{\text{DS(ON)}}}{150\mu\text{A}} \right) - 100
\]

**Setting the Current Limit**

A ratio of \( I_{\text{NSNS}} \) is also compared to the current established when a 0.9V internal reference drives the ILIM pin:

\[
R_{\text{LIM}} = \frac{11 I_{\text{LOAD}}}{(100 + R_{\text{DS(ON)}})}
\]

Since the tolerance on the current limit is largely dependent on the ratio of the external resistors, it is fairly accurate if the voltage drop on the switching node side of \( R_{\text{SENSE}} \) is an accurate representation of the load current. When using the MOSFET as the sensing element, the variation of \( R_{\text{DS(ON)}} \) causes proportional variation in \( I_{\text{NSNS}} \). This value varies from device to device and has a typical junction temperature coefficient of about 0.4%/°C (consult the MOSFET datasheet for actual values), the actual current limit set point decreases proportional to increasing MOSFET die temperature. A factor of 1.6 in the current limit set point should compensate for all MOSFET \( R_{\text{DS(ON)}} \) variations, assuming the MOSFET’s heat sinking keep its operating die temperature below 125°C.
More accurate sensing can be achieved by using a resistor (R1) instead of the $R_{DS(on)}$ of the FET, as shown in Figure 5. This approach causes higher losses, but yields greater accuracy in both $V_{DROOP}$ and $I_{LIMIT}$. R1 is a low value (e.g. 10mΩ) resistor.

Current limit ($I_{LIMIT}$) should be set high enough to allow inductor current to rise in response to an output load transient. Typically, a factor of 1.2 is sufficient. Since $I_{LIMIT}$ is a peak current cut-off value, multiply $I_{LOAD(MAX)}$ by the inductor ripple current (use 25%). For example, in Figure 1 the target for $I_{LIMIT}$ would be:

$$I_{LIMIT} > 1.2 \times 1.25 \times 1.6 \times 3.5A \approx 8.5A$$

(6)

**Duty Cycle Clamp**

During severe load increase, the error amplifier output can go to its upper limit, pushing a duty cycle to almost 100% for a significant amount of time. This could cause a large increase of the inductor current and lead to a long recovery from a transient over-current condition or even to a failure at high input voltages. To prevent this, the output of the error amplifier is clamped to a fixed value after two clock cycles if severe output voltage excursion is detected, limiting maximum duty cycle to:

$$D_{C} = \frac{V_{out}}{V_{w}} + \left(\frac{2.4}{V_{IN}}\right)$$

(7)

This is designed to not interfere with normal PWM operation. When FPWM is grounded, the duty cycle clamp is disabled and the maximum duty cycle is 87%.

**Gate Driver**

The adaptive gate control logic translates the internal PWM control signal into the MOSFET gate drive signals, providing necessary amplification, level shifting, and shoot-through protection. It also has functions that help optimize the IC performance over a wide range of operating conditions. Since MOSFET switching time can vary dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring the gate-to-source voltages of both upper and lower MOSFETS. The lower MOSFET drive is not turned on until the gate-to-source voltage of the upper MOSFET has decreased to less than approximately 1V. Similarly, the upper MOSFET is not turned on until the gate-to-source voltage of the lower MOSFET has decreased to less than approximately 1V. This allows a wide variety of upper and lower MOSFETS to be used without concern for simultaneous conduction or shoot-through.

There must be a low-resistance, low-inductance path between the driver pin and the MOSFET gate for the adaptive dead-time circuit to work properly. Any delay along that path subtracts from the delay generated by the adaptive dead-time circuit and shoot-through may occur.

**Frequency Loop Compensation**

Due to the implemented current-mode control, the modulator has a single-pole response with -1 slope at frequency determined by load. Therefore:

$$f_{po} = \frac{1}{2\pi R_{o} C_{o}}$$

(8)

where $R_{o}$ is load resistance and $C_{o}$ is load capacitance.

For this type of modulator, type-2 compensation circuit is usually sufficient. To reduce the number of external components and simplify the design task, the PWM controller has an internally compensated error amplifier. Figure 7 shows a type two amplifier, its response, and the responses of a current mode modulator and the converter. The type-2 amplifier, in addition to the pole at the origin, has a zero-pole pair that causes a flat gain region at frequencies between the zero and the pole.
This region is also associated with phase “bump” or reduced phase shift. The amount of phase shift reduction depends on the width of the region of flat gain and has a maximum value of 90°. To further simplify the converter compensation, the modulator gain is kept independent of the input voltage variation by providing feed-forward of VIN to the oscillator ramp.

The zero frequency, the amplifier high-frequency gain, and the modulator gain are chosen to satisfy most typical applications. The crossover frequency appears at the point where the modulator attenuation equals the amplifier high-frequency gain. The system designer must specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. With this type of compensation, plenty of phase margin is achieved due to zero-pole pair phase “boost.”

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within the 10kHz to 50kHz range gives some additional phase boost. There is an opposite trend in mobile applications to keep the output capacitor as small as possible.

**Protections**

The converter output is monitored and protected against extreme overload, short circuit, over-voltage, and under-voltage conditions.

A sustained overload on an output sets the PGOOD pin LOW and latches off the chip. Operation is restored by cycling the VCC voltage or by toggling the EN pin.

If VOUT drops below the under-voltage threshold, the chip shuts down immediately.

**Over-Current Sensing**

If the circuit's current-limit signal (“I_LIMIT det” in Figure 6) is HIGH at the beginning of a clock cycle, a pulse-skipping circuit is activated and HDRV is inhibited. The circuit continues to pulse skip in this manner for the next eight clock cycles. If at any time from the ninth to the sixteenth clock cycle, the I_LIMIT det is again reached, the over-current protection latch is set, disabling the chip. If I_LIMIT det does not occur between cycles 9 and 16, normal operation is restored and the over-current circuit resets itself.

Figure 8. Over-Current Protection Waveforms

**Over-Voltage / Under-Voltage Protection**

Should the VSEN voltage exceed 120% of VREF (0.9V) due to an upper MOSFET failure or for other reasons, the over-voltage protection comparator forces LDRV HIGH. This action actively pulls down the output voltage and, in the event of the upper MOSFET failure, eventually blows the battery fuse. As soon as the output voltage drops below the threshold, the OVP comparator is disengaged.

This OVP scheme provides a ‘soft’ crowbar function to tackle severe load transients and does not invert the output voltage when activated — a common problem for latched OVP schemes.

Similarly, if an output short-circuit or severe load transient causes the output to droop to less than 75% of its regulation set point, the regulator shuts down.

**Over-Temperature Protection**

The chip incorporates an over-temperature protection circuit that shuts the chip down when a die temperature reaches 150°C. Normal operation is restored at die temperature below 125°C with internal power on reset asserted, resulting in a full soft-start cycle.
Design and Component Selection

Guidelines

As an initial step, define operating input voltage range, output voltage, and minimum and maximum load currents for the controller.

For the examples in the following discussion, select components for:

- \( V_{IN} \) from 5V to 20V
- \( V_{OUT} = 1.8V \) at \( I_{LOAD(MAX)} = 3.5A \)

Setting the Output Voltage

The output voltage is divided down by a voltage divider to the VSEN pin (for example, R1 and R2 in Figure 1). The output voltage therefore is:

\[
\frac{V_{OUT}}{R_2} = \frac{0.9V}{R_1} \tag{11}
\]

To minimize noise pickup on this node, keep the resistor to GND (R2) below 2K; for example R2 at 1.82K, then choose R5:

\[
R_5 = \frac{(1.82K\Omega) 	imes (1.8V - 0.9)}{0.9} = 1.82K \tag{12}
\]

Output Inductor Selection

The minimum practical output inductor value keeps inductor current just on the boundary of continuous conduction at some minimum load. The industry standard practice is to choose the ripple current to be somewhere from 15% to 35% of the nominal current. At light-load, the ripple current determines the point where the converter automatically switches to Hysteretic Mode to sustain high efficiency. The following equations help to choose the proper value of the output filter inductor:

\[
\Delta I = 2I_{MIN} - \frac{\Delta V}{ESR} \tag{13}
\]

where \( \Delta I \) is the inductor ripple current, which is chosen for 20% of the full load current and \( \Delta V_{OUT} \) is the maximum output ripple voltage allowed:

\[
L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \tag{14}
\]

For this example, use:

\[
V_{IN} = 20V,\ V_{OUT} = 1.8V \tag{15}
\]

\[
\Delta I = 20\% \times 3.5A = 0.7A
\]

\[
f_{SW} = 300KHz.
\]

Therefore;

\[
L \approx 8\mu H \tag{16}
\]

Output Capacitor Selection

The output capacitor serves two major functions in a switching power supply. Along with the inductor, it filters the sequence of pulses produced by the switcher and it supplies the load transient currents. The output capacitor requirements are usually dictated by ESR, inductor ripple current (\( \Delta I \)), and the allowable ripple voltage (\( \Delta V \)):

\[
ESR < \frac{\Delta V}{\Delta I} \tag{17}
\]

For this example,

\[
ESR_{MAX} = \frac{\Delta V}{\Delta I} = \frac{0.1V}{0.7A} = 142m\Omega
\]

In addition, the capacitor's ESR must be low enough to allow the converter to stay in regulation during a load step. The ripple voltage due to ESR for the converter in Figure 1 is 100mVpp. Some additional ripple will appear due to the capacitance value itself:

\[
\Delta V = \frac{\Delta I}{C_{OUT} \times 8 \times f_{SW}} \tag{18}
\]

which is only about 1.5mV for the converter in Figure 1 and can be ignored.

The capacitor must also be rated to withstand the RMS current, which is approximately \( 0.3 \times \Delta I \) or about 210mA for the converter in Figure 1. High-frequency decoupling capacitors should be placed as close to the loads as physically possible.

Input Capacitor Selection

The input capacitor should be selected by its ripple current rating. The input RMS current at maximum load current (\( I_L \)) is:

\[
I_{RMS} = I_L \sqrt{D - D^2} \tag{19}
\]

where the converter duty cycle; \( D = \frac{V_{OUT}}{V_{IN}} \), which for the circuit in Figure 1, with \( V_{IN} = 6 \), calculates to \( I_{RMS} \approx 1.6A \).

Power MOSFET Selection

Losses in a MOSFET are the sum of its switching (\( P_{SW} \)) and conduction (\( P_{COND} \)) losses.

In typical applications, the FAN5234 converter's output voltage is low with respect to its input voltage. Therefore, the lower MOSFET (Q2) is conducting the full-load current for most of the cycle. Q2 should therefore be selected to minimize conduction losses, thereby selecting a MOSFET with low \( R_{DS(ON)} \).

In contrast, the high-side MOSFET (Q1) has a shorter duty cycle, and its conduction loss has less impact. Q1, however, sees most of the switching losses, so Q1's primary selection criteria should be gate charge.
High-Side Losses

Figure 9 shows a MOSFET's switching interval, with the upper graph being the voltage and current on the drain-to-source and the lower graph detailing $V_{GS}$ vs. time with a constant current charging the gate. The x-axis therefore is also representative of gate charge ($Q_G$). $C_{ISS} = C_{GD} + C_{GS}$, and it controls $t_1$, $t_2$, and $t_4$ timing. $C_{GD}$ receives the current from the gate driver during $t_3$ (as $V_{DS}$ is falling). The gate charge ($Q_G$) parameters on the lower graph are either specified or can be derived from MOSFET datasheets.

Assuming switching losses are about the same for both the rising edge and falling edge, $Q_1$'s switching losses occur during the shaded time when the MOSFET has voltage across it and current through it.

These losses are given by:

$$P_{UPPER} = P_{SW} + P_{COND}$$  \hspace{1cm} (20)

where:

$$P_{SW} = \left(\frac{V_{DS}}{2} \times I_L \times 2 \times t_S\right) f_{SW}$$  \hspace{1cm} (21)

$$P_{COND} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^2 \times R_{DS(ON)}$$  \hspace{1cm} (22)

$P_{UPPER}$ is the upper MOSFET’s total losses and $P_{SW}$ and $P_{COND}$ are the switching and conduction losses for a given MOSFET. $R_{DS(ON)}$ is at the maximum junction temperature ($T_J$). $t_S$ is the switching period (rise or fall time) and is $t_2+t_3$ in Figure 9.

![Figure 9. Switching Losses and $Q_G$ ($C_{SS} = C_{GS} \parallel C_{GD}$)](image)

The driver’s impedance and $C_{ISS}$ determine $t_2$ while $t_3$’s period is controlled by the driver's impedance and $Q_{GD}$. Since most of $t_S$ occurs when $V_{DS} = V_{SP}$, use a constant current assumption for the driver to simplify the calculation of $t_S$:

$$t_S = \frac{Q_{G(SW)}^{SW}}{I_{DRIVER}^{SW}} = \frac{Q_{G(SW)}^{SW}}{\left(\frac{V_{CC} - V_{SP}}{R_{DRIVER}^{SW} + R_{GATE}^{SW}}\right)}$$  \hspace{1cm} (23)

Most MOSFET vendors specify $Q_{GD}$ and $Q_{GS}$. $Q_{G(SW)}$ can be determined as:

$$Q_{G(SW)} = Q_{GD} + Q_{GS} - Q_{TH}$$  \hspace{1cm} (24)

where $Q_{TH}$ is the gate charge required to get the MOSFET to its threshold ($V_{TH}$).

For the high-side MOSFET, $V_{DS} = V_{IN}$, which can be as high as 20V in a typical portable application. Care should be taken to include the delivery of the MOSFET’s gate power ($P_{GATE}$) in calculating the power dissipation required for the FAN5234:

$$P_{GATE} = Q_g \times V_{CC} \times f_{SW}$$  \hspace{1cm} (25)

where $Q_g$ is the total gate charge to reach $V_{CC}$.

Low-Side Losses

$Q_2$ switches on or off with its parallel Schottky diode conducting; therefore, $V_{DS} \approx 0.5V$. Since $P_{SW}$ is proportional to $V_{DS}$, $Q_2$’s switching losses are negligible and $Q_2$ is selected based on $R_{DS(ON)}$ only.

Conduction losses for $Q_2$ are given by:

$$P_{COND} = (1 - D) \times I_{OUT}^2 \times R_{DS(ON)}$$  \hspace{1cm} (26)

where $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the MOSFET at the highest operating junction temperature and

$$D = \frac{V_{OUT}}{V_{IN}}$$ is the minimum duty cycle for the converter.

Since $D_{MIN} < 20\%$ for portable computers, $(1-D)=1$ produces a conservative result, simplifying the calculation.

The maximum power dissipation ($P_{D(MAX)}$) is a function of the maximum allowable die temperature of the low-side MOSFET, the $\Theta_{JA}$, and the maximum allowable ambient temperature rise:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\Theta_{JA}}$$  \hspace{1cm} (27)

$\Theta_{JA}$ depends primarily on the amount of PCB area that can be devoted to heat sinking (see AN-1029 — Maximum Power Enhancement Techniques for SO-8 Power MOSFET for MOSFET thermal information).
Table 2. Build Of Materials for 1.8V, 3.5A Regulator

<table>
<thead>
<tr>
<th>Description</th>
<th>Qty.</th>
<th>Ref.</th>
<th>Vendor</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitor 68μF, Tantalum, 25V, ESR 95mΩ</td>
<td>1</td>
<td>C1</td>
<td>AVX.</td>
<td>TPSV686*025#095</td>
</tr>
<tr>
<td>Capacitor 10nF, Ceramic</td>
<td>2</td>
<td>C2, C3</td>
<td>Any</td>
<td></td>
</tr>
<tr>
<td>Capacitor 68μF, Tantalum, 6V, ESR 1.8Ω</td>
<td>1</td>
<td>C4</td>
<td>AVX.</td>
<td>TAJV686*006</td>
</tr>
<tr>
<td>Capacitor 0.1μF, Ceramic</td>
<td>2</td>
<td>C5</td>
<td>Any</td>
<td></td>
</tr>
<tr>
<td>Capacitor 330μF, Tantalum, 6V, ESR 100mΩ</td>
<td>2</td>
<td>C6</td>
<td>AVX.</td>
<td>TPSE337*006#0100</td>
</tr>
<tr>
<td>1.82KΩ, 1% Resistor</td>
<td>2</td>
<td>R1, R2</td>
<td>Any</td>
<td></td>
</tr>
<tr>
<td>1.3KΩ, 1% Resistor</td>
<td>1</td>
<td>R3</td>
<td>Any</td>
<td></td>
</tr>
<tr>
<td>100KΩ, 5% Resistor</td>
<td>1</td>
<td>R4</td>
<td>Any</td>
<td></td>
</tr>
<tr>
<td>56.2KΩ, 1% Resistor</td>
<td>1</td>
<td>R5</td>
<td>Any</td>
<td></td>
</tr>
<tr>
<td>Schottky Diode; 0.5A, 20V</td>
<td>2</td>
<td>D1</td>
<td>Fairchild Semiconductor</td>
<td>MBR05S0L</td>
</tr>
<tr>
<td>Inductor 8.4μH, 6A</td>
<td>1</td>
<td>L1</td>
<td>Any</td>
<td></td>
</tr>
<tr>
<td>Dual MOSFET with Schottky</td>
<td>1</td>
<td>Q</td>
<td>Fairchild Semiconductor</td>
<td>FDS6986AS(1)</td>
</tr>
<tr>
<td>PWM Controller</td>
<td>1</td>
<td>U1</td>
<td>Fairchild Semiconductor</td>
<td>FAN5234</td>
</tr>
</tbody>
</table>

Note:
1. If currents above 4A continuous are required, use single SO-8 packages. For more information, refer to the Power MOSFET Selection Section and AN-6002 for design calculations.

Layout Considerations

Switching converters, even during normal operation, produce short pulses of current that could cause substantial ringing and be a source of EMI if layout constrains are not observed.

There are two sets of critical components in a DC-DC converter. The switching power components process large amounts of energy at high rate and are noise generators. The low-power components responsible for bias and feedback functions are sensitive to noise.

A multi-layer printed circuit board is recommended. Dedicate one solid layer for a ground plane. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels.

Notice all the nodes that are subjected to high dV/dt voltage swing; such as SW, HDRV, and LDRV. All surrounding circuitry tends to couple the signals from these nodes through stray capacitance. Do not oversize copper traces connected to these nodes. Do not place traces connected to the feedback components adjacent to these traces. It is not recommended to use high density interconnect systems, or micro-vias, on these signals. The use of blind or buried vias should be limited to the low-current signals only. The use of normal thermal vias is at the discretion of the designer.

Keep the wiring traces from the IC to the MOSFET gate and source as short as possible and capable of handling peak currents of 2A. Minimize the area within the gate-source path to reduce stray inductance and eliminate parasitic ringing at the gate.

Locate small critical components, like the soft-start capacitor and current sense resistors, as close as possible to the respective pins of the IC.

The FAN5234 utilizes advanced packaging technologies with lead pitches of 0.6mm. High-performance analog semiconductors utilizing narrow lead spacing may require special considerations in PWB design and manufacturing. It is critical to maintain proper cleanliness of the area surrounding these devices. It is not recommended to use any type of rosin or acid core solder, or the use of flux, in either the manufacturing or touch up process as these may contribute to corrosion or enable electro-migration and / or eddy currents near the sensitive low-current signals. When chemicals are used on or near the PWB, it is suggested that the entire PWB be cleaned and dried completely before applying power.
Physical Dimensions

Figure 11. 16-Lead, Thin-Shrink Outline Package

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild’s worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor’s online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/
TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
AutoSMP™
Build It Now™
CorePlus™
CorePowerR™
CROSSOL™
CTOL™
Current Transfer Log™
DELIPLAN™
Dual Cool™
EcoSMP™
EfficientMark™
ESGC®

Fairchild®
Fairchild Semiconductor®
FACT Quiet Series®
FACT™
FAST™
FastCore™
FETBench™
FlipWAVE™
FP™

PowerPrench™
PowerXS™
Programmable Active Droop™
QS™
Quiet Series™
QuickConfigure™

Solving the world, 1mW/WAN at a time™
SquidMax™
SmartMax™
SMART START™
SP™
STEALTH™
SuperFET™
SuperSOT™ 3
SuperSOT™ 8
SuperMOS®
SyncFET™
Sync-Lock™

SYSTEM GENERAL™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, PERFORMANCE, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:
1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation’s Anti-Counterfeiting Policy. Fairchild’s Anti-Counterfeiting Policy is also stated on our external web site, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild’s quality standards for handling and storage, and provide access to Fairchild’s full range of up-to-date technical and product information.

Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assurance for parts bought from Unauthorized Sources. Fairchild is committed to combating this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

<table>
<thead>
<tr>
<th>Datasheet Identification</th>
<th>Product Status</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advance Information</td>
<td>Formative / In Design</td>
<td>Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
</tr>
<tr>
<td>Preliminary</td>
<td>First Production</td>
<td>Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.</td>
</tr>
<tr>
<td>Not Identification Needed</td>
<td>Full Production</td>
<td>Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.</td>
</tr>
<tr>
<td>Obsolete</td>
<td>Not In Production</td>
<td>Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.</td>
</tr>
</tbody>
</table>

Rev: 1.0

© 2004 Fairchild Semiconductor Corporation
FA5234 • Rev. 2.0.0
www.fairchildsemi.com