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June 2016

FCH023N65S3

N-Channel SuperFET[®] III MOSFET

650 V, 75 A, 23 mΩ

Features

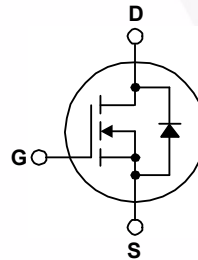
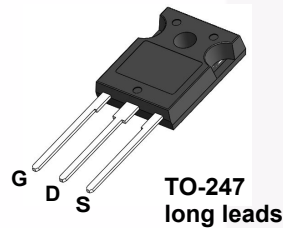
- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 19.5\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 222\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 1980\text{ pF}$)
- 100% Avalanche Tested
- RoHS Compliant

Applications

- Telecom / Server Power Supplies • UPS / Solar
- Industrial Power Supply

Description

SuperFET[®] III MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate. Consequently, SuperFET III MOSFET is suitable for various DC/AC power conversion for system miniaturization and higher efficiency.



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCH023N65S3_F155	Unit
V_{DSS}	Drain to Source Voltage	650	V
V_{GSS}	Gate to Source Voltage	- DC	± 30
		- AC (f > 1 Hz)	± 30
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	75
		- Continuous ($T_C = 100^\circ\text{C}$)	65.8
I_{DM}	Drain Current	- Pulsed (Note 1)	300
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	2025	mJ
I_{AR}	Avalanche Current (Note 1)	15	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	5.95	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	595
		- Derate Above 25°C	4.76
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FCH023N65S3_F155	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.21	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

FCH023N65S3 — N-Channel SuperFET[®] III MOSFET

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH023N65S3_F155	FCH023N65S3	TO-247 G03	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	650	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 150^\circ\text{C}$	700	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}, \text{Referenced to } 25^\circ\text{C}$	-	0.72	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 520\text{ V}, T_C = 125^\circ\text{C}$	-	6.8	-	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 7.5\text{ mA}$	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 37.5\text{ A}$	-	19.5	23	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 37.5\text{ A}$	-	66	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	-	7160	-	pF
C_{oss}	Output Capacitance		-	195	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	1980	-	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	298	-	
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400\text{ V}, I_D = 37.5\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4)	-	222	-	nC
Q_{gs}	Gate to Source Gate Charge		-	54	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	90	-	nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	0.9	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 37.5\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 2\ \Omega$ (Note 4)	-	45	-	ns
t_r	Turn-On Rise Time		-	55	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	140	-	ns
t_f	Turn-Off Fall Time		-	29	-	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	75	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	300	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 37.5\text{ A}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 37.5\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$	-	600	-	ns
Q_{rr}	Reverse Recovery Charge		-	17.9	-	μC

Notes:

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. $I_{AS} = 15\text{ A}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 75\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

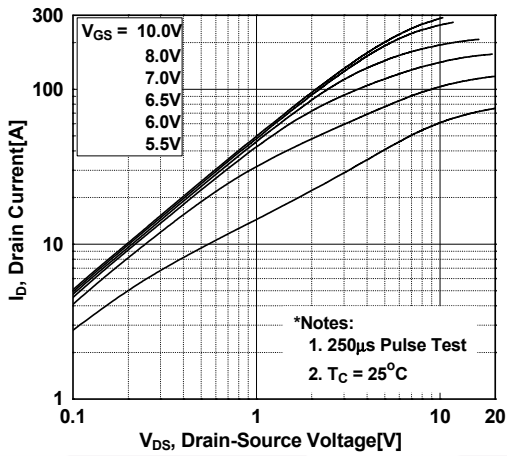


Figure 2. Transfer Characteristics

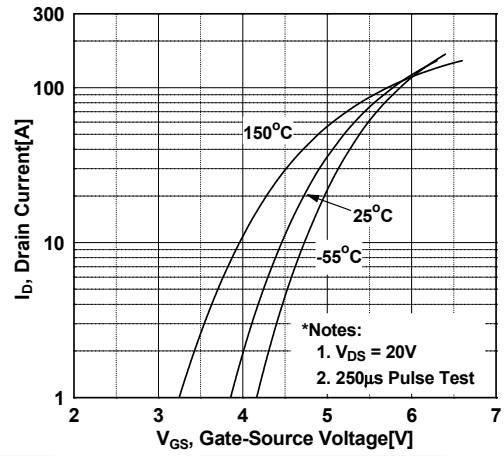


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

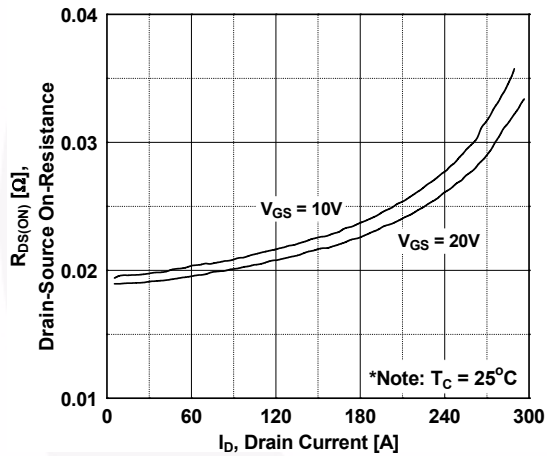


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

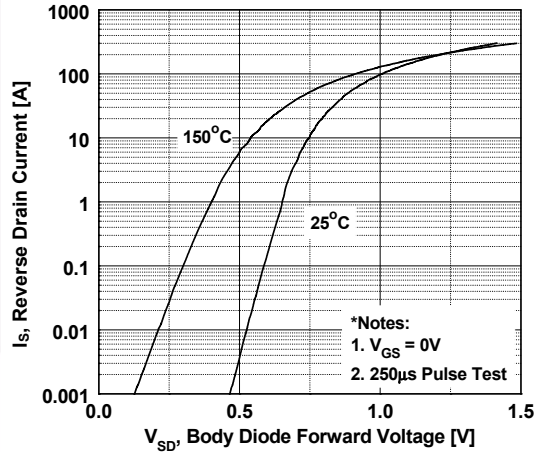


Figure 5. Capacitance Characteristics

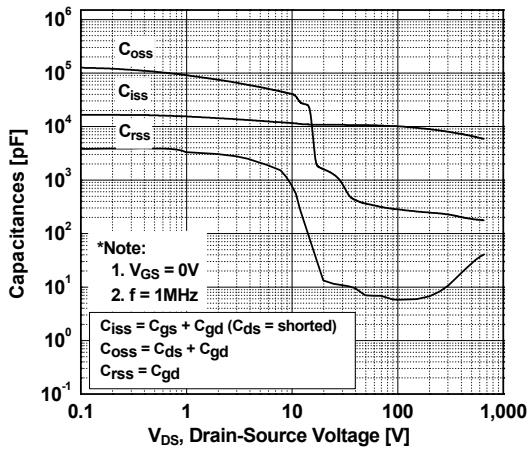
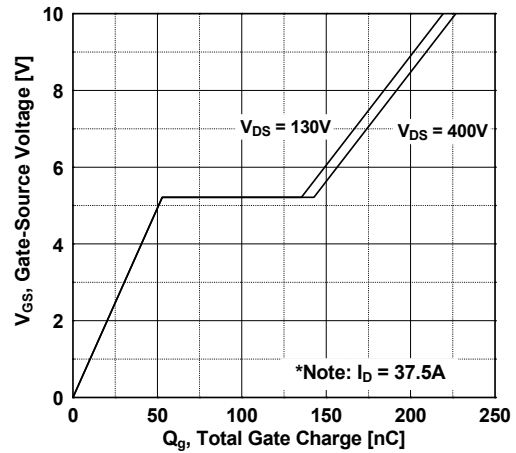


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

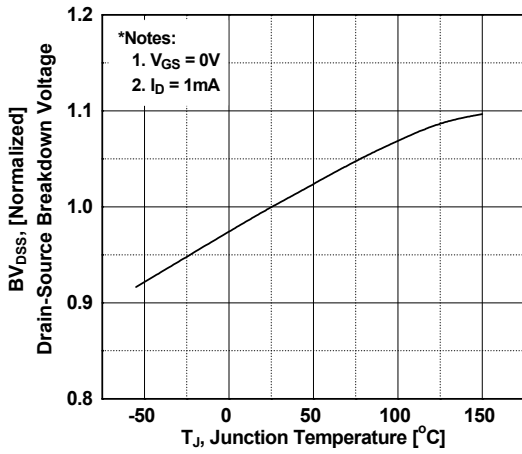


Figure 8. On-Resistance Variation vs. Temperature

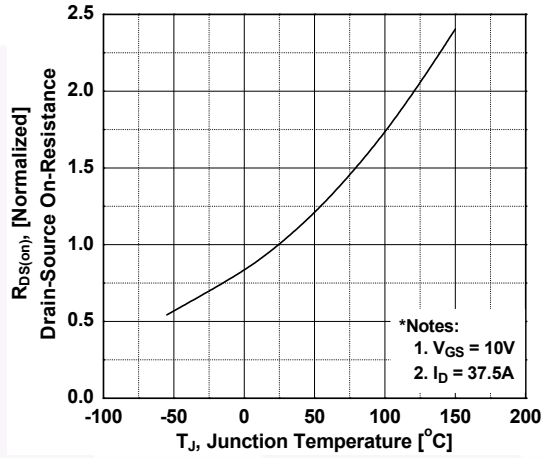


Figure 9. Maximum Safe Operating Area

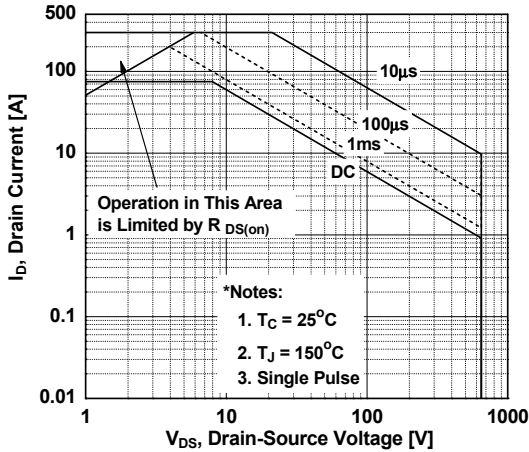


Figure 10. Maximum Drain Current vs. Case Temperature

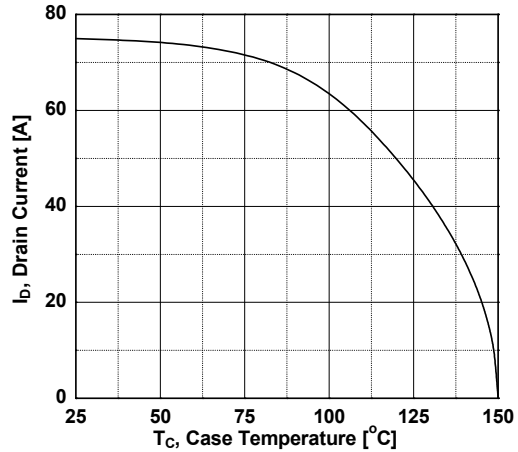
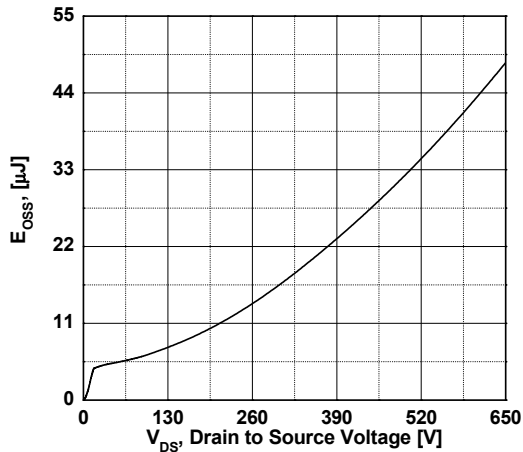
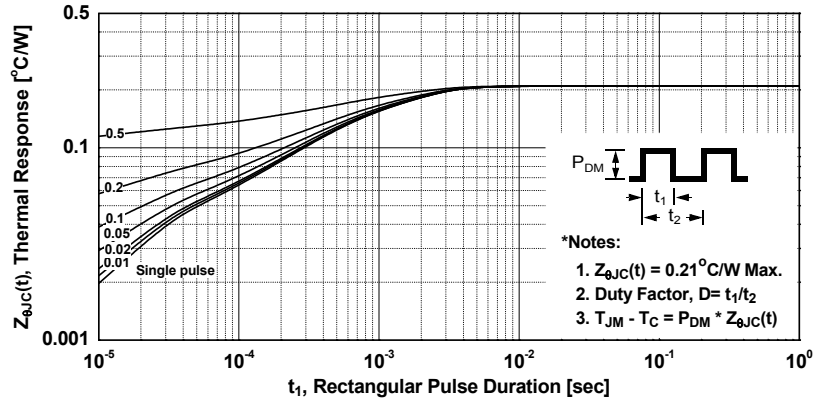


Figure 11. Eoss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



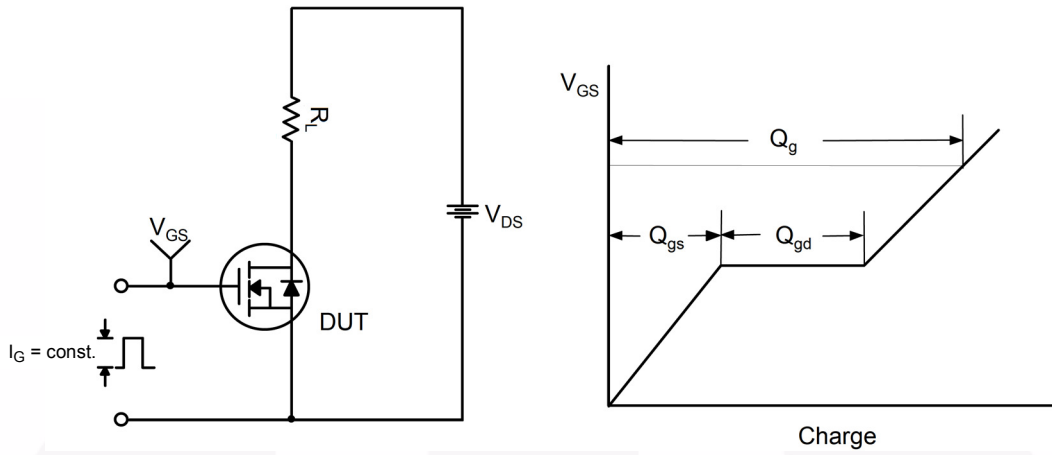


Figure 13. Gate Charge Test Circuit & Waveform



Figure 14. Resistive Switching Test Circuit & Waveforms

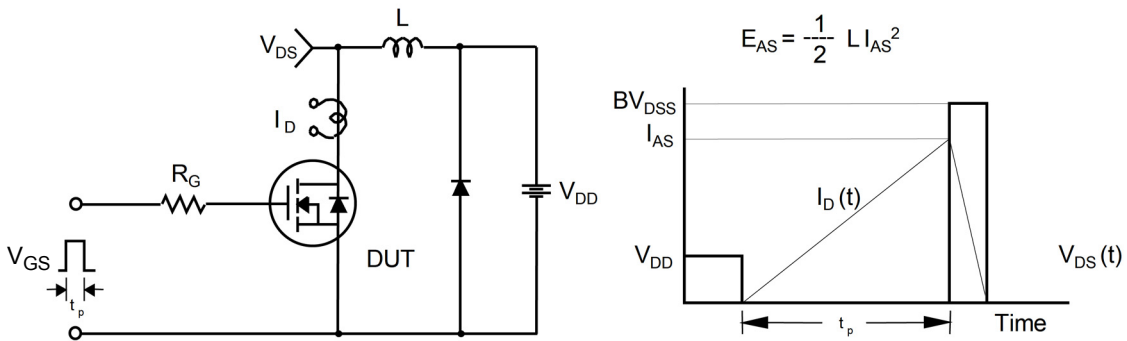


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

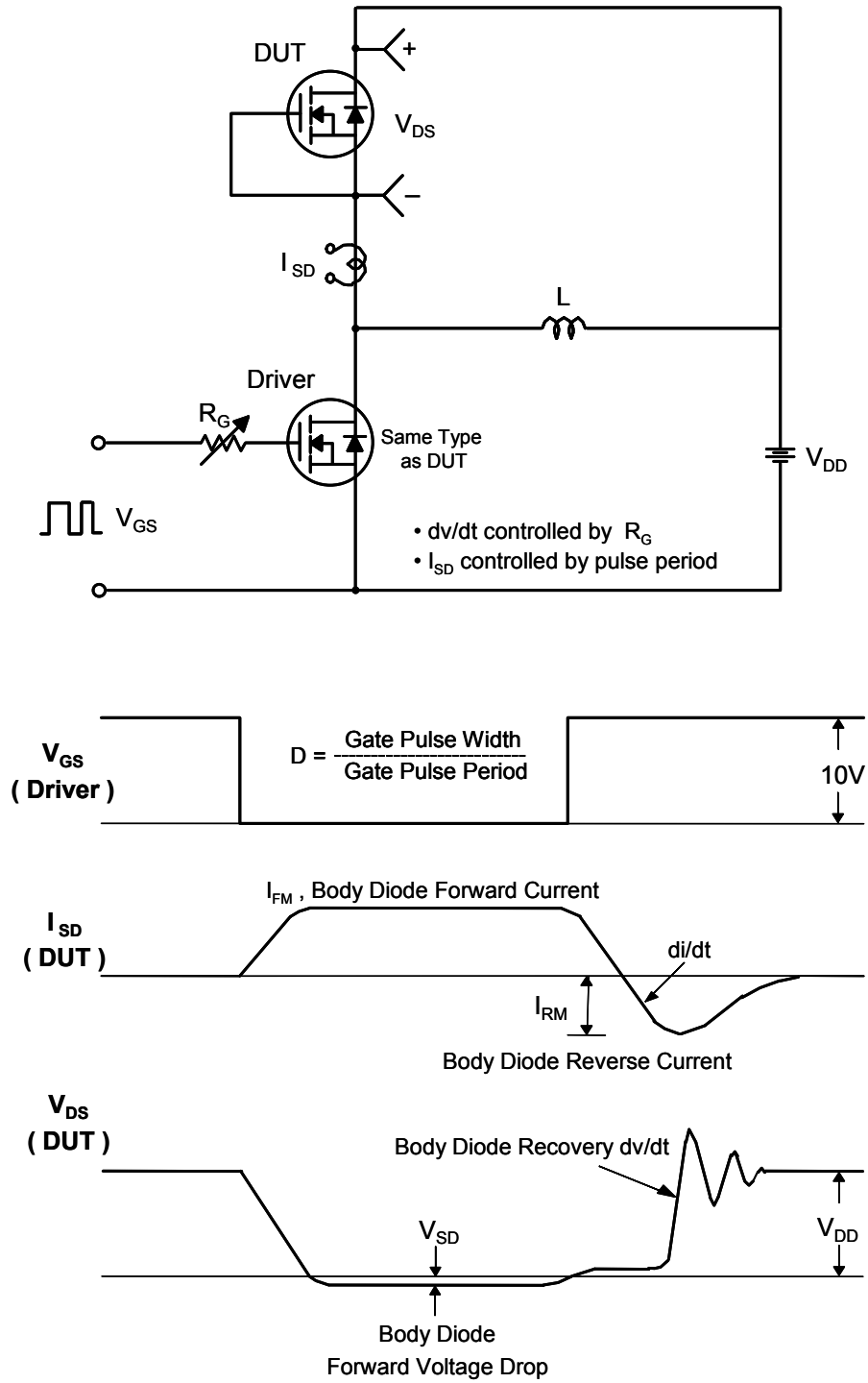
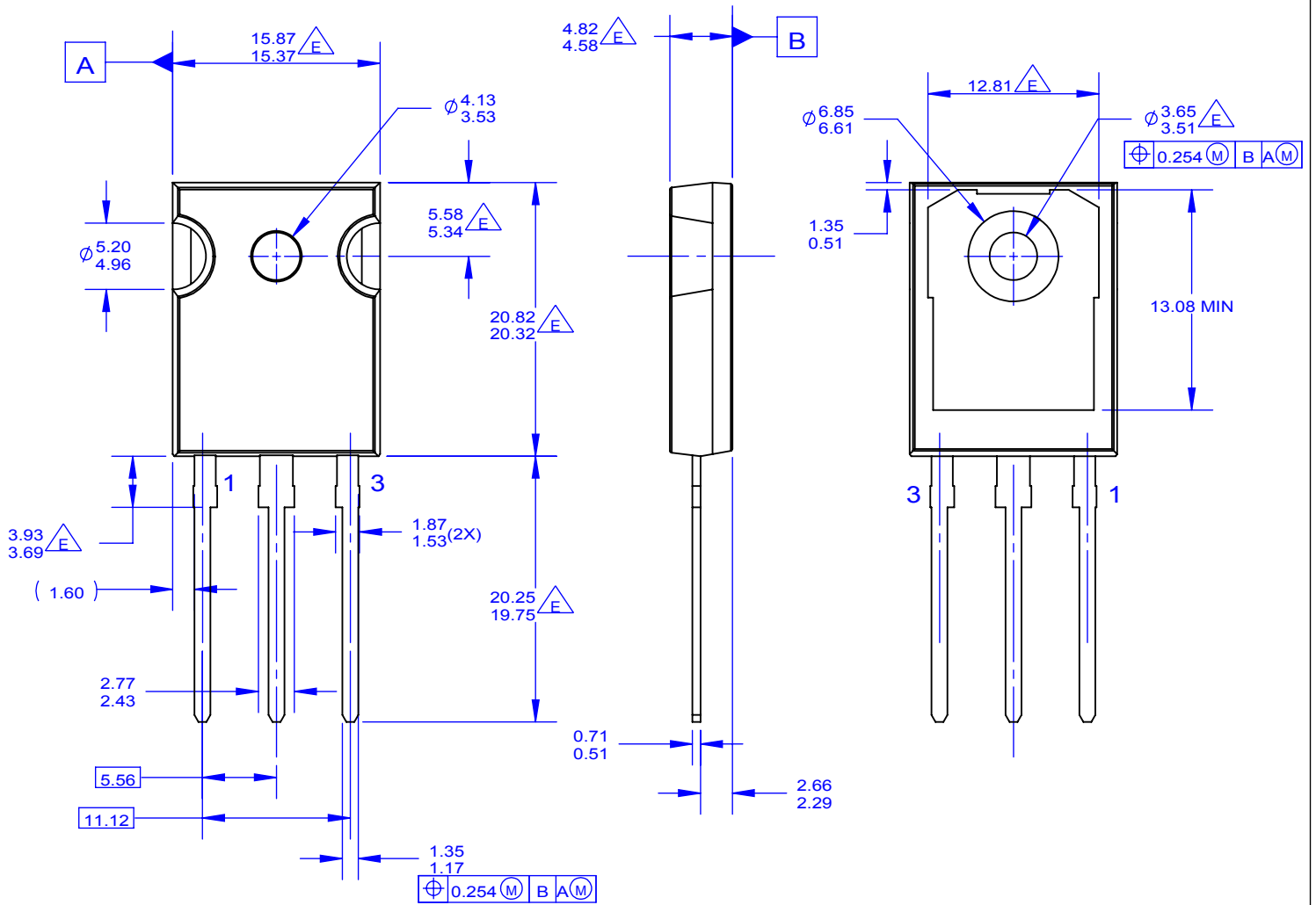


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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