**FDC658AP**

Single P-Channel Logic Level PowerTrench® MOSFET

-30V, -4A, 50mΩ

**General Description**

This P-Channel Logic Level MOSFET is produced using Fairchild's advanced PowerTrench process. It has been optimized for battery power management applications.

**Applications**

- Battery management
- Load switch
- Battery protection
- DC/DC conversion

**Features**

- Max \(r_{DS(on)}\) = 50 mΩ @ \(V_{GS} = -10\) V, \(I_D = -4A\)
- Max \(r_{DS(on)}\) = 75 mΩ @ \(V_{GS} = -4.5\) V, \(I_D = -3.4A\)
- Low Gate Charge
- High performance trench technology for extremely low \(r_{DS(on)}\)
- RoHS Compliant

**Absolute Maximum Ratings** \(T_A = 25°C\) unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{DS})</td>
<td>Drain-Source Voltage</td>
<td>-30</td>
<td>V</td>
</tr>
<tr>
<td>(V_{GS})</td>
<td>Gate-Source Voltage</td>
<td>±25</td>
<td>V</td>
</tr>
<tr>
<td>(I_D)</td>
<td>Drain Current - Continuous</td>
<td>-4</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>- Pulsed</td>
<td>-20</td>
<td></td>
</tr>
<tr>
<td>(P_D)</td>
<td>Maximum Power dissipation</td>
<td>1.6</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>(Note 1a)</td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td>(T_J, T_{STG})</td>
<td>Operating and Storage Junction Temperature Range</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Thermal Characteristics**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JJA})</td>
<td>Thermal Resistance, Junction-to-Ambient</td>
<td>(Note 1a)</td>
<td>78</td>
</tr>
<tr>
<td>(R_{JJC})</td>
<td>Thermal Resistance, Junction-to-Case</td>
<td>(Note 1)</td>
<td>30</td>
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**Package Marking and Ordering Information**

<table>
<thead>
<tr>
<th>Device Marking</th>
<th>Device</th>
<th>Reel Size</th>
<th>Tape Width</th>
<th>Quantity</th>
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<tr>
<td>.58A</td>
<td>FDC658AP</td>
<td>7inch</td>
<td>8mm</td>
<td>3000 units</td>
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### Electrical Characteristics  $T_J = 25^\circ\text{C}$ unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$BV_{DSS}$</td>
<td>Drain-Source Breakdown Voltage</td>
<td>$I_D = -250\mu$A, $V_{GS} = 0$V</td>
<td>-30</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$\Delta BV_{DSS}$</td>
<td>Breakdown Voltage Temperature Coefficient</td>
<td>$I_D = -250\mu$A, Referenced to $25^\circ$C</td>
<td>-22</td>
<td>mV/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>Zero Gate Voltage Drain Current</td>
<td>$V_{GS} = 0$V, $V_{DS} = -24$V</td>
<td>-1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{GSS}$</td>
<td>Gate-Body Leakage</td>
<td>$V_{GS} = \pm25$V, $V_{DS} = 0$V</td>
<td>±100</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Off Characteristics

- **$V_{GS(TH)}$** Gate Threshold Voltage $V_{DS} = V_{GS}, I_D = -250\mu$A $-1$, -1.8, -3 V
- **$\Delta V_{GS(TH)}$** Gate Threshold Voltage Temperature Coefficient $I_D = -250\mu$A, Referenced to $25^\circ$C 4, 50 mV/°C
- **$r_{DS(on)}$** Static Drain-Source On-Resistance $I_D = -4$A, $V_{GS} = -10$V 44, 50 mΩ
- **$I_D(ON)$** On-State Drain Current $V_{GS} = -10$V, $V_{DS} = -5$V 20 A
- **$g_{FS}$** Forward Transconductance $I_D = -4$A, $V_{DS} = -5$V 8.4 S

#### Dynamic Characteristics

- **$C_{iss}$** Input Capacitance $V_{DS} = -15$V, $V_{GS} = 0$V, $f = 1$MHz 470, 680 pF
- **$C_{oss}$** Output Capacitance $f = 1$MHz 126, 180 pF
- **$C_{rss}$** Reverse Transfer Capacitance 61, 90 pF

#### Switching Characteristics  (Note 2)

- **$t_{d(on)}$** Turn-On Delay Time $V_{DD} = -15$V, $I_D = -1$A 7, 14 ns
- **$t_r$** Turn-On Rise Time $V_{GS} = -10$V, $R_{GEN} = 6$Ω 12, 22 ns
- **$t_{d(off)}$** Turn-Off Delay Time 16, 29 ns
- **$t_f$** Turn-Off Fall Time 6, 12 ns
- **$Q_g$** Total Gate Charge $V_{DS} = -15$V, $I_D = -4$A, $V_{GS} = -5$V 6, 8.1 nC
- **$Q_{gs}$** Gate-Source Charge $V_{GS} = -15$V, $I_D = -4$A, $V_{DS} = -5$V 2.1 nC
- **$Q_{gd}$** Gate-Drain Charge 2 nC

#### Drain-Source Diode Characteristics and Maximum Ratings

- **$I_S$** Maximum Continuous Drain-Source Diode Forward Current -1.3 A
- **$V_{SD}$** Drain-Source Diode Forward Voltage $V_{GS} = 0$V, $I_S = -1.3$ A (Note 2) -0.77, -1.2 V

**Notes:**

1. $R_{JUC}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{JUC}$ is guaranteed by design while $R_{VCA}$ is determined by the user’s board design.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

Scale 1: 1 on letter size paper

- a) 78°C/W when mounted on a 1 in² pad of 2 oz copper
- b) 156°C/W when mounted on a minimum pad of 2 oz copper
Typical Characteristics

Figure 1. On-Region Characteristics

Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

Figure 3. Normalized On-Resistance vs Junction Temperature

Figure 4. On-Resistance vs Gate to Source Voltage

Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs Source Current
Typical Characteristics

Figure 7. Gate Charge Characteristics

Figure 8. Capacitance vs Drain to Source Voltage

Figure 9. Forward Bias Safe Operating Area

Figure 10. Single Pulse Maximum Power Dissipation

Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.
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