General Description
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Features
- Max $r_{DS(on)} = 13m\Omega$ at $V_{GS} = -10V, I_D = -11A$
- Max $r_{DS(on)} = 21.8m\Omega$ at $V_{GS} = -4.5V, I_D = -9A$
- Extended $V_{GS}$ range (-25V) for battery applications
- HBM ESD protection level of 5.4 KV typical (note 3)
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability
- RoHS Compliant

MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>Drain to Source Voltage</td>
<td>-30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate to Source Voltage</td>
<td>±25</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain Current -Continuous</td>
<td>(Note 1a)</td>
<td>-11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-Pulsed</td>
<td></td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power Dissipation for Single Operation</td>
<td>(Note 1a)</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Note 1b)</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Note 1c)</td>
<td>1.0</td>
</tr>
<tr>
<td>$T_J, T_{STG}$</td>
<td>Operating and Storage Temperature</td>
<td>-55 to 150</td>
<td>°C</td>
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Thermal Characteristics

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<td>$R_{JUA}$</td>
<td>Thermal Resistance, Junction to Ambient (Note 1a)</td>
<td>50</td>
<td>°C/W</td>
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<tr>
<td>$R_{JUC}$</td>
<td>Thermal Resistance, Junction to Case (Note 1)</td>
<td>25</td>
<td>°C/W</td>
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Package Marking and Ordering Information

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<tr>
<th>Device Marking</th>
<th>Device</th>
<th>Reel Size</th>
<th>Tape Width</th>
<th>Quantity</th>
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<tr>
<td>FDS6675BZ</td>
<td>FDS6675BZ</td>
<td>13”</td>
<td>12mm</td>
<td>2500 units</td>
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## Electrical Characteristics  \( T_J = 25°C \) unless otherwise noted

### Off Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>( B_{V_{DSS}} )</td>
<td>Drain to Source Breakdown Voltage</td>
<td>( I_D = -250 \mu A, V_{GS} = 0V )</td>
<td>0</td>
<td>-30</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( \Delta B_{V_{DSS}} )</td>
<td>Breakdown Voltage Temperature Coefficient</td>
<td>( I_D = -250 \mu A, ) referenced to 25°C</td>
<td>-20</td>
<td></td>
<td></td>
<td>mV/°C</td>
</tr>
<tr>
<td>( I_{DSS} )</td>
<td>Zero Gate Voltage Drain Current</td>
<td>( V_{DS} = -24V, V_{GS} = 0V )</td>
<td>-1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>( I_{GSS} )</td>
<td>Gate to Source Leakage Current</td>
<td>( V_{GS} = \pm 25V, V_{DS} = 0V )</td>
<td>±10</td>
<td></td>
<td></td>
<td>µA</td>
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### On Characteristics (Note 2)

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<tr>
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<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
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</thead>
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<tr>
<td>( V_{GS(th)} )</td>
<td>Gate to Source Threshold Voltage</td>
<td>( V_{DS}, I_D = -250 \mu A )</td>
<td>-1</td>
<td>-2</td>
<td>-3</td>
</tr>
<tr>
<td>( \Delta V_{GS(th)} )</td>
<td>Gate to Source Threshold Voltage Temperature Coefficient</td>
<td>( I_D = -250 \mu A, ) referenced to 25°C</td>
<td>15.7</td>
<td></td>
<td>16.5</td>
</tr>
<tr>
<td>( r_{DS(on)} )</td>
<td>Drain to Source On Resistance</td>
<td>( V_{GS} = -10V, I_D = -11A )</td>
<td>10.8</td>
<td>12.0</td>
<td></td>
</tr>
<tr>
<td>( V_{GS} )</td>
<td>Source to Drain Diode Forward Voltage</td>
<td>( V_{DS}, I_D = -11A )</td>
<td>17.4</td>
<td>18.8</td>
<td></td>
</tr>
<tr>
<td>( T_J )</td>
<td>Temperature</td>
<td></td>
<td>15.7</td>
<td></td>
<td>16.5</td>
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### Dynamic Characteristics

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<th>Max</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>( C_{iss} )</td>
<td>Input Capacitance</td>
<td>( V_{DS} = -15V, V_{GS} = 0V, f = 1MHz )</td>
<td>1855</td>
<td>2470</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( C_{oss} )</td>
<td>Output Capacitance</td>
<td>( f = 1MHz )</td>
<td>335</td>
<td>450</td>
<td></td>
<td>pF</td>
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<tr>
<td>( C_{rss} )</td>
<td>Reverse Transfer Capacitance</td>
<td>( f = 1MHz )</td>
<td>330</td>
<td>500</td>
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<td>pF</td>
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### Switching Characteristics (Note 2)

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<th>Typ</th>
<th>Max</th>
<th>Units</th>
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</thead>
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<tr>
<td>( t_{d(on)} )</td>
<td>Turn-On Delay Time</td>
<td>( V_{DD} = -15V, I_D = -11A )</td>
<td>3.0</td>
<td>10</td>
<td></td>
<td>ns</td>
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<tr>
<td>( t_{r} )</td>
<td>Rise Time</td>
<td>( V_{GS} = -10V, R_{GS} = 6\Omega )</td>
<td>7.8</td>
<td>16</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{d(off)} )</td>
<td>Turn-Off Delay Time</td>
<td>( V_{DS} = -15V, I_D = -11A )</td>
<td>12.0</td>
<td>200</td>
<td></td>
<td>ns</td>
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<tr>
<td>( t_{f} )</td>
<td>Fall Time</td>
<td>( V_{GS} = -10V, I_D = -11A )</td>
<td>60</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( Q_g )</td>
<td>Total Gate Charge</td>
<td></td>
<td>44</td>
<td>62</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( Q_g )</td>
<td>Total Gate Charge</td>
<td></td>
<td>25</td>
<td>35</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( Q_{gs} )</td>
<td>Gate to Source Gate Charge</td>
<td></td>
<td>7.2</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( Q_{gd} )</td>
<td>Gate to Drain Charge</td>
<td></td>
<td>11.4</td>
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<td></td>
<td>nC</td>
</tr>
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</table>

### Drain-Source Diode Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{SD} )</td>
<td>Source to Drain Diode Forward Voltage</td>
<td>( V_{GS} = 0V, I_S = -2.1A )</td>
<td>-0.7</td>
<td>-1.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( t_r )</td>
<td>Reverse Recovery Time</td>
<td>( I_T = -11A, di/dt = 100A/µs )</td>
<td>42</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{rr} )</td>
<td>Reverse Recovery Time</td>
<td>( I_T = -11A, di/dt = 100A/µs )</td>
<td>30</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
</tbody>
</table>

### Notes:

1. \( R_{th JA} \) is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. \( R_{th JC} \) is guaranteed by design while \( R_{th CA} \) is determined by the user’s board design.

2. Pulse Test: Pulse Width <300 µs, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
Typical Characteristics  \( T_J = 25^\circ C \) unless otherwise noted

Figure 1. On Region Characteristics

Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

Figure 3. Normalized On Resistance vs Junction Temperature

Figure 4. On-Resistance vs Gate to Source Voltage

Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs Source Current
### Typical Characteristics

$T_J = 25^\circ C$ unless otherwise noted

![Figure 7. Gate Charge Characteristics](image)

![Figure 8. Capacitance vs Drain to Source Voltage](image)

![Figure 9. $I_g$ vs $V_{GS}$](image)

![Figure 10. Unclamped Inductive Switching Capability](image)

![Figure 11. Maximum Continuous Drain Current vs Ambient Temperature](image)

![Figure 12. Forward Bias Safe Operating Area](image)
Typical Characteristics $T_J = 25^\circ C$ unless otherwise noted

Figure 13. Single Pulse Maximum Power Dissipation

Figure 14. Junction-to-Ambient Transient Thermal Response Curve
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