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# FDS8962C

## Dual N & P-Channel PowerTrench® MOSFET

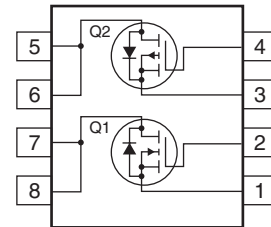
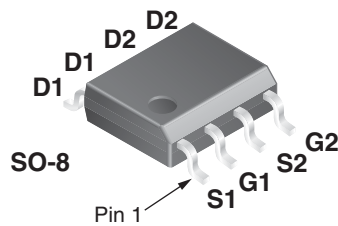
### Features

- **Q1:** N-Channel  
7.0A, 30V  $R_{DS(on)} = 0.030\Omega$  @  $V_{GS} = 10V$   
 $R_{DS(on)} = 0.044\Omega$  @  $V_{GS} = 4.5V$
- **Q2:** P-Channel  
-5A, -30V  $R_{DS(on)} = 0.052\Omega$  @  $V_{GS} = -10V$   
 $R_{DS(on)} = 0.080\Omega$  @  $V_{GS} = -4.5V$
- Fast switching speed
- High power and handling capability in a widely used surface mount package

### General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DSS}$	Drain-Source Voltage	30	-30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a)	7	-5	A
	– Pulsed	20	-20	
$P_D$	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$
<b>Thermal Characteristics</b>				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78		$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40		$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS8962C	FDS8962C	13"	12mm	2500 units

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Off Characteristics</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	Q1 Q2	30 -30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$ $I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	Q1 Q2		25 -23		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2			1 -1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	All			100	nA
$I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	All			-100	nA
<b>On Characteristics (Note 2)</b>							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	Q1 Q2	1 -1	1.9 -1.7	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$ $I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	Q1 Q2		-4.5 4.5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 7\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 7\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 6\text{ A}$	Q1		21 29 26	30 46 44	m $\Omega$
		$V_{GS} = -10\text{ V}, I_D = -5\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -5\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = -4.5\text{ V}, I_D = -4\text{ A}$	Q2		42 57 65	52 78 80	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	Q1 Q2	20 -20			A
		$V_{GS} = 10\text{ V}, I_D = 7\text{ A}$ $V_{GS} = -5\text{ V}, I_D = -5\text{ A}$	Q1 Q2		25 10		S
<b>Dynamic Characteristics</b>							
$C_{iss}$	Input Capacitance	Q1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	Q1		575		pF
			Q2		528		
$C_{oss}$	Output Capacitance	Q2 $V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	Q1		145		pF
			Q2		132		
$C_{rss}$	Reverse Transfer Capacitance	Q1 $V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	Q1		65		pF
			Q2		70		
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$	Q1		2.1		$\Omega$
			Q2		6.0		
<b>Switching Characteristics (Note 2)</b>							
$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$	Q1		8	16	ns
			Q2		7	14	
$t_r$	Turn-On Rise Time	Q2 $V_{DD} = -15\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$	Q1		5	10	ns
			Q2		13	24	
$t_{d(off)}$	Turn-Off Delay Time	Q1 $V_{DD} = -15\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$	Q1		23	37	ns
			Q2		14	25	
$t_f$	Turn-Off Fall Time	Q1 $V_{DD} = -15\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$	Q1		3	6	ns
			Q2		9	17	
$Q_g$	Total Gate Charge	Q1 $V_{DS} = 15\text{ V}, I_D = 7\text{ A}, V_{GS} = 10\text{ V}$	Q1		10.7	26	nC
			Q2		9.6	13	
$Q_{gs}$	Gate-Source Charge	Q2 $V_{DS} = -15\text{ V}, I_D = -5\text{ A}, V_{GS} = -10\text{ V}$	Q1		1.7		nC
			Q2		2.2		
$Q_{gd}$	Gate-Drain Charge	Q1 $V_{DS} = -15\text{ V}, I_D = -5\text{ A}, V_{GS} = -10\text{ V}$	Q1		2.1		nC
			Q2		1.7		

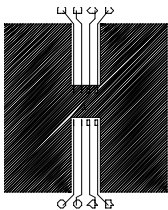
**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted **(Continued)**

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>							
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			1.3 -1.3	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)	Q1 Q2		0.75 -0.88	1.2 -1.2	V
$t_{rr}$	Diode Reverse Recovery Time	Q1 $I_F = 7\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$ Q2	Q1 Q2		19 19		nS
$Q_{rr}$	Diode Reverse Recovery Charge	Q1 $I_F = -5\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$ Q2	Q1 Q2		9 6		nC

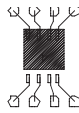
**Notes:**

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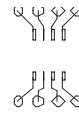
- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $78^\circ\text{W}$  when mounted on a  $0.5\text{ in}^2$  pad of 2 oz copper



b)  $125^\circ\text{W}$  when mounted on a  $.02\text{ in}^2$  pad of 2 oz copper

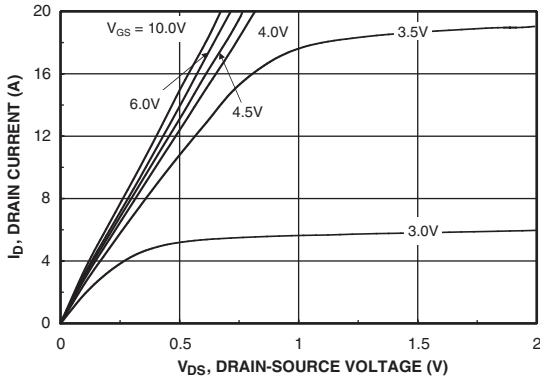


c)  $135^\circ\text{W}$  when mounted on a minimum pad.

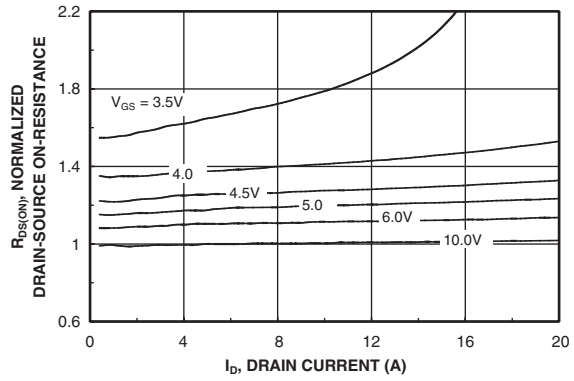
Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty Cycle < 2.0%

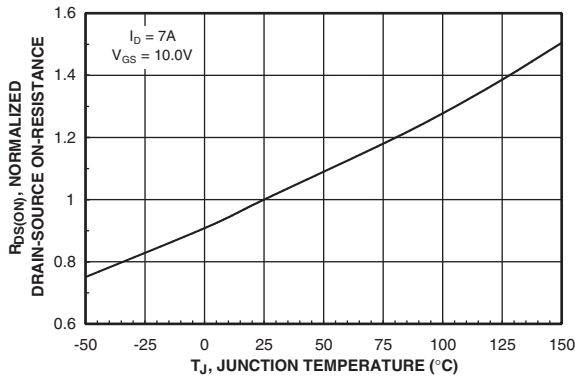
### Typical Characteristics: Q1 (N-Channel)



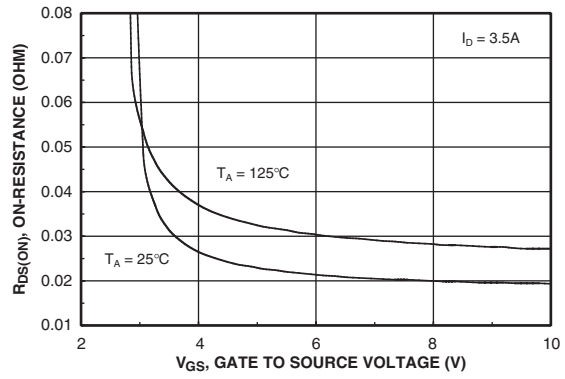
**Figure 1. On-Region Characteristics.**



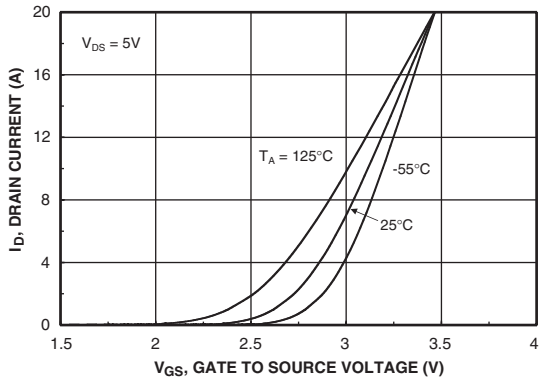
**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**



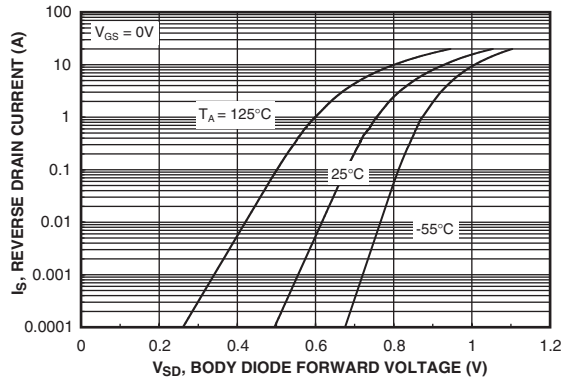
**Figure 3. On-Resistance Variation with Temperature.**



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**



**Figure 5. Transfer Characteristics.**



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

### Typical Characteristics: Q1 (N-Channel)

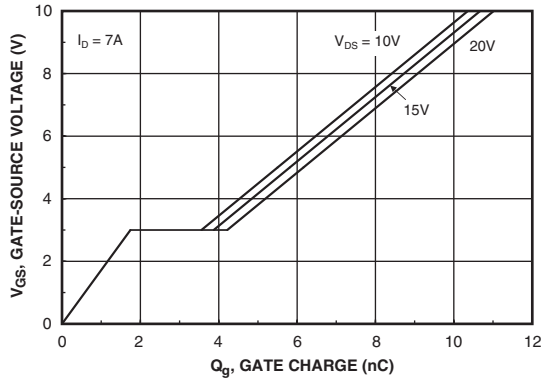


Figure 7. Gate Charge Characteristics.

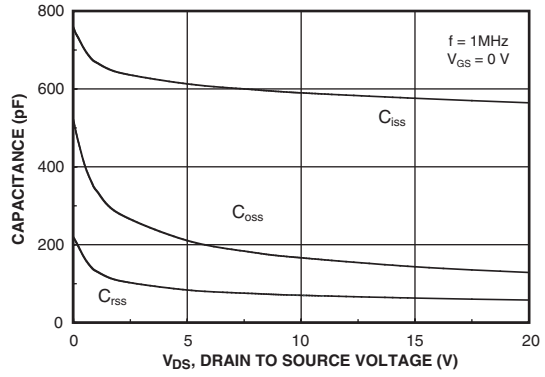


Figure 8. Capacitance Characteristics.

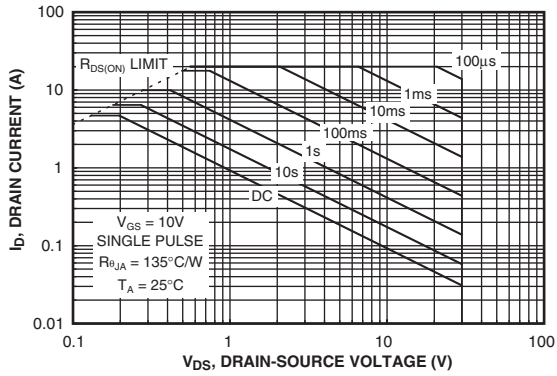


Figure 9. Maximum Safe Operating Area.

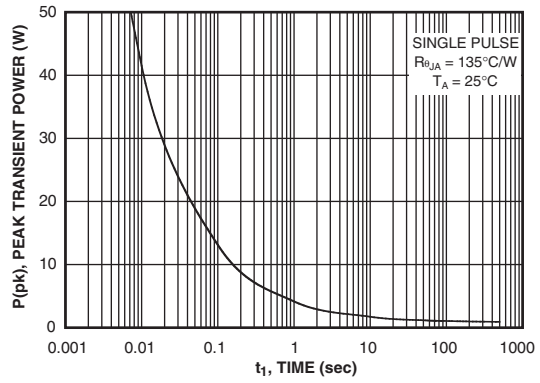


Figure 10. Single Pulse Maximum Power Dissipation.

### Typical Characteristics: Q2 (P-Channel)

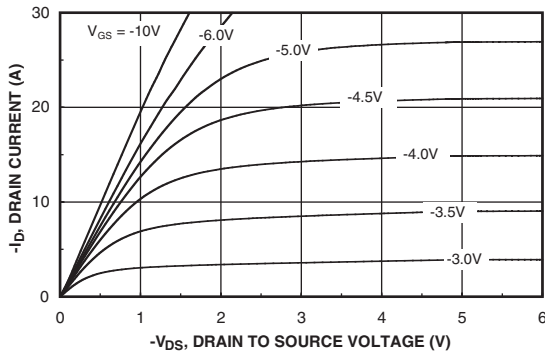


Figure 11. On-Region Characteristics.

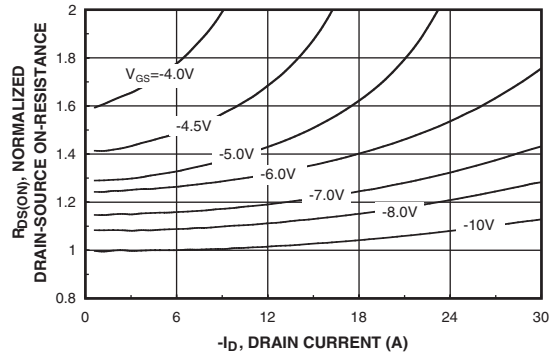


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

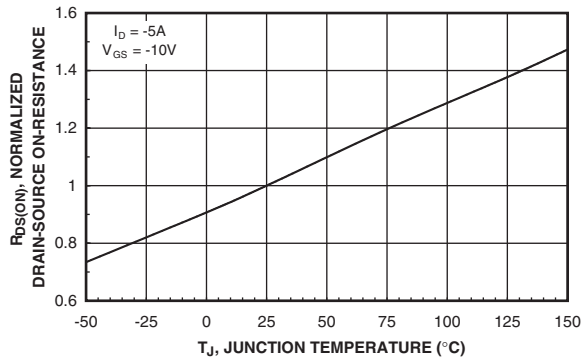


Figure 13. On-Resistance Variation with Temperature.

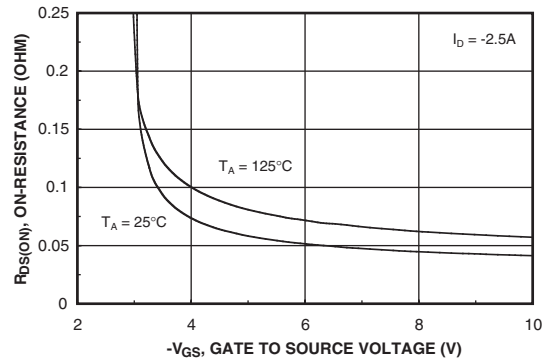


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

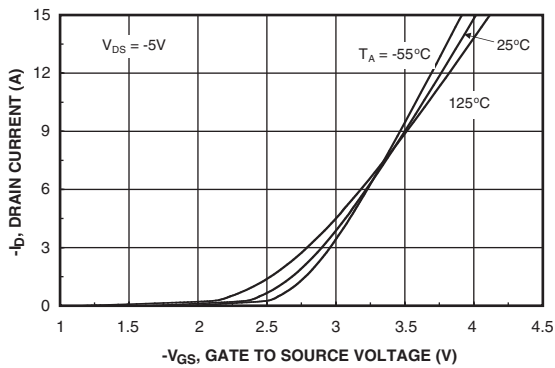


Figure 15. Transfer Characteristics.

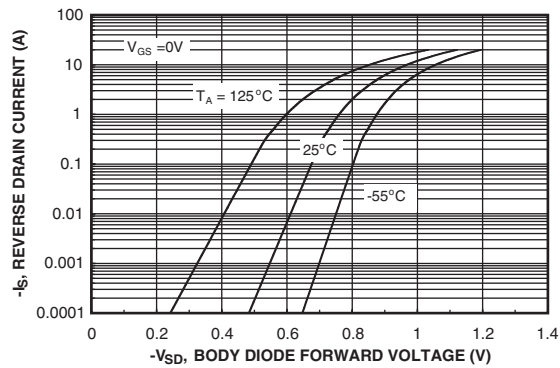


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Characteristics: Q2 (P-Channel)

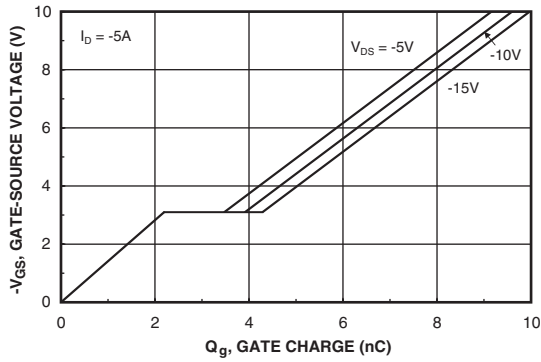


Figure 17. Gate Charge Characteristics.

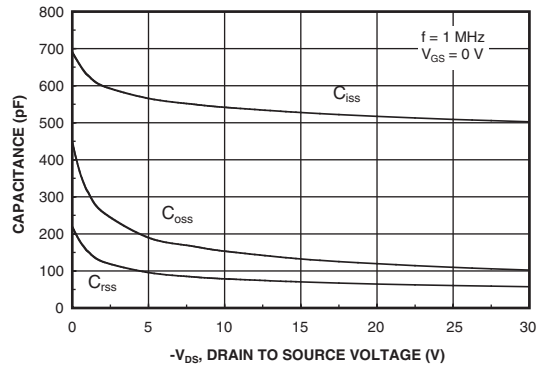


Figure 18. Capacitance Characteristics.

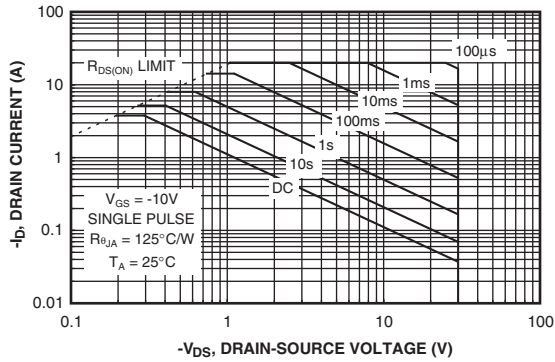


Figure 19. Maximum Safe Operating Area.

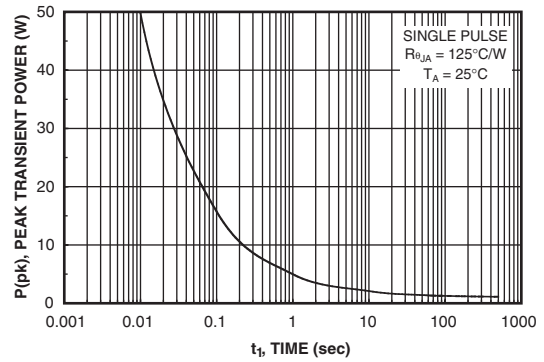


Figure 20. Single Pulse Maximum Power Dissipation.

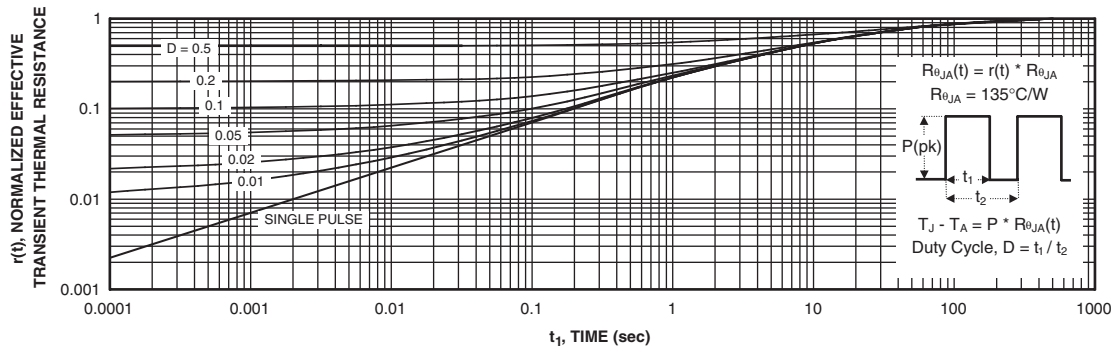


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



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