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# NC7SZ57 / NC7SZ58

## TinyLogic® UHS Universal Configurable Two-Input Logic Gates

### Features

- Ultra High Speed
- Capable of Implementing any Two-Input Logic Functions
- Typical Usage Replaces Two (2) TinyLogic® Gate Devices
- Reduces Part Counts in Inventory
- Broad  $V_{CC}$  Operating Range: 1.65V to 5.5V
- Power Down High Impedance Input/Output
- Over-Voltage Tolerant Inputs Facilitate 5V to 3V Translation
- Proprietary Noise/EMI Reduction Circuitry Implemented

### Description

The NC7SZ57 and NC7SZ58 are universal configurable two-input logic gates. Each device is capable of being configured for 1 of 5 unique two-input logic functions. Any possible two-input combinatorial logic function can be implemented, as shown in the *Function Selection Table*. Device functionality is selected by how the device is wired at the board level. *Figures 4 through 13* illustrate how to connect the NC7SZ57 and NC7SZ58, respectively, for the desired logic function. All inputs have been implemented with hysteresis.

The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad  $V_{CC}$  operating range. The device is specified to operate over the 1.65V to 5.5V  $V_{CC}$  operating range. The input and output are high impedance when  $V_{CC}$  is 0V. Inputs tolerate voltages up to 5.5V independent of  $V_{CC}$  operating range.

### Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SZ57P6X	Z57	6-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SZ57L6X	KK	6-Lead Micropak™, 1.0mm Wide	5000 Units on Tape & Reel
NC7SZ57FHX	KK	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	
NC7SZ58P6X	Z58	6-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SZ58L6X	LL	6-Lead Micropak™, 1.0mm Wide	5000 Units on Tape & Reel
NC7SZ58FHX	LL	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	

### Pin Configurations

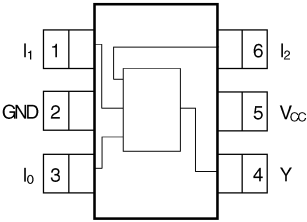


Figure 1. SC70 (Top View)

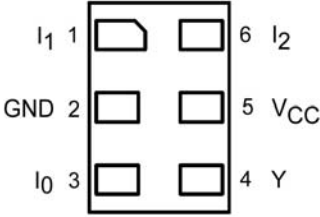


Figure 2. MicroPak™ (Top Through View)

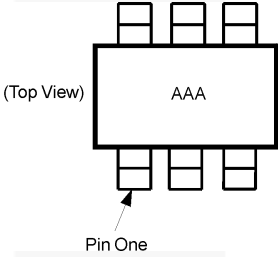


Figure 3. Pin 1 Orientation

**Notes:**

1. AAA represents product code top mark (see *Ordering Information*).
2. Orientation of top mark determines pin one location.
3. Reading the top mark left to right, pin one is the lower left pin.

### Pin Definitions

Pin # SC70	Pin # MicroPak™	Name	Description
1	1	I <sub>1</sub>	Data Input
2	2	GND	Ground
3	3	I <sub>0</sub>	Data Input
4	4	Y	Output
5	5	V <sub>CC</sub>	Supply Voltage
6	6	I <sub>2</sub>	Data Input

### Function Table

Inputs			NC7SZ57	NC7SZ58
I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	$Y = \overline{(I_0)} \cdot \overline{(I_2)} + (I_1) \cdot (I_2)$	$Y = (I_0) \cdot \overline{(I_2)} + \overline{(I_1)} \cdot (I_2)$
L	L	L	H	L
L	L	H	L	H
L	H	L	H	L
L	H	H	L	H
H	L	L	L	H
H	L	H	L	H
H	H	L	H	L
H	H	H	H	L

H = HIGH Logic Level

L = LOW Logic Level

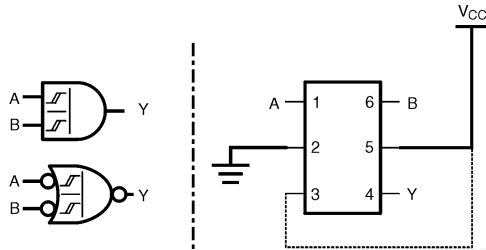
### Function Selection Table

2-Input Logic Function	Device Selection	Connection Configuration
2-Input AND	NC7SZ57	Figure 4
2-Input AND with Inverted Input	NC7SZ58	Figure 10, Figure 11
2-Input AND with Both Inputs Inverted	NC7SZ57	Figure 7
2-Input NAND	NC7SZ58	Figure 9
2-Input NAND with Inverted Input	NC7SZ57	Figure 5, Figure 6
2-Input NAND with Both Inputs Inverted	NC7SZ58	Figure 12
2-Input OR	NC7SZ58	Figure 12
2-Input OR with Inverted Input	NC7SZ57	Figure 5, Figure 6
2-Input OR with Both Inputs Inverted	NC7SZ58	Figure 9
2-Input NOR	NC7SZ57	Figure 7
2-Input NOR with Inverted Input	NC7SZ58	Figure 9, Figure 10
2-Input NOR with Both Inputs Inverted	NC7SZ57	Figure 4
2-Input XOR	NC7SZ58	Figure 13
2-Input XNOR	NC7SZ57	Figure 8

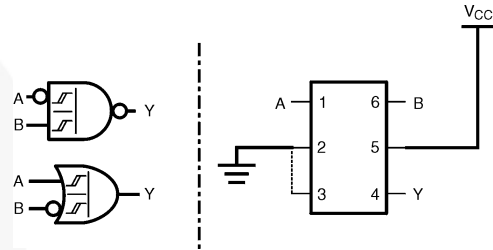
## NC7SZ57 Logic Configurations

Figure 4 through Figure 8 show the logical functions that can be implemented using the NC7SZ57. The diagrams show the DeMorgan's equivalent logic duals for a given

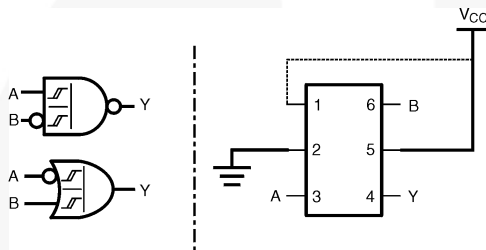
two-input function. The logical implementation is next to the board-level physical implementation of how the pins of the function should be connected.



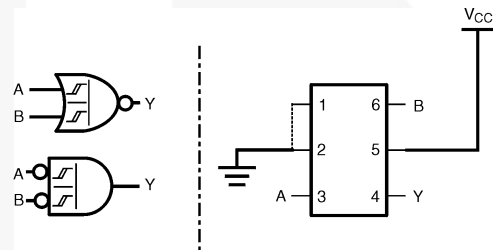
**Figure 4. 2-Input AND Gate**



**Figure 5. 2-Input NAND with Inverted A Input**



**Figure 6. 2-Input NAND with Inverted B Input**



**Figure 7. 2-Input NOR Gate**



**Figure 8. 2-Input XNOR Gate**

## NC7SZ58 Logic Configurations

Figure 9 through Figure 13 show the logical functions that can be implemented using the NC7SZ58. The diagrams show the DeMorgan's equivalent logic duals for a given two-input function. The logical

implementation is next to the board-level physical implementation of how the pins of the function should be connected.



Figure 9. 2-Input NAND Gate

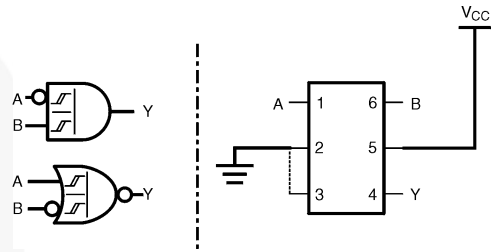


Figure 10. 2-Input AND with Inverted A Input

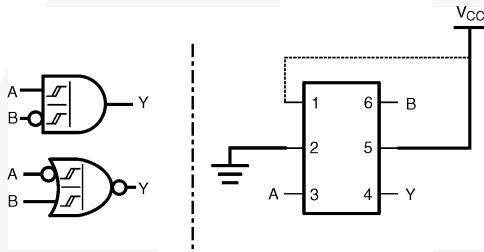


Figure 11. 2-Input AND with Inverted B Input

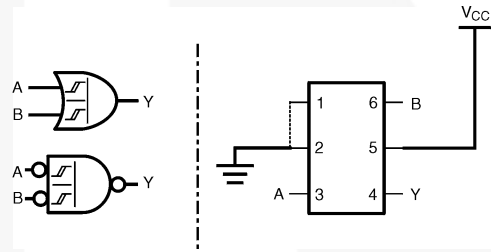


Figure 12. 2-Input OR Gate

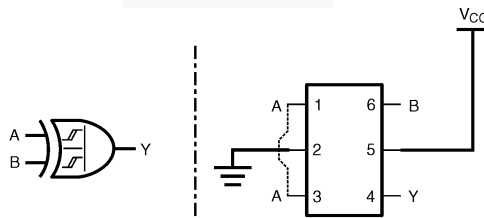


Figure 13. 2-Input XOR Gate

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
$V_{CC}$	Supply Voltage		-0.5	7.0	V
$V_{IN}$	DC Input Voltage		-0.5	7.0	V
$V_{OUT}$	DC Output Voltage		-0.5	7.0	V
$I_{IK}$	DC Input Diode Current	$V_{IN} < 0.5V$		-50	mA
$I_{OK}$	DC Output Diode Current	$V_{OUT} < -0.5V$		-50	mA
$I_{OUT}$	DC Output Source / Sink Current			$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current			$\pm 50$	mA
$T_{STG}$	Storage Temperature Range		-65	+150	°C
$T_J$	Maximum Junction Temperature under Bias			+150	°C
$T_L$	Lead Temperature, Soldering 10 Seconds			+260	°C
$P_D$	Power Dissipation at +85°C	MicroPak™-6		130	mW
		SC70-6		180	
		MicroPak2™-6		120	
ESD	Human Body Model, JEDEC:JESD22-A114			4000	V
	Charged Device Model, JEDEC:JESD22-C101			2000	

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Units
$V_{CC}$	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.5	5.5	
$V_{IN}$	Input Voltage		0	5.5	V
$V_{OUT}$	Output Voltage		0	$V_{CC}$	V
$T_A$	Operating Temperature		-40	+85	°C
$\theta_{JA}$	Thermal Resistance	SC70-6		350	°C/W
		MicroPak™-6		500	
		MicroPak2™-6		560	

### DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	T <sub>A</sub> =+25°C			T <sub>A</sub> =-40 to +85°C		Units	
				Min.	Typ.	Max.	Min.	Max.		
V <sub>P</sub>	Positive Threshold Voltage	1.65		0.60	0.99	1.40	0.60	1.40	V	
		2.30		1.00	1.39	1.80	1.00	1.80		
		3.00		1.30	1.77	2.20	1.30	2.20		
		4.50		1.90	2.49	3.10	1.90	3.10		
		5.50		2.20	2.95	3.60	2.20	3.60		
V <sub>N</sub>	Negative Threshold Voltage	1.65		0.20	0.50	0.90	0.20	0.90	V	
		2.30		0.40	0.75	1.15	0.40	1.15		
		3.00		0.60	0.99	1.50	0.60	1.50		
		4.50		1.00	1.43	2.00	1.00	2.00		
		5.50		1.20	1.70	2.30	1.20	2.30		
V <sub>H</sub>	Hysteresis Voltage	1.65		0.15	0.48	0.90	0.15	0.90	V	
		2.30		0.25	0.64	1.10	0.25	1.10		
		3.00		0.40	0.78	1.20	0.40	1.20		
		4.50		0.60	1.06	1.50	0.60	1.50		
		5.50		0.70	1.25	1.70	0.70	1.70		
V <sub>OH</sub>	HIGH Level Output Voltage	1.65	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -100μA	1.55	1.65		1.55		V	
		2.30		2.20	2.30		2.20			
		3.00		2.90	3.00		2.90			
		4.50		4.40	4.50		4.40			
		1.65	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -4mA	1.29	1.52		1.29		
		2.30		I <sub>OH</sub> = -8mA	1.90	2.15		1.90		
		3.00		I <sub>OH</sub> = -16mA	2.40	2.80		2.40		
		3.00		I <sub>OH</sub> = -24mA	2.30	2.68		2.30		
		4.50		I <sub>OH</sub> = -32mA	3.80	4.20		3.80		

Continued on the following page...



### DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub>	Conditions	T <sub>A</sub> =+25°C			T <sub>A</sub> =-40 to +85°C		Units	
				Min.	Typ.	Max.	Min.	Max.		
V <sub>OL</sub>	LOW Level Output Voltage	1.65	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> =100μA			0.10		0.10	V	
		2.30				0.10		0.10		
		3.00				0.10		0.10		
		4.50				0.10		0.10		
		1.65	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> =4mA		0.08	0.24			0.24
		2.30		I <sub>OL</sub> =8mA		0.10	0.30			0.30
		3.00		I <sub>OL</sub> =16mA		0.15	0.40			0.40
		3.00		I <sub>OL</sub> =24mA		0.22	0.55			0.55
4.50		I <sub>OL</sub> =32mA		0.22	0.55		0.55			
I <sub>IN</sub>	Input Leakage Current	0 to 5.50	V <sub>IN</sub> = 5.5V, GND			±0.1		±1.0	μA	
I <sub>OFF</sub>	Power Off Leakage Current	0	V <sub>IN</sub> or V <sub>OUT</sub> = 5.5V			1		10	μA	
I <sub>CC</sub>	Quiescent Supply Current	1.65 to 5.5	V <sub>IN</sub> = 5.5V, GND			1		10	μA	

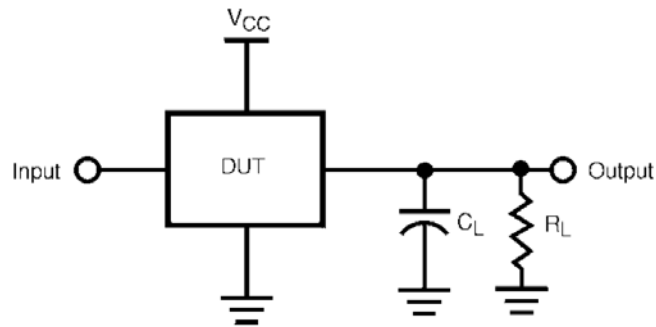
### AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	T <sub>A</sub> =25°C			T <sub>A</sub> =-40 to 85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to Y	1.8 ± 0.15	C <sub>L</sub> =15pF, R <sub>L</sub> =1MΩ	3.0	8.0	14.0	3.0	14.5	ns	Figure 14 Figure 16
		2.5 ± 0.2		1.5	4.9	8.0	1.5	8.5		
		3.3 ± 0.3		1.2	3.7	5.3	1.2	5.7		
		5.0 ± 0.5		0.8	2.8	4.3	0.8	4.6		
		3.3 ± 0.3	C <sub>L</sub> =50pF, R <sub>L</sub> =500Ω	1.5	4.2	6.0	1.5	6.5		
		5.0 ± 0.5		1.0	3.4	4.9	1.0	5.3		
C <sub>IN</sub>	Input Capacitance	0			2				pF	
C <sub>PD</sub>	Power Dissipation Capacitance	3.3	Note 4		14				pF	Figure 15
		5.0			17					

**Note:**

- C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. (See Figure 12) C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression: I<sub>CCD</sub> = (C<sub>PD</sub>)(V<sub>CC</sub>)(f<sub>in</sub>) + (I<sub>CCstatic</sub>).

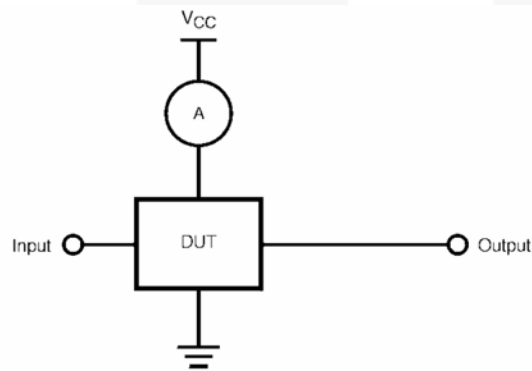
## AC Loadings and Waveforms



**Note:**

- 5.  $C_L$  includes load and stray capacitance.
- 6. Input PRR = 1.0MHz,  $t_w$  = 500ns.

**Figure 14. AC Test Circuit**



**Note:**

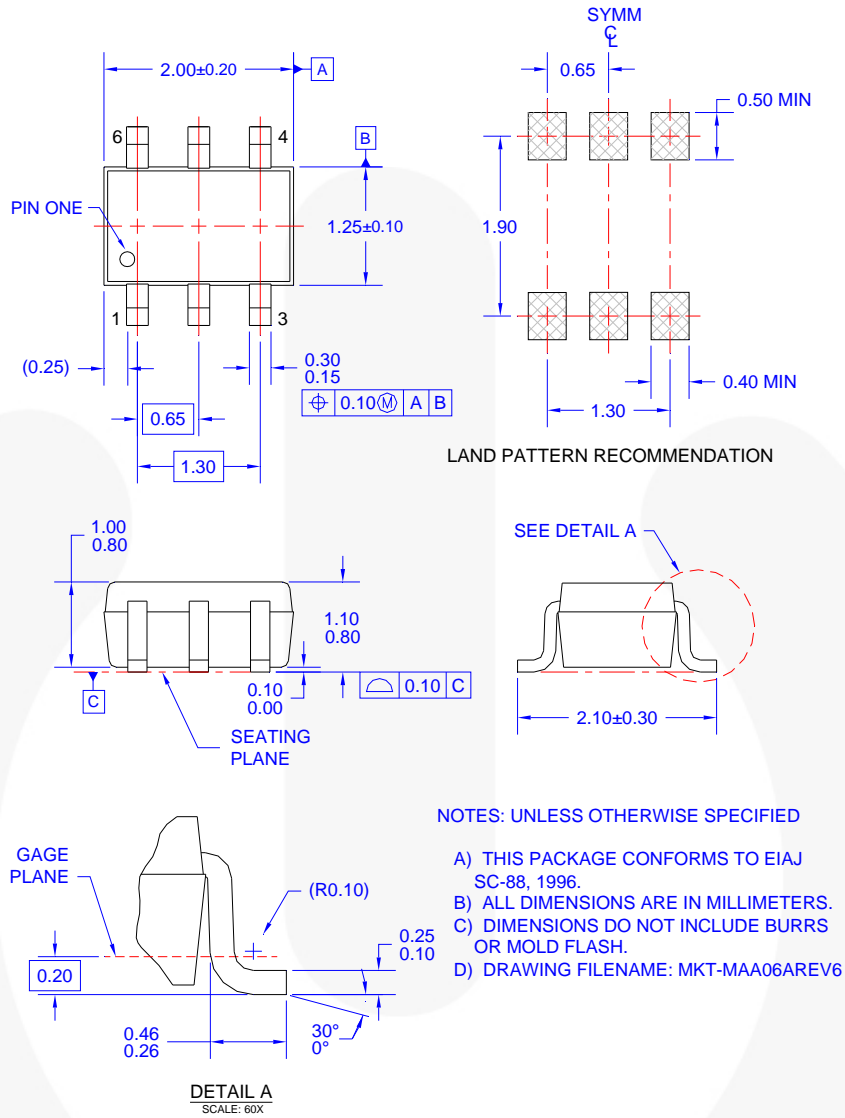
- 7. Input = AC waveforms.
- 8. PRR = Variable; Duty Cycle = 50%.

**Figure 15.  $I_{CCD}$  Test Circuit**



**Figure 16. AC Waveforms**

## Physical Dimensions



**Figure 17. 6-Lead, SC70, EIAJ SC-88a, 1.25mm Wide**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

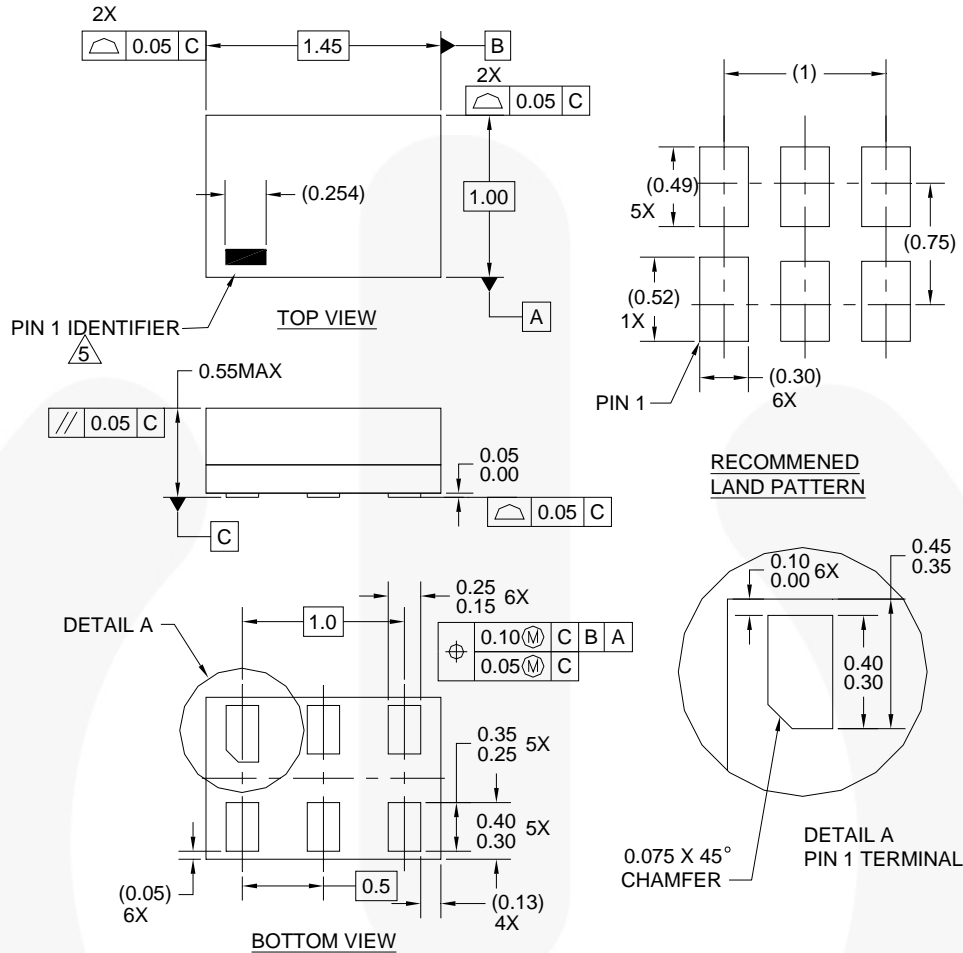
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
<http://www.fairchildsemi.com/packaging/>.

## Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:  
[http://www.fairchildsemi.com/products/analog/pdf/sc70-6\\_tr.pdf](http://www.fairchildsemi.com/products/analog/pdf/sc70-6_tr.pdf)

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
P6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

## Physical Dimensions



**Notes:**

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

**Figure 18. 6-Lead, MicroPak™, 1.0mm Wide**

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[http://www.fairchildsemi.com/products/logic/pdf/micropak\\_tr.pdf](http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf)

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

## Physical Dimensions



**Figure 19. 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch**

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[http://www.fairchildsemi.com/packaging/MicroPAK2\\_6L\\_tr.pdf](http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf)

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



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- |   |  |   |   |
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| AccuPower™  | F-PFS™   | Power-SPM™  | <b>the power franchise</b>  |
| Auto-SPM™   | FRFET®   | PowerTrench®  | TinyBoost™  |
| AX-CAPT™  | Global Power Resource™                         | PowerXST™   | TinyBuck™   |
| BitSic®   | Green FPST™                                    | Programmable Active Droop™  | TinyCalc™   |
| Build it Now™   | Green FPST™ e-Series™                          | QFET®   | TinyLogic®  |
| CorePLUS™   | Gmax™  | QST™  | TINYOPTO™   |
| CorePOWER™  | GTO™   | Quiet Series™   | TinyPower™  |
| CROSSVOL™   | IntelliMAX™                                    | RapidConfigure™   | TinyPWM™  |
| CTL™  | ISOPLANAR™                                     |  ™               | TinyWire™   |
| Current Transfer Logic™   | Making Small Speakers Sound Louder and Better™ | Saving our world, 1mW/W/kW at a time™   | TranSiC®  |
| DEUXPEED®   | MegaBuck™                                      | SignalWise™   | TriFault Detect™  |
| Dual Cool™  | MICROCOUPLER™                                  | SmartMax™   | TRUECURRENT®  |
| EcoSPARK®   | MicroFET™                                      | SMART START™  | µSerDes™  |
| EfficientMax™   | MicroPak™                                      | SPM®  |  ™ |
| ESBC™   | MicroPak2™                                     | STEALTH™  | UHC®  |
|  ™ | MillerDrive™                                   | SuperFET®   | Ultra FRFET™  |
| Fairchild®  | MotionMax™                                     | SuperSOT™-3   | UniFET™   |
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