**N-Channel Logic Level Power MOSFET**

100 V, 12 A, 200 mΩ

These are N-Channel enhancement mode silicon gate power field effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V to 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

Formerly developmental type TA09526.

**Features**

- 12A, 100V
- \( r_{DS(ON)} = 0.200 \Omega \)
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

**Ordering Information**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BRAND</th>
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<tbody>
<tr>
<td>RFP12N10L</td>
<td>TO-220AB</td>
<td>F12N10L</td>
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**Symbol**

![Symbol Diagram]

**Packaging**

JEDEC TO-220AB

![Packaging Diagram]
## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to Source Voltage (Note 1)</td>
<td>( V_{DS} )</td>
<td>( I_D = 250 \mu A, V_{GS} = 0 ) V</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Drain to Gate Voltage ((R_{GS} = 1M \Omega)) (Note 1)</td>
<td>( V_{DGR} )</td>
<td>( V_{GS} = V_{DS}, I_D = 250 \mu A ) (Figure 7)</td>
<td>1</td>
<td>2</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Continuous Drain Current</td>
<td>( I_D )</td>
<td>( V_{DS} = 80 ) V</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Pulsed Drain Current (Note 3)</td>
<td>( I_{DM} )</td>
<td>( V_{GS} = 0 ) V</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate to Source Voltage</td>
<td>( V_{GS} )</td>
<td>( V_{GS} = 10 ) V, ( V_{DS} = 0 ) V</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>Maximum Power Dissipation</td>
<td>( P_D )</td>
<td>( I_D = 12 ) A, ( V_{DD} = 5 ) V (Figures 5, 6)</td>
<td>-</td>
<td>-</td>
<td>0.200</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Maximum Temperature for Soldering</td>
<td>( T_L )</td>
<td>( V_{GS} = 0 ) V, ( V_{DS} = 25 ) V, ( f = 1 ) MHz (Figure 8)</td>
<td>-</td>
<td>-</td>
<td>900</td>
<td>( \mu F )</td>
</tr>
<tr>
<td>Operating and Storage Temperature</td>
<td>( T_{J, T_{STG}} )</td>
<td>( V_{GS} = 5 ) V, ( V_{DD} = 6.25 ) V, ( R_G = 6.25 ) ( \Omega ) (Figures 9, 10, 11)</td>
<td>-</td>
<td>50</td>
<td>150</td>
<td>ns</td>
</tr>
</tbody>
</table>

**CAUTION:** Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**
1. \( T_J = 25 \)°C to 125°C.

## Electrical Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to Source Breakdown Voltage</td>
<td>( BV_{DSS} )</td>
<td>( I_D = 250 \mu A, V_{GS} = 0 ) V</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Gate to Threshold Voltage</td>
<td>( V_{GS(TH)} )</td>
<td>( V_{GS} = V_{DS}, I_D = 250 \mu A ) (Figure 7)</td>
<td>1</td>
<td>2</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>( I_{DSS} )</td>
<td>( V_{DS} = 80 ) V, ( V_{GS} = 0 ) V</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Gate to Source Leakage Current</td>
<td>( I_{GSS} )</td>
<td>( V_{GS} = 10 ) V, ( V_{DS} = 0 ) V</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Drain to Source On Resistance (Note 2)</td>
<td>( r_{DS(ON)} )</td>
<td>( I_D = 12 ) A, ( V_{GS} = 5 ) V (Figures 5, 6)</td>
<td>-</td>
<td>-</td>
<td>0.200</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>( C_{ISS} )</td>
<td>( V_{GS} = 0 ) V, ( V_{DS} = 25 ) V, ( f = 1 ) MHz (Figure 8)</td>
<td>-</td>
<td>-</td>
<td>900</td>
<td>( \mu F )</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>( C_{OSS} )</td>
<td>( V_{GS} = 5 ) V, ( V_{DD} = 6.25 ) V, ( R_G = 6.25 ) ( \Omega ) (Figures 9, 10, 11)</td>
<td>-</td>
<td>-</td>
<td>325</td>
<td>( \mu F )</td>
</tr>
<tr>
<td>Reverse-Transfer Capacitance</td>
<td>( C_{RSS} )</td>
<td>( V_{GS} = 0 ) V, ( V_{DS} = 25 ) V, ( f = 1 ) MHz (Figure 8)</td>
<td>-</td>
<td>-</td>
<td>170</td>
<td>( \mu F )</td>
</tr>
<tr>
<td>Turn-On Delay Time</td>
<td>( t_{d(ON)} )</td>
<td>( I_D = 6 ) A, ( V_{DD} = 50 ) V, ( R_G = 6.25 ) ( \Omega ) (Figures 9, 10, 11)</td>
<td>-</td>
<td>15</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>Rise Time</td>
<td>( t_r )</td>
<td>( V_{GS} = 5 ) V (Figures 9, 10, 11)</td>
<td>-</td>
<td>70</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>Turn-Off Delay Time</td>
<td>( t_{d(OFF)} )</td>
<td>( I_D = 4 ) A, ( dI_D/dt = 50 ) ( \mu A/\mu s ) (Figures 9, 10, 11)</td>
<td>-</td>
<td>100</td>
<td>130</td>
<td>ns</td>
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<tr>
<td>Fall Time</td>
<td>( t_f )</td>
<td>( I_D = 4 ) A, ( dI_D/dt = 50 ) ( \mu A/\mu s ) (Figures 9, 10, 11)</td>
<td>-</td>
<td>80</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>Thermal Resistance Junction to Case</td>
<td>( R_{\theta JC} )</td>
<td>( V_{GS} = 0 ) V, ( V_{DS} = 25 ) V, ( f = 1 ) MHz (Figure 8)</td>
<td>-</td>
<td>-</td>
<td>2.083</td>
<td>°C/W</td>
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## Source to Drain Diode Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source to Drain Diode Voltage (Note 2)</td>
<td>( V_{SD} )</td>
<td>( I_{SD} = 6 ) A</td>
<td>-</td>
<td>-</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>Diode Reverse Recovery Time</td>
<td>( t_{rr} )</td>
<td>( I_{SD} = 4 ) A, ( dI_{SD}/dt = 50 ) ( \mu A/\mu s )</td>
<td>-</td>
<td>150</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTES:**
2. Pulsed: pulse duration = 80\( \mu \)s max, duty cycle = 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.
Typical Performance Curves  Unless Otherwise Specified

**FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE**

![Normalized Power Dissipation vs Case Temperature](image1)

**FIGURE 2. FORWARD BIAS OPERATING AREA**

![Forward Bias Operating Area](image2)

**FIGURE 3. SATURATION CHARACTERISTICS**

![Saturation Characteristics](image3)

**FIGURE 4. TRANSFER CHARACTERISTICS**

![Transfer Characteristics](image4)

**FIGURE 5. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT**

![Drain to Source On Resistance vs Drain Current](image5)

**FIGURE 6. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE**

![Normalized Drain to Source On Resistance vs Junction Temperature](image6)
Typical Performance Curves  Unless Otherwise Specified  (Continued)

![Graph 7: Normalized Gate Threshold Voltage vs Junction Temperature](image1)

![Graph 8: Capacitance vs Drain to Source Voltage](image2)

![Graph 9: Normalized Switching Waveforms for Constant Gate Current](image3)

Test Circuits and Waveforms

![Test Circuit and Waveforms](image4)

1. Switching Time Test Circuit
2. Resistive Switching Waveforms
Test Circuits and Waveforms (Continued)

**FIGURE 12. GATE CHARGE TEST CIRCUIT**

**FIGURE 13. GATE CHARGE WAVEFORMS**
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<th>Product Status</th>
<th>Definition</th>
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<tr>
<td>Advance Information</td>
<td>Formative / In Design</td>
<td>Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
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Rev. 166