Reference Design RD-356

1. **Fairchild Motion SPM® 7 Series**

This reference design supports design of Fairchild’s Motion SPM® 7 Series. It should be used in conjunction with each datasheet as well as Fairchild’s application notes and technical support team. Please visit Fairchild’s website at [http://www.fairchildsemi.com](http://www.fairchildsemi.com).

<table>
<thead>
<tr>
<th>Application</th>
<th>Device Name</th>
<th>Max. Supply Voltage</th>
<th>Max. Power Rating</th>
<th>Topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>'Home Appliance</td>
<td>FSB70625</td>
<td>200 V DC</td>
<td>81 W</td>
<td>3-Phase Inverter</td>
</tr>
<tr>
<td>(Fan Motor)</td>
<td>FSB70325</td>
<td>200 V DC</td>
<td>49 W</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FSB70550</td>
<td>400 V DC</td>
<td>110 W</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FSB70450</td>
<td>400 V DC</td>
<td>110 W</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FSB70250</td>
<td>400 V DC</td>
<td>81 W</td>
<td></td>
</tr>
</tbody>
</table>

1.1. **Key Features**

- 3-Phase FRFET® Inverter with High-Voltage Integrated Circuit (HVIC)
- Maximum $R_{DS(on)}$: FSB70625=0.8 Ω, FSB70325=1.4 Ω, FSB70550=1.85 Ω, FSB70450=2.2 Ω, FSB70250=3.4 Ω
- High-Performance PQFN Package
- Open-Source Pins Separate from Low-Side MOSFETs for 3-Phase Current-Sensing
- Active-HIGH Interface Works with 3.3 V / 5 V Logic
- Schmitt-Trigger Input
- Optimized for Low Electromagnetic Interference (EMI)
- HVIC Temperature-Sensing for Temperature Monitoring
- HVIC for Gate Driving with Under-Voltage Protection (UVP)
- Interlock Function
- Isolation Rating: 1500 V$_{RMS}$ / Min.
- Moisture Sensitive Level (MSL) 3
- RoHS Compliant

The internal circuit diagram is shown in Figure 1. The $V_{TS}$ pin is from the HVIC and provides the temperature-sensing signal.
Figure 1. Internal Circuit Diagram
2. Pin Description

![Figure 2. Pin Numbers and Locations in PQFN Package (Top-Through View)](image)

Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Pin Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>/FO</td>
<td>Fault Output</td>
</tr>
<tr>
<td>2</td>
<td>V&lt;sub&gt;TS&lt;/sub&gt;</td>
<td>Voltage Output of HVIC Temperature</td>
</tr>
<tr>
<td>3</td>
<td>Cfod</td>
<td>Capacitor for Duration Time of Fault Output</td>
</tr>
<tr>
<td>4</td>
<td>Csc</td>
<td>Capacitor (Low-Pass Filter) for Short-Circuit Current Detection Input</td>
</tr>
<tr>
<td>5</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Supply Bias Voltage for IC and MOSFETs Driving</td>
</tr>
<tr>
<td>6</td>
<td>IN_UH</td>
<td>Signal Input for High-Side U Phase</td>
</tr>
<tr>
<td>7</td>
<td>IN_VH</td>
<td>Signal Input for High-Side V Phase</td>
</tr>
<tr>
<td>8 (8a)</td>
<td>COM</td>
<td>Common Supply Ground</td>
</tr>
<tr>
<td>9</td>
<td>IN_WH</td>
<td>Signal Input for High-Side W Phase</td>
</tr>
<tr>
<td>10</td>
<td>IN_UL</td>
<td>Signal Input for Low-Side U Phase</td>
</tr>
<tr>
<td>11</td>
<td>IN_VL</td>
<td>Signal Input for Low-Side V Phase</td>
</tr>
<tr>
<td>12</td>
<td>IN_WL</td>
<td>Signal Input for Low-Side W Phase</td>
</tr>
<tr>
<td>13</td>
<td>Nu</td>
<td>Negative DC-Link Input for U Phase</td>
</tr>
<tr>
<td>14</td>
<td>U</td>
<td>Output for U Phase</td>
</tr>
<tr>
<td>15</td>
<td>N&lt;sub&gt;V&lt;/sub&gt;</td>
<td>Negative DC-Link Input for V Phase</td>
</tr>
<tr>
<td>16</td>
<td>V</td>
<td>Output for V Phase</td>
</tr>
<tr>
<td>17</td>
<td>W</td>
<td>Output for W Phase</td>
</tr>
<tr>
<td>18</td>
<td>N&lt;sub&gt;W&lt;/sub&gt;</td>
<td>Negative DC-Link Input for W Phase</td>
</tr>
<tr>
<td>19</td>
<td>V&lt;sub&gt;S(W)&lt;/sub&gt;</td>
<td>High-Side Bias Voltage Ground for W Phase MOSFET Driving</td>
</tr>
<tr>
<td>20</td>
<td>P&lt;sub&gt;W&lt;/sub&gt;</td>
<td>Positive DC-Link Input for W Phase</td>
</tr>
<tr>
<td>21</td>
<td>P&lt;sub&gt;V&lt;/sub&gt;</td>
<td>Positive DC-Link Input for V Phase</td>
</tr>
<tr>
<td>22</td>
<td>P&lt;sub&gt;U&lt;/sub&gt;</td>
<td>Positive DC-Link Input for U Phase</td>
</tr>
<tr>
<td>Pin #</td>
<td>Name</td>
<td>Pin Description</td>
</tr>
<tr>
<td>-------</td>
<td>---------</td>
<td>------------------------------------------------------</td>
</tr>
<tr>
<td>23(23a)</td>
<td>$V_{S(V)}$</td>
<td>High-Side Bias Voltage Ground for V Phase MOSFET Driving</td>
</tr>
<tr>
<td>24(24a)</td>
<td>$V_{S(U)}$</td>
<td>High-Side Bias Voltage Ground for U Phase MOSFET Driving</td>
</tr>
<tr>
<td>25</td>
<td>$V_{B(U)}$</td>
<td>High-Side Bias Voltage for U phase MOSFET Driving</td>
</tr>
<tr>
<td>26</td>
<td>$V_{B(V)}$</td>
<td>High-Side Bias Voltage for V phase MOSFET Driving</td>
</tr>
<tr>
<td>27</td>
<td>$V_{B(W)}$</td>
<td>High-Side Bias Voltage for W phase MOSFET Driving</td>
</tr>
</tbody>
</table>
3. Application Block Diagram

Figure 3. Block Diagram of Outdoor Fan Motor for Air-Conditioner
4. Schematic

Figure 4. Schematic for 3-Phase Inverter Part (Direct Coupling)
5. Key Parameter Design

5.1. Selection of Bootstrap Capacitance ($C_{BS}$)

The current flow path of the bootstrap circuit is shown in Figure 5. When $V_S$ is pulled down to ground (either through the low-side or the load), bootstrap capacitor $C_{BS}$ is charged through bootstrap diode $D_{BS}$ and resistor $R_{BS}$ from the $V_{DD}$ supply.

![Figure 5. Bootstrap Circuit](image)

The bootstrap capacitor of the Motion SPM® 7 Series can be calculated by:

$$C_{BS} = \frac{Q_{BS}}{\Delta V_{BS}}$$  \(1\)

where:
- $Q_{BS}$ = Total gate charge from $C_{BS}$; and
- $\Delta V_{BS}$ = Allowable drop voltage of the $C_{BS}$ (voltage ripple).

Total gate charge, $Q_{BS}$, required by the bootstrap capacitor, can be calculated by:

$$Q_{BS} = Q_g + Q_{LS} + (I_{LK,D} + I_{LK,C} + I_{QBS}) \times t_{ON}$$  \(2\)

where:
- $Q_g$ = Gate charge to turn on the high-side MOSFET;
- $Q_{LS}$ = Level-shift charge required per cycle;
- $I_{LK}$ = Total leakage current;
- $I_{LK,D}$ = Bootstrap diode leakage current;
- $I_{LK,C}$ = Bootstrap capacitor leakage current, which can be ignored if it is not an electrolytic capacitor;
- $I_{QBS}$ = Quiescent current of gate driver IC; and
- $t_{ON}$ = Maximum on pulse width of high-side MOSFET.

The total leakage current can be calculated by summing all of the individual components’ leakage currents. In case of FSB70325, minimum $C_{BS}$ is calculated as:

$$C_{BS_{\text{min}}} = \frac{Q_{BS}}{\Delta V_{BS}} = \frac{Q_g + Q_{LS} + (I_{LK,D} + I_{LK,C} + I_{QBS}) \times t_{ON}}{\Delta V_{BS}}$$  \(3\)
\[ C_{BS} = \frac{50 \mu C + (100 \mu A + 70 \mu A) \times 200 \mu s}{0.1 V} = 0.84 \mu F \]

→ More than two times (2X) → 2.2 µF

where:

- \(V_{DD}=15\) V
- Bootstrap diode = US1J
- \(Q_g + Q_{LS} = \) Approximate maximum 50 nC (designed value);
- \(I_{L,K,D} = 100 \mu A\) (maximum value from datasheet);
- \(I_{L,K,C} = 0\) (ceramic capacitor);
- \(I_{QBS}=70 \mu A\) (maximum value from datasheet);
- \(t_{ON}= 200 \mu s\) (depends on system);
- \(\Delta V_{BS} = 0.1 V\) (depends on system);

Recommended \(C_{BS}\) is normally 2~3 times \(C_{BS\_min}\).

### 5.2. Initial Charging Sequence for Bootstrap Capacitor

Adequate on-time duration of the low-side MOSFET to fully charge the bootstrap capacitor is required for initial bootstrap charging. In case of the Motion SPM® 7 Series, the initial charging time \((t_{charge})\) can be calculated from the following equation:

\[ t_{charge} = C_{BS} \times R_{BS} = \frac{1}{\delta} \times \frac{1}{V_{DD} - V_{BS\_min} - V_F - V_{LS}} \]

where:

- \(V_F = \) Forward voltage drop across the bootstrap diode;
- \(V_{BS\_min} = \) Minimum value of the bootstrap capacitor;
- \(V_{LS} = \) Voltage drop across the low-side IGBT or load; and
- \(\delta = \) Duty ratio of PWM.

To charge three bootstrap capacitors at the same time; theoretically, the maximum initial charging current could exceed OCP level. Therefore, initial charging time for bootstrap capacitors should be separated as shown in Figure 6.

**Figure 6. Bootstrap Recommended Initial Bootstrap Capacitors Charging Sequence**
5.3. **Selection of Shunt Resistor (One Shunt)**

The value of shunt resistor is calculated by the following equations.

Maximum short-circuit (SC) current trip level (depends on user selection):

\[
I_{SC(\text{max})} = 1.5 \times I_{D(\text{max})}
\]  
(5)

SC trip reference voltage (depends on datasheet):

\[
V_{SC} = \text{Min.0.45 V, Typ.0.5 V, Max.0.55 V}
\]  
(6)

Shunt resistance:

\[
I_{SC(\text{max})} = \frac{V_{SC(\text{max})}}{R_{SHUNT(\text{min})}} \rightarrow R_{SHUNT(\text{min})} = \frac{V_{SC(\text{max})}}{I_{SC(\text{max})}}
\]  
(7)

If the deviation of the shunt resistor is limited below ±5%:

\[
R_{SHUNT(\text{typ})} = \frac{R_{SHUNT(\text{min})}}{0.95}, R_{SHUNT(\text{max})} = R_{SHUNT(\text{typ})} \times 1.05
\]  
(8)

Actual SC trip current level becomes:

\[
I_{SC(\text{typ})} = \frac{V_{SC(\text{typ})}}{R_{SHUNT(\text{typ})}}, I_{SC(\text{min})} = \frac{V_{SC(\text{min})}}{R_{SHUNT(\text{max})}}
\]  
(9)

Inverter output power:

\[
P_{\text{OUT}} = \sqrt{3} / \sqrt{2} \times M_I \times V_{\text{DC Link}} \times I_{\text{RMS}} \times PF
\]  
(10)

where:

- $M_I$ = modulation index;
- $V_{\text{DC Link}}$ = DC link voltage;
- $I_{\text{RMS}}$ = Maximum load current of inverter; and
- $PF$ = power factor;

Average DC current:

\[
I_{\text{DC AVG}} = \frac{V_{\text{DC Link}}}{(P_{\text{out}} \times \text{Eff})}
\]  
(11)

where:

- $\text{Eff} =$ inverter efficiency.

The power rating of shunt resistor is calculated by the following equation:

\[
P_{\text{SHUNT}} = \frac{(I^2_{\text{DC AVG}} \times R_{SHUNT} \times \text{Margin})}{\text{Derating Ratio}}
\]  
(12)

where:

- $R_{SHUNT} =$ Shunt resistor typical value at $T_C=25^\circ\text{C}$
- $\text{Derating Ratio} =$ Derating ratio of shunt resistor at $T_{SHUNT}=100^\circ\text{C}$ (from datasheet of shunt resistor); and
- $\text{Margin} =$ Safety margin (determined by customer).
Shunt Resistor Calculation Examples

Calculation Conditions:

- **DUT:** FSB70450, Tolerance of \( R_{\text{SHUNT}} \): ±5%
- **SC Trip Reference Voltage:**
  - \( V_{\text{SC(min)}} = 0.45 \text{ V} \), \( V_{\text{SC(typ)}} = 0.50 \text{ V} \), \( V_{\text{SC(max)}} = 0.55 \text{ V} \)
- **Maximum Load Current of Inverter (I_{\text{RMS}}):** 0.4 A\(_{\text{rms}}
- **Maximum Peak Load Current of Inverter (I_{\text{D(max)}}):** 0.6 A
- **Modulation Index (MI):** 0.9
- **V\text{DC Link (V}_{\text{DC LINK}}):** 300 V
- **Power Factor (PF):** 0.8
- **Inverter Efficiency (Eff):** 0.98
- **Shunt Resistor Value at T\(_c\)=25°C (R_{\text{SHUNT}}):** 0.25 Ω
- **Derating Ratio of Shunt Resistor at T_{\text{SHUNT}}=100°C:** 70%
- **Safety Margin:** 20%

Calculation Results:

- \( I_{\text{SC(max)}}: 1.5 \times I_{\text{D(max)}} = 1.5 \times 0.6 \text{ A} = 0.9 \text{ A} \)
- \( R_{\text{SHUNT(min)}}: V_{\text{SC(max)}} / I_{\text{SC(max)}} = 0.55 \text{ V} / 0.9 \text{ A} = 0.61 \text{ Ω} \)
- \( R_{\text{SHUNT(typ)}}: R_{\text{SHUNT(min)}} / 0.95 = 0.61 \text{ Ω} / 0.95 = 0.64 \text{ Ω} \)
- \( R_{\text{SHUNT(max)}}: R_{\text{SHUNT(typ)}} \times 1.05 = 0.64 \text{ Ω} \times 1.05 = 0.67 \text{ Ω} \)
- \( I_{\text{SC(min)}}: V_{\text{SC(min)}} / R_{\text{SHUNT(max)}} = 0.45 \text{ V} / 0.67 \text{ Ω} = 0.67 \text{ A} \)
- \( I_{\text{SC(typ)}}: V_{\text{SC(typ)}} / R_{\text{SHUNT(typ)}} = 0.5 \text{ V} / 0.64 \text{ Ω} = 0.78 \text{ A} \)
- \( P_{\text{OUT}} = \sqrt{3} \times \sqrt{2} \times MI \times V_{\text{DC Link}} \times I_{\text{RMS}} \times \text{PF} = 105.8 \text{ W} \)
- \( I_{\text{DC AVG}} = (P_{\text{OUT}} / \text{Eff}) / V_{\text{DC Link}} = 0.36 \text{ A} \)
- \( P_{\text{SHUNT}} = (I_{\text{DC AVG}}^2 \times R_{\text{SHUNT}} \times \text{Margin}) / \text{Derating \ Ratio} = (0.36^2 \times 0.67 \times 1.2) / 0.7 = 0.15 \text{ W} \) (therefore, recommended power rating of shunt resistor is 0.2 W)
5.4. Design of Over-Temperature Protection (OTP) Circuit

The Motion SPM® 7 Series provides sensing output of the temperature for the OTP circuit. The $V_{TS}$ PIN is directly connected to the built-in temperature sensor in HVIC, as shown in the Figure 7.

Note:
1. $V_{TS}$ is only for sensing temperature related to the module and cannot shutdown MOSFETs automatically.

Figure 7. Position of the Built-in Temperature Sensor

Figure 8 is V-T curve of Temperature Sensing (TS) function in Motion SPM® 7 Series.

Figure 8. V-T Curve of Temperature Sensing (TS) Function
Figure 9 is a typical application circuit for the TS function. In this reference design, the set level is 100°C ($V_{TS}=2.1$ V), the reset level is 80°C ($V_{TS}=1.72$ V), and the hysteresis temperature is 20°C (Figure 10). If using an Analog-to-Digital Converter (ADC) port, a capacitor is needed between the VTS and GND pins (Figure 11).
5.5. Interlock Function

The Motion SPM® 7 Series has an interlock function to prevent shoot-through when high- and low-side input, HIN and LIN, are placed in HIGH status at the same time.

The behavior of the interlock function, based on the one-leg diagram in Figure 12 is shown in Table 2 and Figure 13.

![One-Leg Diagram of Motion SPM® 7 Series](image)

**Table 2. Logic Table for Inverter Output**

<table>
<thead>
<tr>
<th>HIN</th>
<th>LIN</th>
<th>Output</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Z</td>
<td>Both MOSFETs OFF</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Low-Side MOSFET ON</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>VDC</td>
<td>High-Side MOSFET ON</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Forbidden</td>
<td>Interlock (refer to Figure 13)</td>
</tr>
<tr>
<td>Open</td>
<td>Open</td>
<td>Z</td>
<td>Same as (0,0)</td>
</tr>
</tbody>
</table>

5.6. Selection of $C_{FOD}$

The external capacitor connected between the $C_{FOD}$ and COM pins determines the fault output duration ($t_{FOD}$).

$t_{FOD}$ can be calculated by the following approximate equation:

$$t_{FOD} = C_{FOD} / (24 \times 10^{-6}) \text{ [s]}$$

(13)
5.7. Printed Circuit Board (PCB) Layout Guidance

- The VIN RC filter should be placed as close as possible to the SPM 7 product.
- It is recommended to connect control GND and power GND at only a point (not copper pattern and don't make a loop in GND pattern). The wiring should be as short as possible.
- The capacitor between VCC and COM should be placed as close as possible to the SPM.
- U, V, W Copper pattern should be as wide as possible.
- The main electrolytic capacitor should be placed as close as possible to the snubber capacitor.
- Wiring between NU, NV, NW and shunt resistor should be as short as possible.
- The capacitor between VCC and COM should be placed as close as possible to the SPM.
- P Copper pattern should be as wide as possible.
- Place snubber capacitor between P and N and closely to terminals.
- The main electrolytic capacitor should be placed to the snubber capacitor as close as possible.

Figure 14. PCB Layout Guidance
Related Resources

AN-9077: Motion SPM® 7 Series Assembly Guide
AN-9078: Motion SPM® 7 Series Assembly Guide
FSB70325 – Motion SPM® 7 Series
FSB70625 – Motion SPM® 7 Series
FSB70250 – Motion SPM® 7 Series
FSB70450 – Motion SPM® 7 Series
FSB70550 – Motion SPM® 7 Series

SPM® Module Design Guide
Motion Control Design Tool

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